

Appendix A

d_logic.2 System Overview

A.1 System Overview

The d_logic.2 board is a custom-designed circuit based on the Xilinx XC9572XL-10VQ44C cPLD and some accompanying hardware. The recommended development software is the ISE WebPack available free of charge from Xilinx. This section will cover the specifics of the board. Further information about the XC9572XL chip or the ISE WebPack can be found from Xilinx.

A.2 Parts of the Logic Board

The various parts of the logic board are: I/ O Connectors, Power and Clock Input Connectors, the Clock Generation Sub-system, IR Communications system, Switches and LEDS, and the Programming Connection. Figure C.2 illustrates these parts.

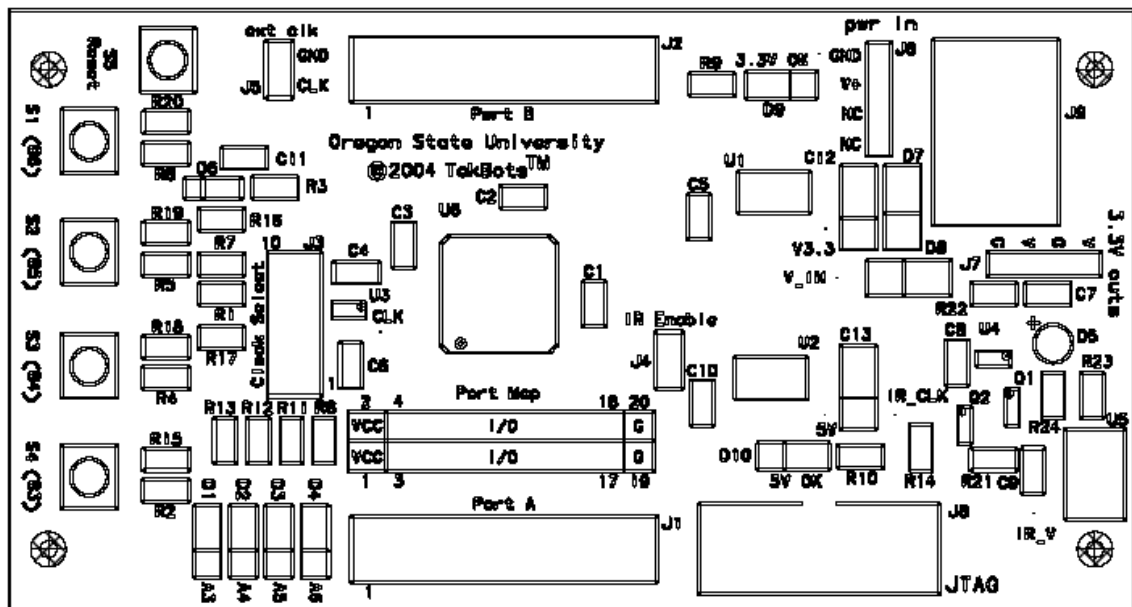


Figure A.1: d_logic.2 Silk Screen

A.3 I/O Connectors

A good rule of thumb when using the I/ O ports on the d_logic board and any other system is that, if you do not understand it, find out more, and do not use it until you do understand it. You can damage the d_logic board if you are not careful.

A.3.1 Port A

This section has a list/description of the Port A parts. Refer to Figure A.2 for the I/O Connections in Port A. Port A consists of:

- 2 ground pins
- 2 3.3V pins
- diodes 1 through 4
- the IR transmit
- 11 unused general I/ O pins

3.3V	1	2	3.3V
IO_1 (D1) Pin 39	3	4	IO_2 (D2) Pin 40
IO_3 (D3) Pin 41	5	6	IO_4 (D4) Pin 42
IO_GCK3 (IR Xmit) Pin 1	7	8	IO_5 Pin 2
IO_6 Pin 3	9	10	IO_7 Pin 5
IO_8 Pin 6	11	12	IO_9 Pin 7
IO_10 Pin 8	13	14	IO_11 Pin 12
IO_12 Pin 13	15	16	IO_13 Pin 14
IO_14 Pin 16	17	18	IO_15 Pin 18
GND	19	20	GND

J1 - PORT A

Figure A.2: I/O Connections in Port A

Pins 1 and 2 are directly connected to the 3.3V power supply. Be very cautious while using these, as these pins are not current-limited. It is possible to damage other portions of the circuitry if these pins are shorted to them.

Pins 19 and 20 are connected to ground. These pins also are not current-limited; therefore, be cautious while using these pins as well.

Pins 8 through 18 are general-purpose I/O pins. They can be used as either inputs or outputs, and are connected only to the cPLD chip. There are no external pull-up or pull-down resistors, so the user needs to take care of input termination. (However, the XC9572XL does have internal pull-up resistors that can be enabled by the user).

Pins 3 through 6 can be used as general-purpose inputs or outputs, but they have the LED indicators D1 through D4 connected to them. When used as outputs, the user needs to be aware of the additional current drawn on each pin (of approximately 4 mA), due to the LEDs. Conversely, when used as inputs, users also need to realize that their input device will need to be able to supply the same amount of current.

Pin 7 is connected to the IR transmitter enable and the GCK3 input. More information on the IR transmitter sub-system can be found later in the IR Communications system section. The GCK3 input allows for an external clock signal to be connected and used by the cPLD.

A.3.2 Port B

This section has a list/description of the Port B parts. Refer to Figure A.3 for the I/O Connections in Port B. Port B contains:

- many of the global signaling lines
- some general purpose I/O pins
- grounds and 3.3V pins
- inputs from some of the on-board sub-systems

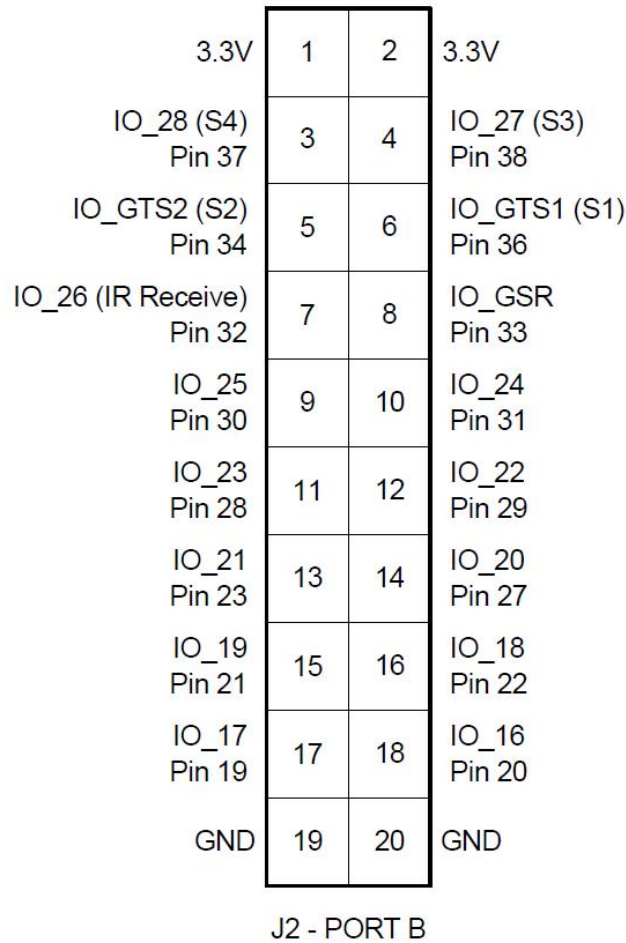


Figure A.3: I/O Connections in Port B

Pins 1 and 2 are connected to the 3.3V power supply. Be cautious while using them, as they are not current-limited.

Pins 19 and 20 are connected to ground. Again, use caution with them, as these pins are not current-limited.

Pins 9 through 18 are connected to general-purpose I/O pins that can be used for both inputs and outputs. There are no external pull-up or pull-down resistors. Therefore, the user needs to take care of input termination. (However, the XC9572XL does have internal pull-up resistors that can be enabled by the user).

Pins 3 and 4 are general-purpose I/O pins that are connected to the on-board switches S3 and S4. These switches are normally high and when they are pressed, they pull the pin low through a 1K ohm resistor. When using this

pin as an output, the user should remember that the pin is connected through a 4.7K ohm resistor to the 3.3V power supply. Therefore, if the switch is depressed, the pin is connected to ground through the 1K resistor.

Pins 5 and 6 are connected to on-board switches S1 and S2. These pins on the XC9572XI chip are used as either global-control pins for the chip, or as general-purpose I/ O pins. Be aware that the cPLD needs to be programmed correctly, depending on the desired use of these pins.

Pin 7 is a general use I/O pin connected to the IR receiver sub-system. More information on this can be found under the IR Communications system sub-section.

Pin 8 is connected to the Global Set-Reset pin of the cPLD. This pin can be configured for general I/O use within the cPLD via programming.

A.4 Power and Clock Input Connectors

In this section, we cover the descriptions for the External Clock Connector, Power Inputs, and the Auxiliary Power Output.

A.4.1 External Clock Connector

The external clock connection allows for any clock signal to be connected to the CLK2 pin of the cPLD. The capacitance of this connection is not guaranteed; so, a very fast clock input may not be possible. The user should verify the signal reaching the CLK2 pin of the cPLD, when a new clock is connected. Refer to Figure 24 for the external clock connections.

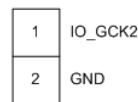


Figure A.4: J5 - External Clock

A.4.2 Power Inputs

The d.logic.2 board is supplied with power from one of two inputs, J6 or J9.

J6 is a TekBots standard power connector capable of powering the board starting from 6.5V to 18V, depending on the d.logic.2 board and the connected circuitry current requirements. Refer to Figure 25 for the power input connections in J6.

J9 is a 2.1mm coaxial power jack required a positive center pin connection. This standard size power jack can be found on many different types of DC power supplies. The DC power supply provided with TekBot kits will work with this connector.

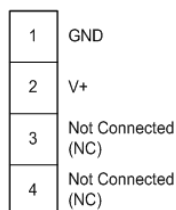


Figure A.5: J6 - Power Inputs



Only one power input should be used at a time. Severe damage to the d.logic board could result, if both supplies are connected at the same time.

A.4.3 Auxiliary Power Output

The auxiliary power output makes the connections of the peripherals to the d.logic.2 power easy. This connector has two positions providing both 3.3V and ground connection. Caution should be taken to not short these pins together as they could damage the d.logic.2 board. Refer to Figure A.6 for the auxiliary power output connections.

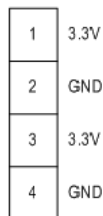


Figure A.6: J7 - Auxiliary Power Output



Do not use the auxiliary power output as a power input, because this bypasses the on-board power regulation and will certainly destroy the d.logic board.

A.5 Clock Generation Sub-system

The d.logic.2 board has an on-board variable oscillator connected to the CLK1 input of the cPLD. The heart of this sub-system is the LTC6900 IC. This device allows for a wide range of reliable and stable clock signals. The clock frequency supplied to the cPLD varies, based on the configuration of the clock selection jumpers on J3. Many configurations are available as shown below, in Figure A.7.

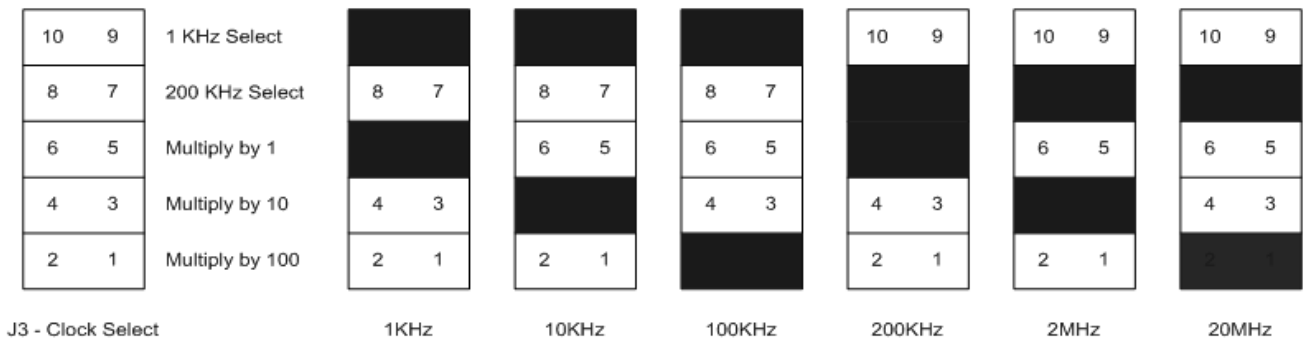


Figure A.7: J3 Configurations



Any settings (other than those shown above) may not function, and/or could result in damage to the d.logic board.

A.6 IR Communications System

The d_logic.2 board is equipped with an on-board IR transmitter and receiver pair, as shown below in Figure 28. The IR transmitter and receiver can be disabled by removing the IR enable jumper J4, thereby disconnecting them from the 5V power supply.

The IR communications system works by using the LTC6900, U4, to generate a 38 KHz signal. This signal is applied to the gate of Q2, causing it to turn off and on at that rate. Q1 is connected to the cPLD, which when set to a logical high, turns on. This is what allows the IR LED to turn off and on at the 38 KHz rate generated by the LCT6900.

The IR receiver is a tuned filter that observes only IR light. When a 38 KHz signal is noticed, it will pull its output pin to ground creating an active low signal. There is some error to this signal, so false triggers can be observed, especially in fluorescent light and sunlight, but these false 0s are normally very short in duration.

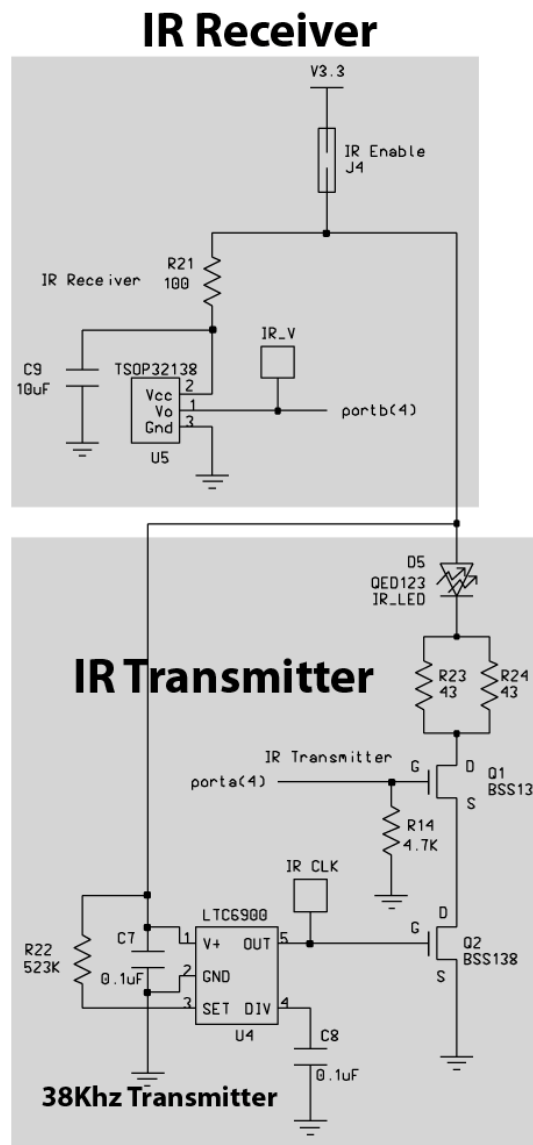


Figure A.8: IR communications schematic

A.7 Switches and LEDs

The d_logic.2 board has four switches and four LEDs that can be used as inputs and outputs for quick design testing. The schematics for these two systems are shown below, in Figures B.3 and B.4. The four LEDs will light when a logical 1, or when a 3.3V is applied to them. These are active high-input devices. The switches are connected to the cPLD on Port B. The pins on Port B will show that these inputs are a logical high at 3.3V, until the switch is pressed, at which point the inputs will go to ground, or logical 0. These are active low inputs.

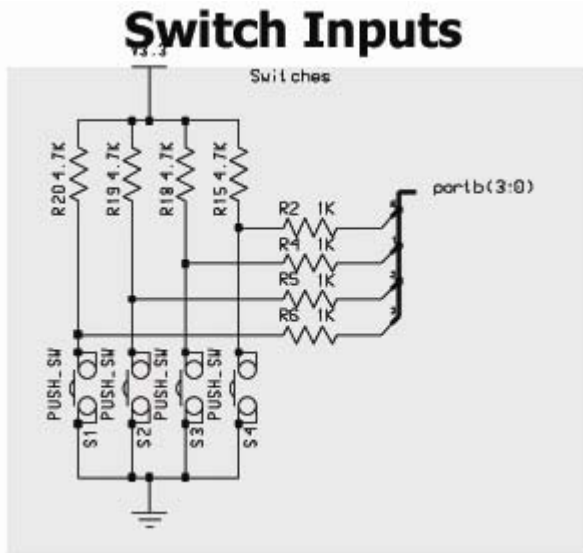


Figure A.9: Switch Inputs Schematic

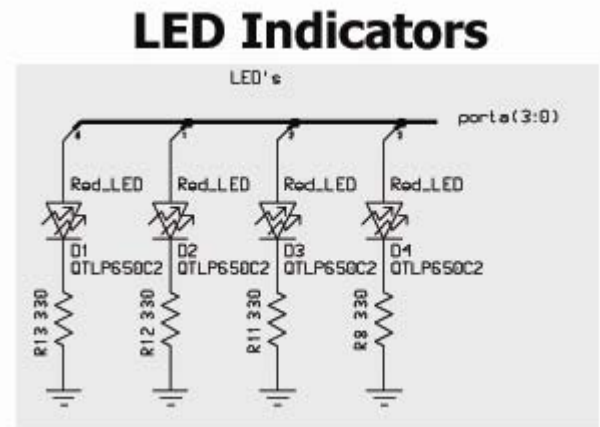


Figure A.10: LED Schematic

A.8 Programming Connection

The d_logic.2 board is programmed using a JTAG interface. There are many different models of JTAG programmers, so it is recommended you use the one included with the d_logic.2 board. The JTAG connector on the board (2x5 Male 0.1 connector) is used on other TekBots systems as well.



The programmers of the various systems, however, are NOT interchangeable. Serious damage to the board could result from improper usage.

Appendix B

Schematics

APPENDIX B. SCHEMATICS

B.1 Digital Logic Board

The schematic of the entire digital logic board can be seen in Figure B.1. This Appendix contains maximized illustrations of the schematics for each of the D-Logic board parts, which were reviewed in Appendix A.

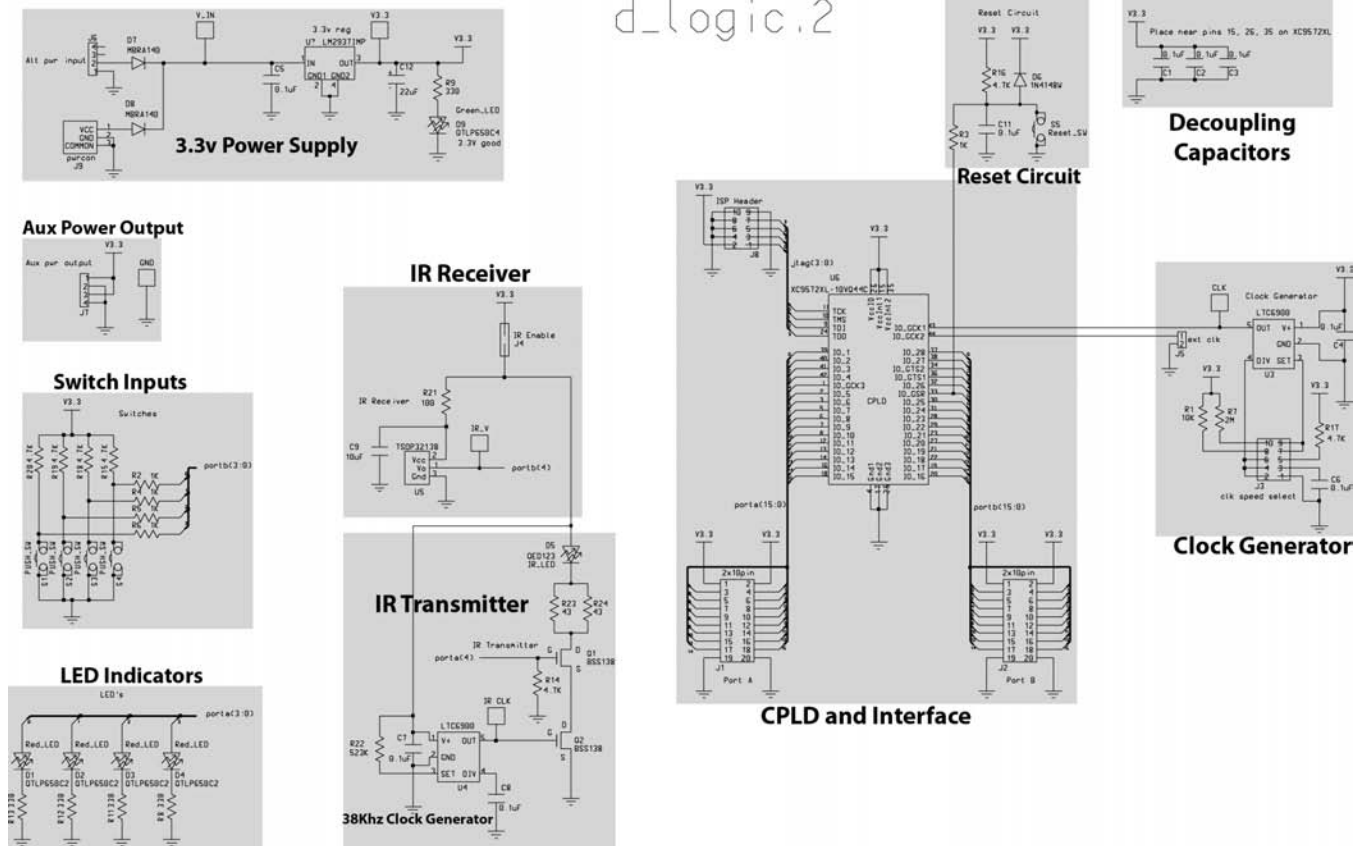


Figure B.1: The Digital Logic Board Schematic

B.2 Power Supplies

This section has the schematic for the power supplies, seen in Figure B.2.

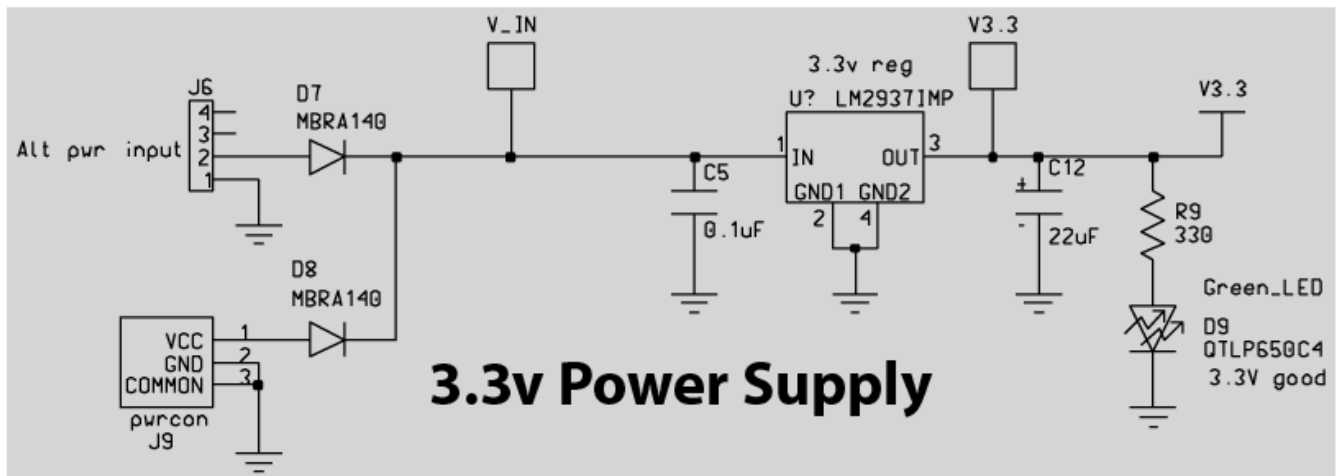


Figure B.2: Power Supplies Schematic

B.3 Switches, LEDs, and IR

This section has the schematic for the switch inputs, the LEDs, and the IR communications system, seen in Figures B.3, B.4, and B.5

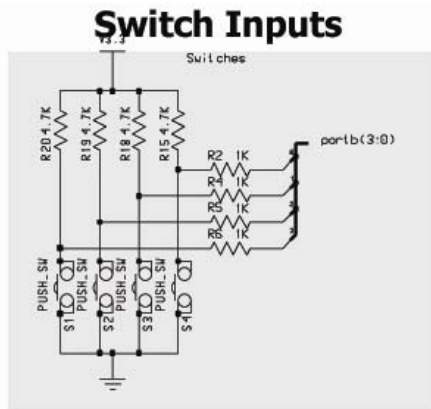


Figure B.3: Switch Inputs Schematic

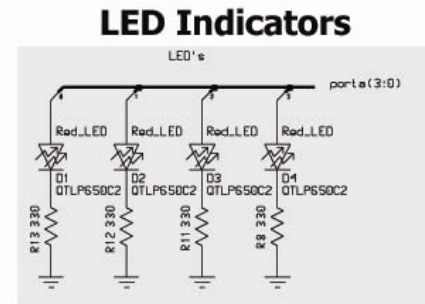


Figure B.4: LED Schematic

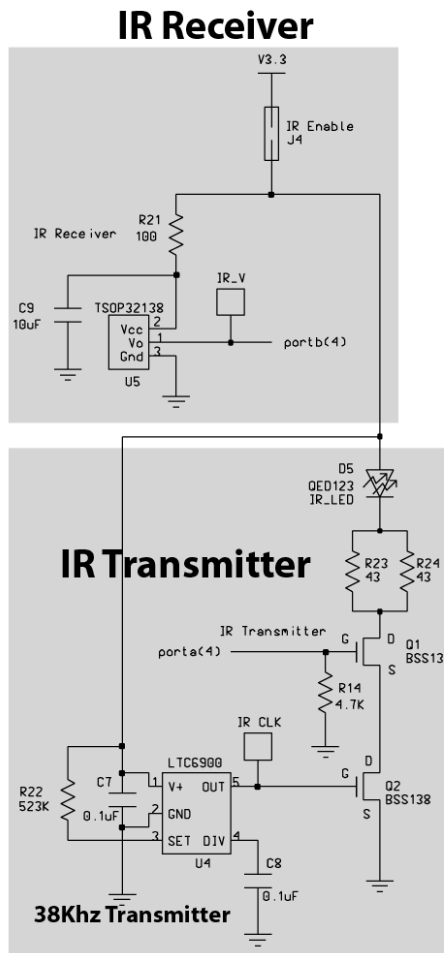


Figure B.5: IR communications schematic

B.4 Miscellaneous

This section has the last set of schematics: for the Reset Circuit, the Clock Generator, the cPLD and its Interface, and the decoupling capacitors. Also, notice how the reset circuit, the cPLD, and the clock generator are connected in Figure B.6.

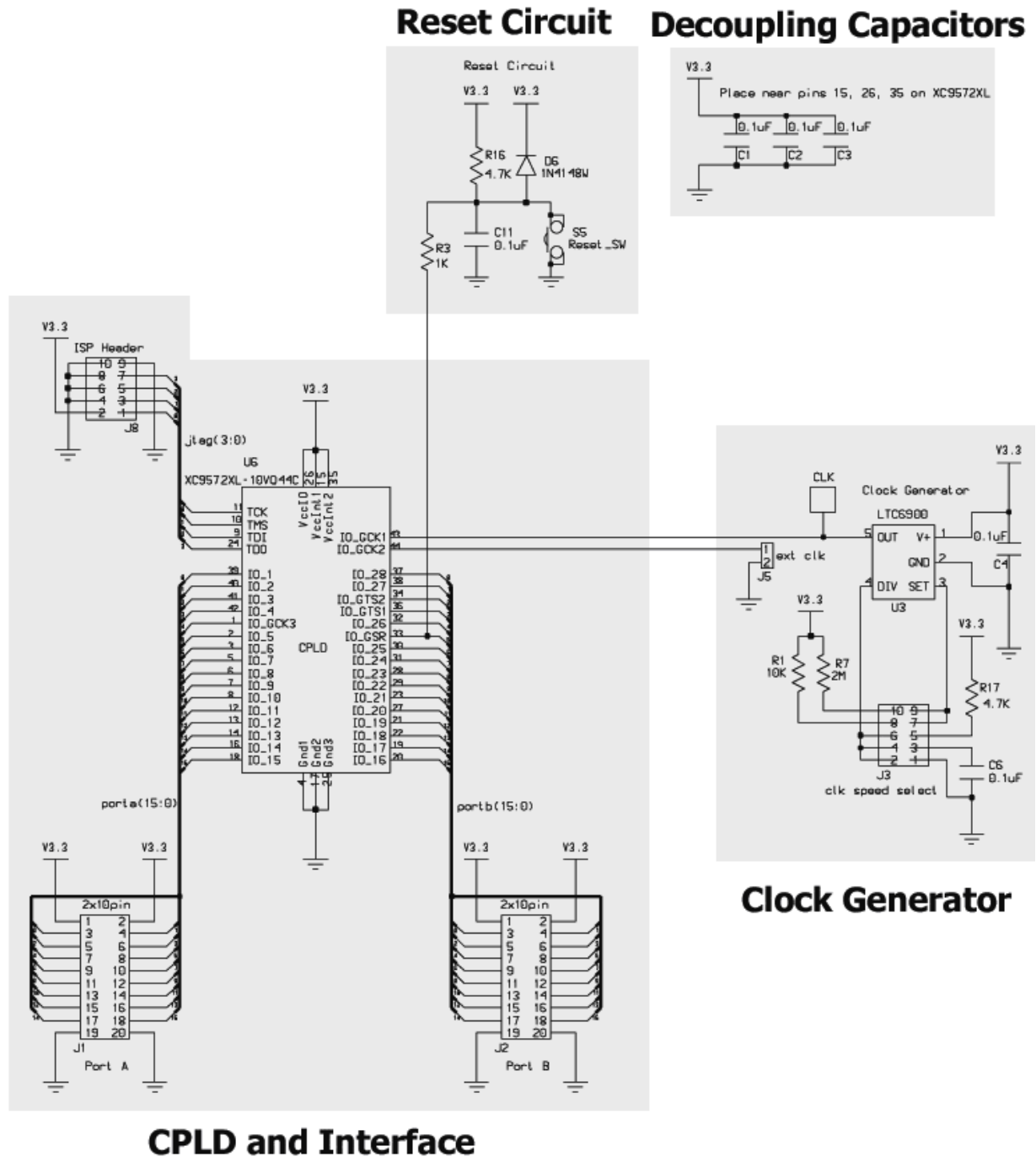


Figure B.6: Reset Circuit, cPLD and Interface, Clock Generator, and Decoupling Capacitors Schematic

Appendix C

Silk Screens and Pinouts

APPENDIX C. SILK SCREENS AND PINOUTS

This appendix has all the silk screens and pinouts used in this course.

C.1 d.logic.2

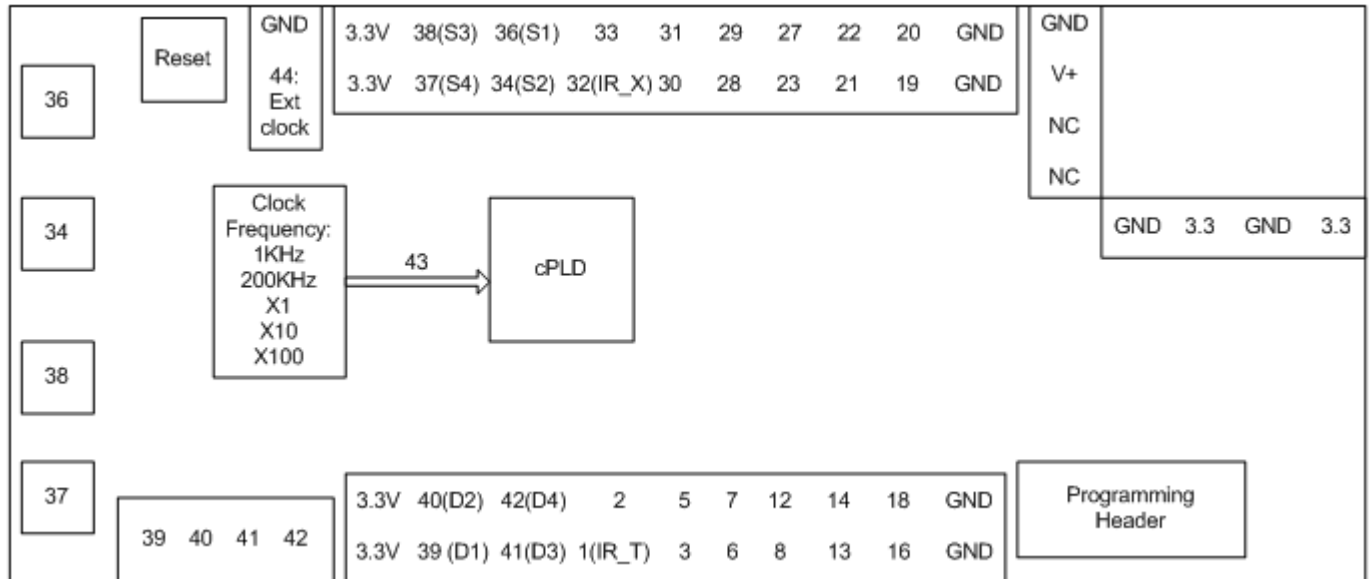


Figure C.1: The d.logic.2 Pinout

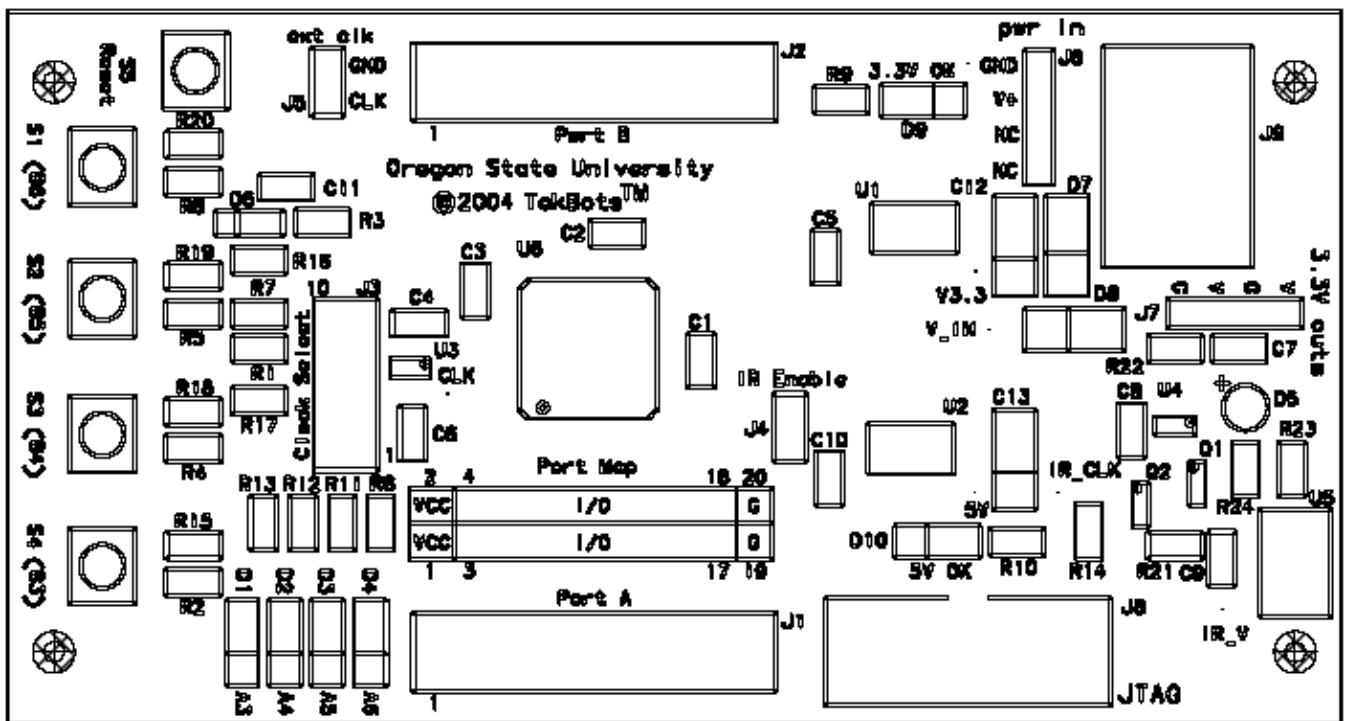


Figure C.2: d.logic.2 Silk Screen

Appendix D

Parts and Suppliers

APPENDIX D. PARTS AND SUPPLIERS

D.1 Parts List

Qty.	Description	Ref.	Fig.	Supplier	Supplier #
1	Digital Logic Board - d_logic.2		A	TekBots	d_logic.2
1	Universal Programmer Board		B	TekBots	usb_prog.2
1	LED - Red HLMP1700		C	Mouser	512-HLMP-1700
1	CAP .33UF 50V 20% CER RADIAL		D	DigiKey	399-2174-ND
4	SWITCH TACT 6MM MOM 100GF		E	DigiKey	SW400-ND
1	LED 7-SEG SGL CC RED RHDP .56"		F	DigiKey	MAN6980-ND
1	74HC573 Octal Transparent Latch		G	DigiKey	296-12815-5-ND
4	1/8 Watt, 10K Ω Resistor		H	Mouser	299-10K
8	1/ 8 Watt, 330 Ω Resistor		H	Mouser	299-330
1	78LM05 5 Volt Regulator (TO-92 Package)		I	Mouser	511-L78L05ABZ
1	DIP-14 Quad 2-Input AND		G	Mouser	511-M74HC08
1	DIP-14 Quad 2-Input OR Gate		G	Mouser	511-M74HC32
1	DIP-14 Quad Exclusive OR		G	Mouser	511-M74HC86

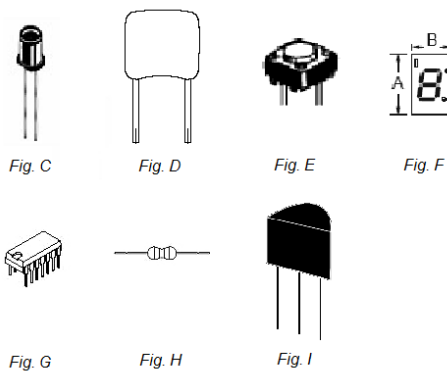


Figure D.1: Use these figures to determine which parts to use.

D.2 Suppliers List

DigiKey	701 Brooks Ave. South Thief River Falls, MN 56701-0677 (800) 344-4539 http://www.digikey.com
Mouser Electronics	1000 N. Main Street Mansfield, TX 76063 (800) 346-6873 http://www.mouser.com
TekBots	1110 Kelley Engineering Center Oregon State University Corvallis, OR 97331 http://eecs.oregonstate.edu/tekbots