

## **Chapter 4**

# **Combinational Logic (Seven Segment Driver)**

## 4.1 Section Overview

Being able to display numbers is useful. Seven segment displays are used in alarm clocks, VCRs, and microwaves. Section four builds a seven-segment display decoder, which is described in example 2.10 of the ECE 271 textbook .

## 4.2 Objectives

In this section, the following items will be covered:

1. Define the problem, what is the controller really doing?
2. Define the inputs to the combinational logic.
3. Define the outputs from the combinational logic.

## 4.3 Materials

1. Xilinx ISE 12 software (Currently installed on the lab computers)
2. Digital Logic Board (d.logic.2 board)
3. Small breadboard, buffer chip (octal latch), and resistors
4. MAN 6980 seven segment display

## 4.4 Procedure

There are 5 steps to digital logic design:

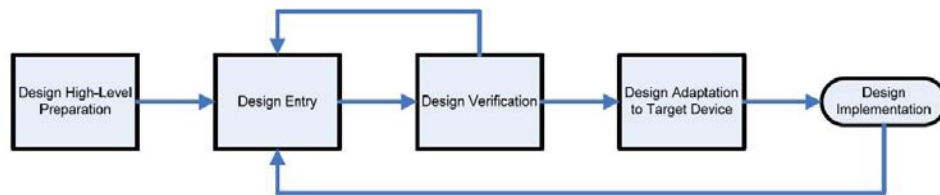


Figure 4.1: Use this process for designing the seven segment display.

1. *High Level Preparation:* Figure 4.2 shows all of the different outputs that the seven segment decoder should produce. Shade in the segments that should be on for each input, 0-F.

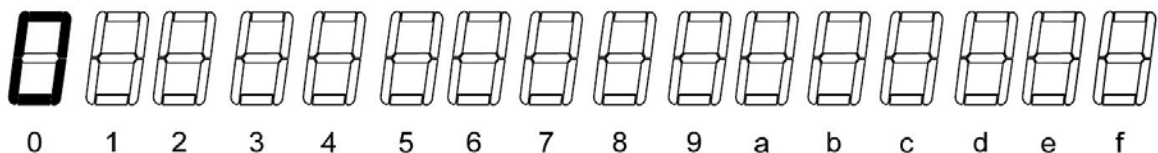


Figure 4.2: The decoder should produce all 16 outputs

Make a block diagram

Add the power source used for each of the three blocks.

Label all Port and Port pins that are used for this project on the block diagram.

Label which inputs on the buffer chip are connected to T, U, V, W, X, Y, and Z.

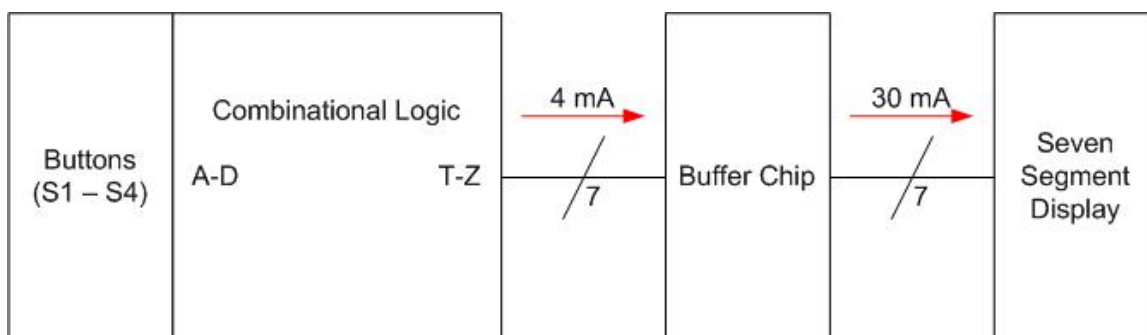


Figure 4.3: This is the block diagram for the remote control

Make a functional truth table

Use the shading in Figure 4.2 to fill in the functional truth table below.

Input Hex	Inputs, ABCD	$Seg_A$	$Seg_B$	$Seg_C$	$Seg_D$	$Seg_E$	$Seg_F$	$Seg_G$
0	0000	1	1	1	1	1	1	0
1	0001							
2	0010							
3	0011							
4	0100							
5	0101							
6	0110							
7	0111							
8	1000							
9	1001							
A	1010							
B	1011							
C	1100							
D	1101							
E	1110							
F	1111							

Minimize the logic

Use seven K-maps to make minimized logic for  $Seg_A$ ,  $Seg_B$ ,  $Seg_C$ ,  $Seg_D$ ,  $Seg_E$ ,  $Seg_F$ , and  $Seg_G$ . Write out the minimized Boolean Equations for each output.

2. *Design Entry*: Enter the design using the same process as in Section 2.



A larger workspace in Xilinx will be needed to fit the entire minimized schematic. To change the schematic size click Edit → Change Sheet Size... In the dialog box use the dropdown menu to select a larger sheet size.

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3. *Design Verification:* Simulate the design to verify correct operation of the digital logic. Use Section 3 as a guide for this process.
4. *Design Adaptation to Target Device:* Follow the same process for using PACE and iMPACT as in Section 2.
5. *Design Implementation:* Program the Xilinx CPLD with the Universal Programmer software.



TA Signature: \_\_\_\_\_  
(Seven Segment display is working and all lab steps are shown)

### 4.5 Study Questions

1. When is a simulation necessary? Was it useful for this section?
2. Attach the detailed block diagram, digital logic schematic, and simulation results for this project.

### 4.6 Challenge - Extra Credit

#### 4.6.1 Option 1

Make a two digit seven segment display. Use the MAN 6940 seven segment display, which has two digits. Each digit has an independent common cathode. There should be eight inputs to this decoder. There should be seven outputs for the seven segments, and two outputs for the two common cathodes. Design the electrical circuits for driving the common cathodes and the digital logic for displaying the turning on the correct segments when the corresponding common cathode is enabled.

#### 4.6.2 Option 2

Design and simulate the Xilinx for a two digit seven segment display. Create your outputs as if they were going to be used by the pins on the MAN 6940.