

Pre-Lab

1. Write out the Verilog for a two input AND gate.

(Hint: Try not to make a new module for this description. Use only one line of Verilog.)

2. Write out the Verilog for a 2:1 multiplexer with 1-bit inputs and output.

(Hint: Look in the textbook for help.)

```
module mux2 (
```

```
endmodule
```