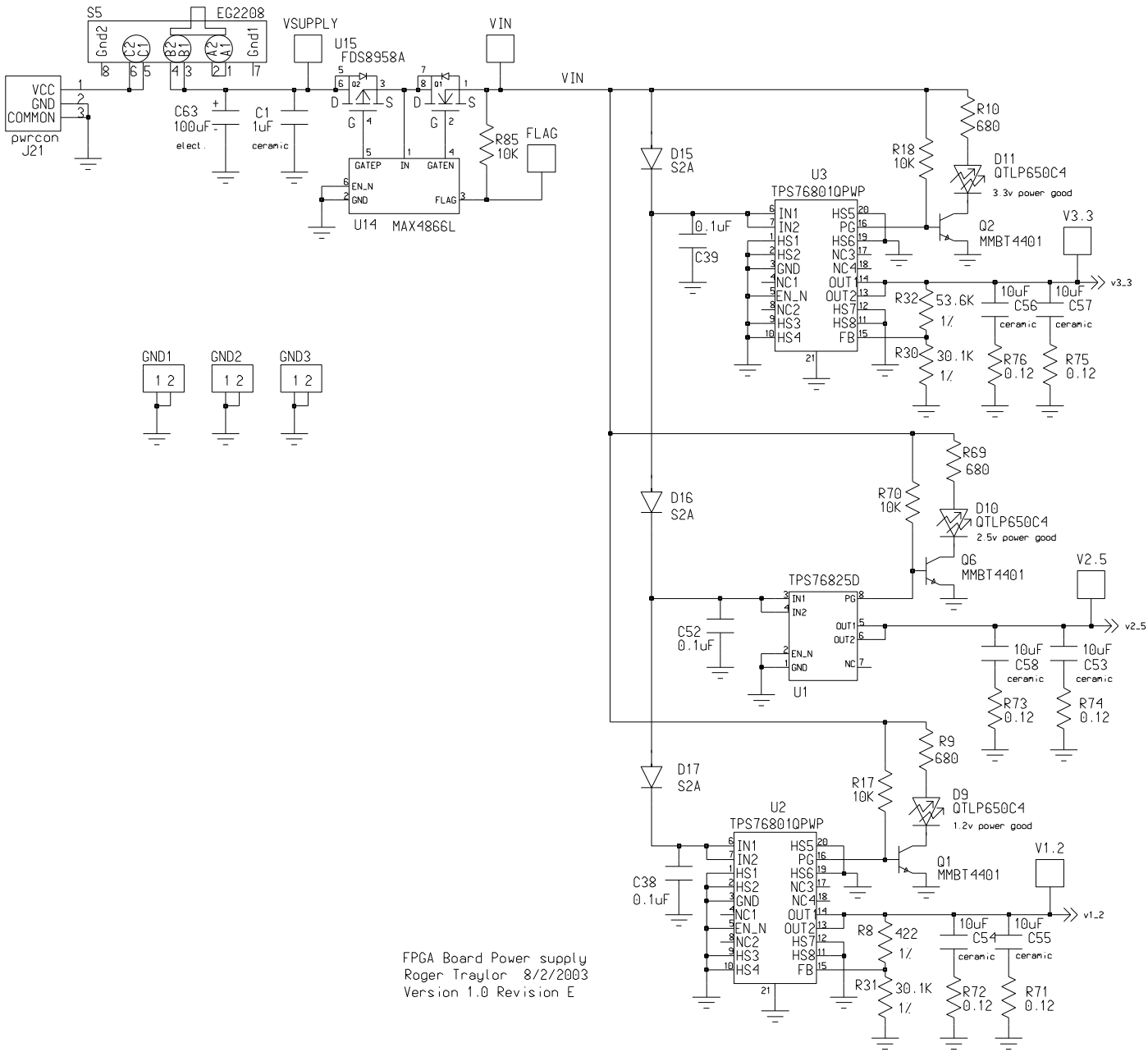
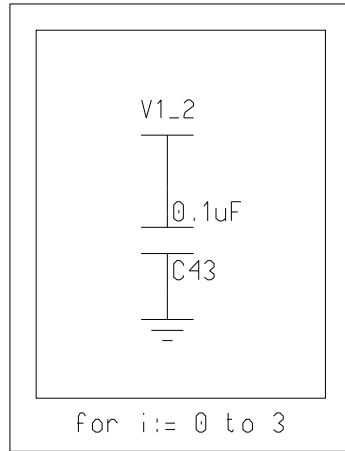
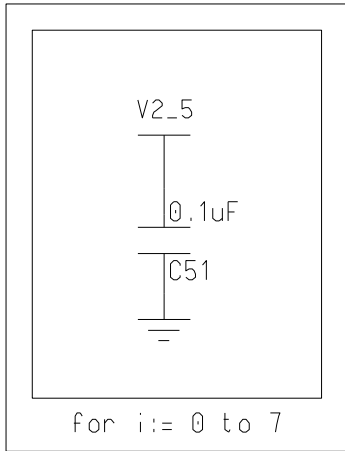


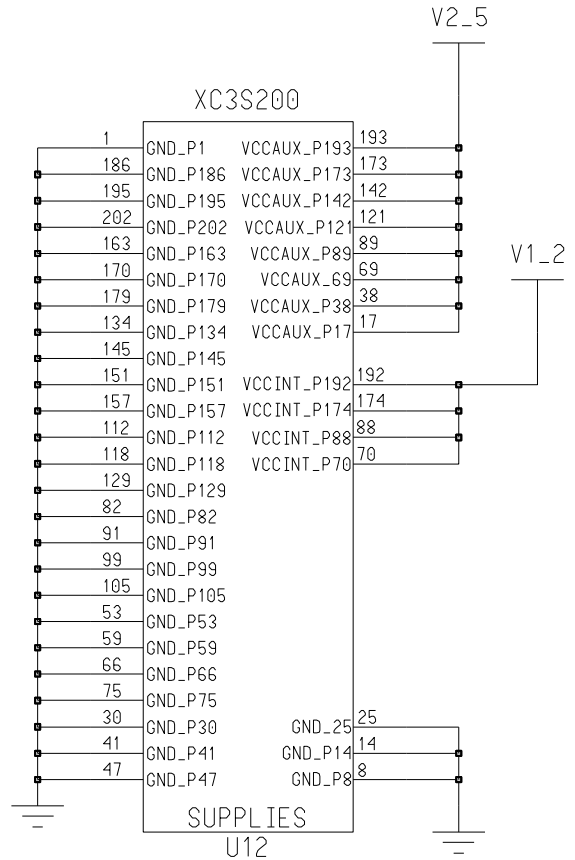
FPGA Board - Bank 0 RS232, LCD, PS2
 Roger Traylor 9/06/05
 Version 1.2 Revision D

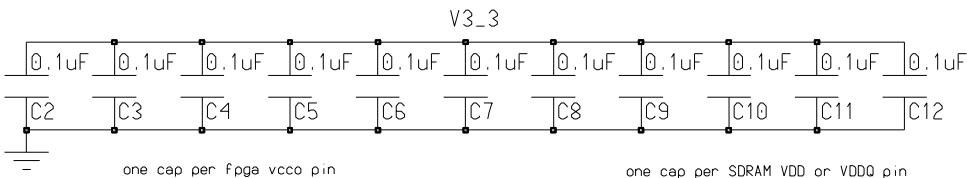
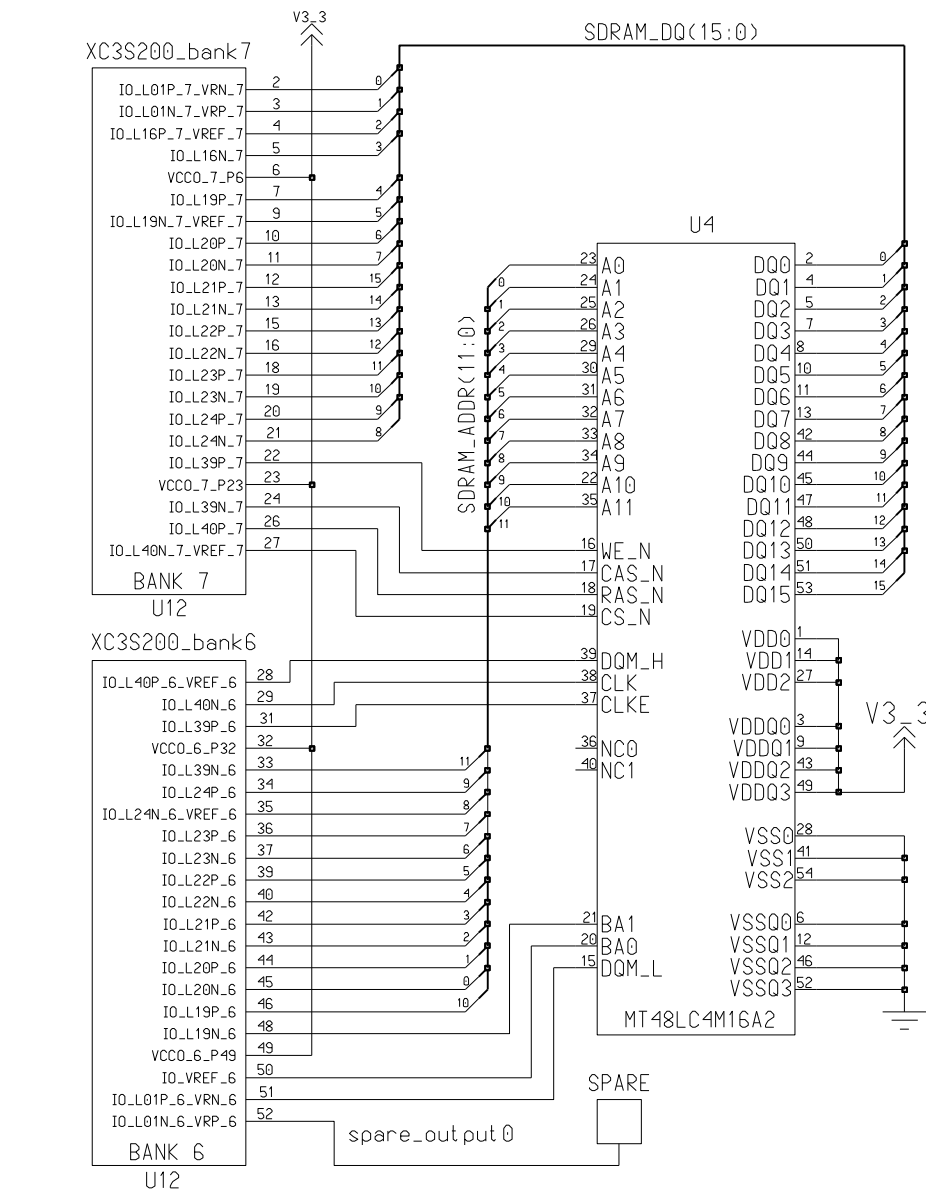


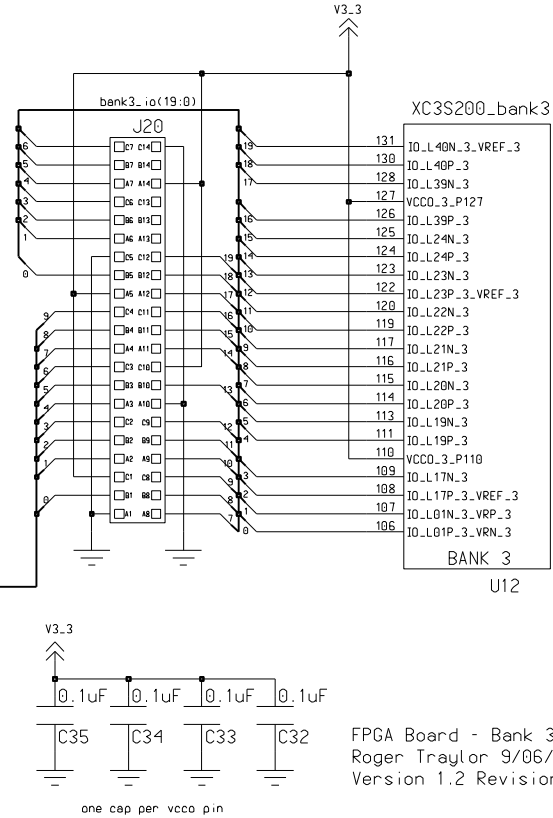
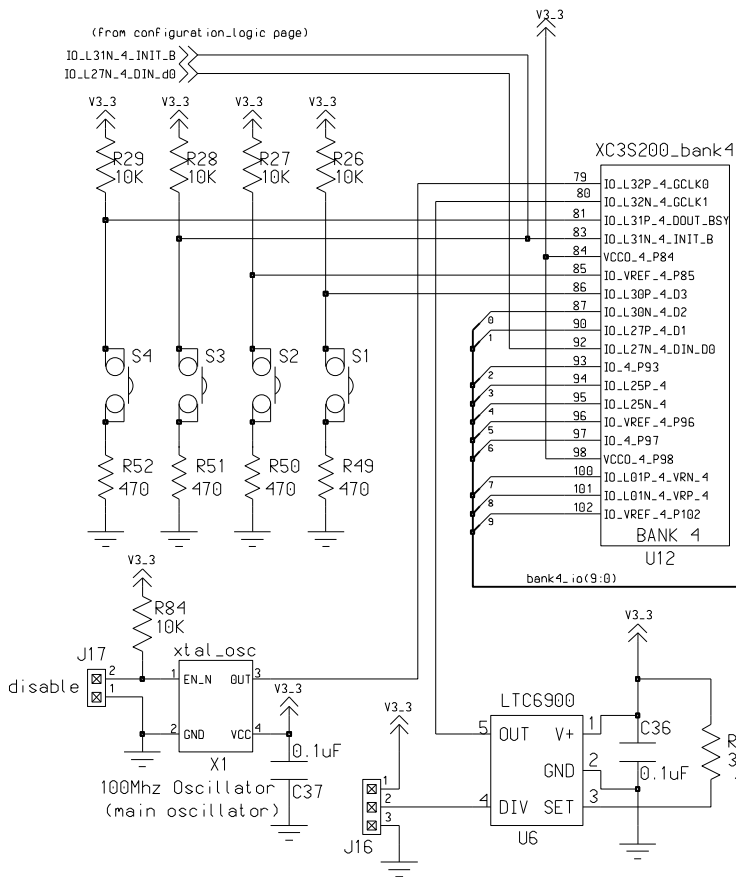
FPGA Board Power supply
 Roger Traylor 8/2/2003
 Version 1.0 Revision E

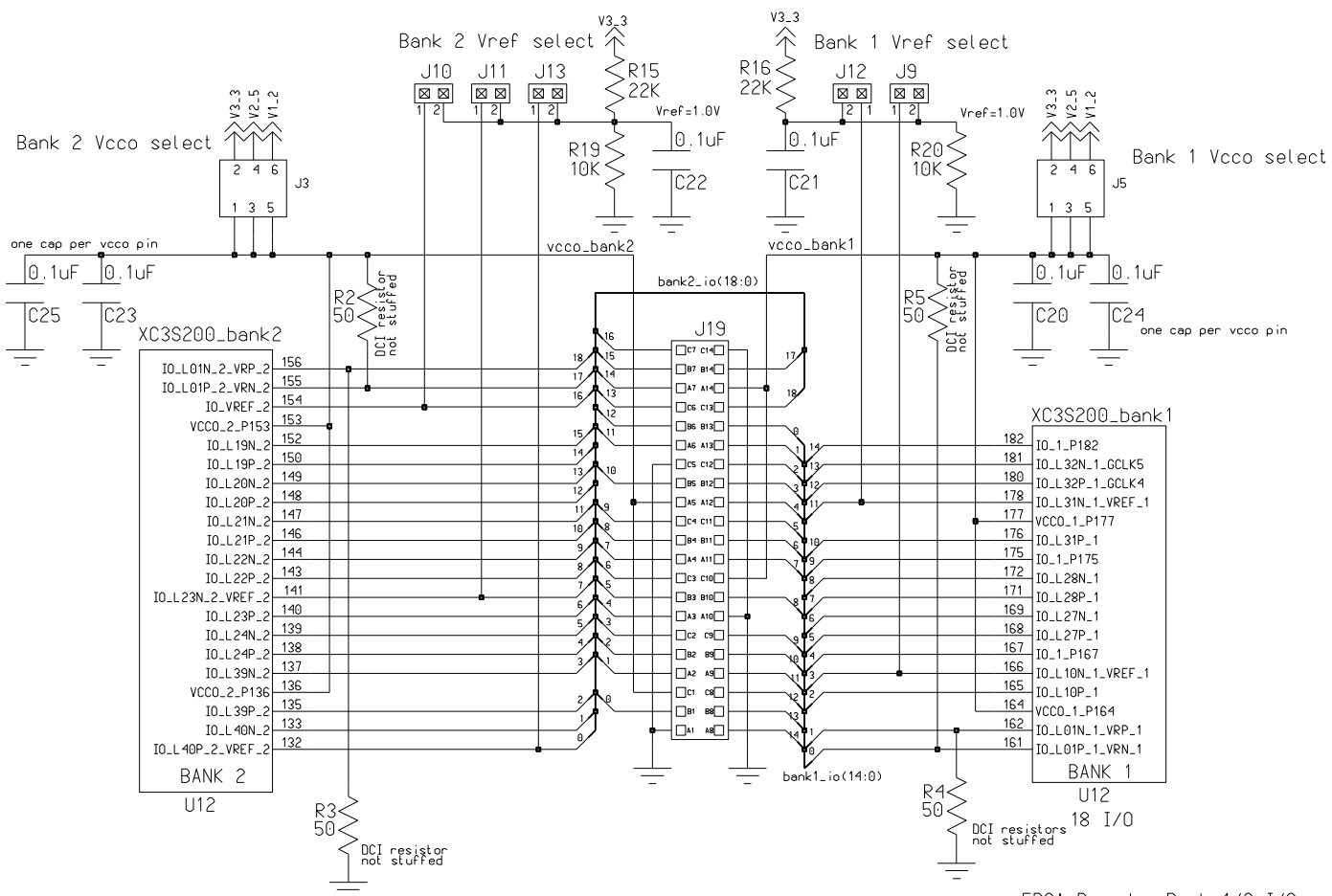


put decoupling caps directly under
via to device pin









XC3S200_bank2

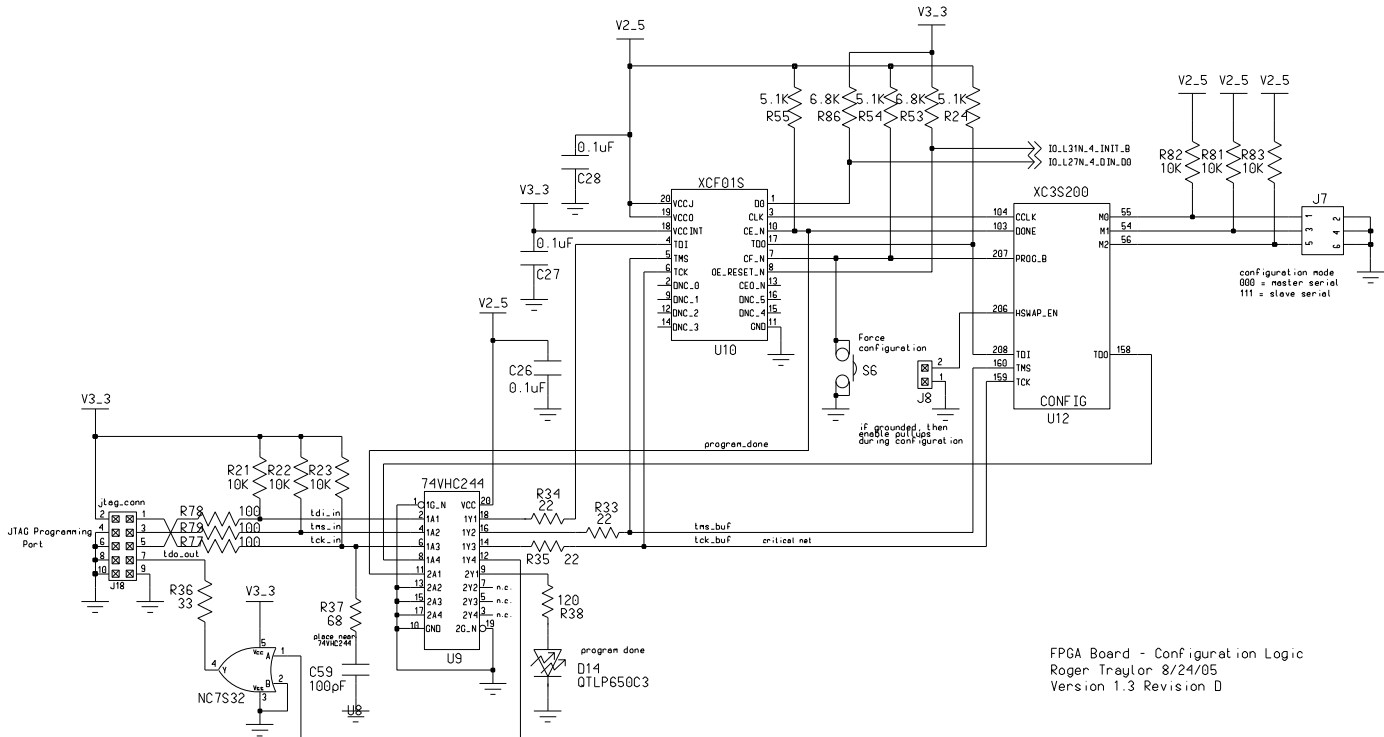
IO_L01N_2_VRP_2	156
IO_L01P_2_VRN_2	155
IO_VREF_2	154
VCC0_2_P153	153
IO_L19N_2	152
IO_L19P_2	150
IO_L20N_2	149
IO_L20P_2	148
IO_L21N_2	147
IO_L21P_2	146
IO_L22N_2	144
IO_L22P_2	143
IO_L23N_2_VREF_2	141
IO_L23P_2	140
IO_L24N_2	139
IO_L24P_2	138
IO_L39N_2	137
VCC0_2_P136	136
IO_L39P_2	135
IO_L40N_2	133
IO_L40P_2_VREF_2	132

BANK 2

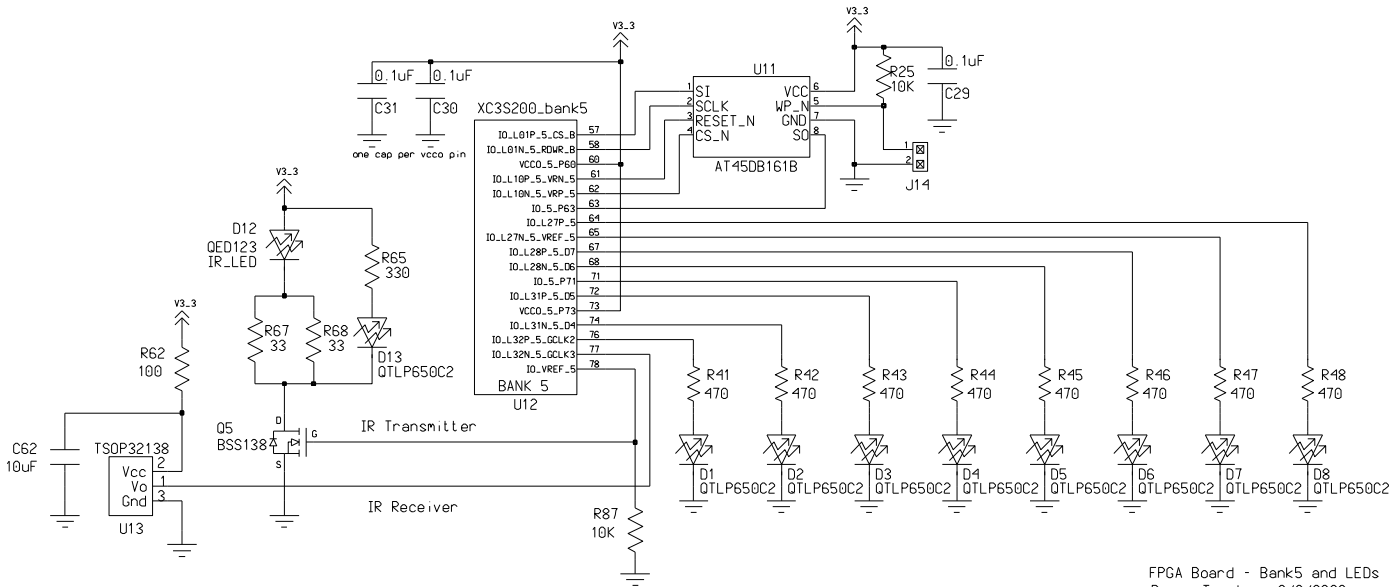
XC3S200_bank1

IO_1_P182	182
IO_L32N_1_GCLK5	181
IO_L32P_1_GCLK4	180
IO_L31N_1_VREF_1	178
VCC0_1_P177	177
IO_L31P_1	176
IO_1_P175	175
IO_L28N_1	172
IO_L28P_1	171
IO_L27N_1	169
IO_L27P_1	168
IO_L27P_1	167
IO_1_P167	166
IO_L10N_1_VREF_1	165
IO_L10P_1	164
VCC0_1_P164	164
IO_L01N_1_VRP_1	162
IO_L01P_1_VRN_1	161

BANK 1



FPGA Board - Configuration Logic
 Roger Traylor 8/24/05
 Version 1.3 Revision D



FPGA Board - Bank5 and LEDs
 Roger Traylor 8/2/2003
 Version 1.0 Revision D