Transparent thin-film transistors with zinc indium oxide channel layer

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High mobility, n-type transparent thin-film transistors (TTFTs) with a zinc indium oxide (ZIO) channel layer are reported. Such devices are highly transparent with ~85% optical transmission in the visible portion of the electromagnetic spectrum. ZIO TTFTs annealed at 600 °C operate in depletion-mode with threshold voltages ~20 to ~10 V and turn-on voltages ~3 V less than the threshold voltage. These devices have excellent drain current saturation, peak incremental channel mobilities of 45–55 cm² V⁻¹ s⁻¹, drain current on-to-off ratios of ~10⁶, and inverse subthreshold slopes of ~0.8 V/decade. In contrast, ZIO TTFTs annealed at 300 °C typically operate in enhancement-mode with threshold voltages of 0–10 V and turn-on voltages 1–2 V less than the threshold voltage. These 300 °C devices exhibit excellent drain–current saturation, peak incremental channel mobilities of 10–30 cm² V⁻¹ s⁻¹, drain current on-to-off ratios of ~10⁶, and inverse subthreshold slopes of ~0.3 V/decade. ZIO TTFTs with the channel layer deposited near room temperature are also demonstrated. X-ray diffraction analysis indicates the channel layers of ZIO TTFTs to be amorphous for annealing temperatures up to 500 °C and polycrystalline at 600 °C. Low temperature processed ZIO is an example of a class of high performance TTFT channel materials involving amorphous oxides composed of heavy-metal cations with (n–1)d¹⁰ns⁰ (n ≥ 4) electronic configurations.


I. INTRODUCTION

Amorphous zinc indium oxide (ZIO) is emerging as a commercially viable transparent conducting oxide because of its excellent optical transmission, high electrical conductivity, chemical stability, thermal stability, film smoothness, and low compressive stress. The purpose of the work reported herein is to demonstrate the utility of ZIO as a channel material for transparent thin-film transistor (TTFT) applications.

Most TTFTs reported to date have employed polycrystalline ZnO as a channel material. Recently, materials such as a single crystal InGaO₃(ZnO)₅ superlattice, polycrystalline SnO₂, and amorphous zinc tin oxide have emerged as alternative TTFT channel layer options. Zinc tin oxide and ZIO constitute two members of a class of TTFT channel materials involving amorphous oxides composed of heavy-metal cations with (n–1)d¹⁰ns⁰(n ≥ 4) electronic configurations.

II. EXPERIMENTAL TECHNIQUE

ZIO TTFTs are prepared on Nippon Electric Company glass substrates (NEG OA2) coated with a 200 nm sputtered indium tin oxide (ITO) gate electrode film and a 220 nm atomic layer deposited superlattice of Al₂O₃ and TiO₂ (ATO). The ITO and ATO layers constitute the gate contact and insulator, respectively, of a bottom-gate TTFT. The ZIO channel layer (typically ~85 nm) is deposited by rf sputtering, using a target purchased from Cerac, Inc. (ZnO:In₂O₃ molar ratio is 2:1). Three different process recipes are employed for the ZIO channel layer deposition, as specified in Table I. ITO (typically ~250 nm) source and drain electrodes are deposited via rf magnetron sputtering in Ar (100%). Both the ZIO channel and the ITO source and drain electrodes are deposited with no intentional heating of the substrate. After ITO source/drain deposition, devices are furnace annealed in air at either 300 or 600 °C for 1 hour; alternatively, the room temperature (RT) devices are not subjected to a post-deposition anneal. Six devices with W/L = 7100 μm/1500 μm (~4.7/1) are fabricated on each substrate.

Table I. rf sputtering and post-deposition annealing process parameters for the three types of zinc indium oxide channel layers used in the fabrication of transparent thin-film transistors. RT indicates room temperature, indicating that no intentional substrate heating or post-deposition annealing is employed.

<table>
<thead>
<tr>
<th>Anneal temperature (°C)</th>
<th>600</th>
<th>300</th>
<th>RT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ar gas flow (sccm⁻¹)</td>
<td>30</td>
<td>45</td>
<td>15</td>
</tr>
<tr>
<td>O₂ gas flow (sccm⁻¹)</td>
<td>3</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Target–substrate distance (cm)</td>
<td>7.5</td>
<td>7.5</td>
<td>10</td>
</tr>
<tr>
<td>Pressure (mTorr)</td>
<td>5</td>
<td>5</td>
<td>1–2</td>
</tr>
<tr>
<td>Power density (W cm⁻²)</td>
<td>2.5</td>
<td>2.5</td>
<td>4.9</td>
</tr>
</tbody>
</table>

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Power density (W cm⁻²)

Standard cubic centimeters per minute.
of all known phases in the ZnO–In₂O₃ system, but no phous precursor. The pattern has been compared with those corresponding to metal–oxygen interatomic distances. Clearly, at 600 °C the film has transformed into a crystalline form. In the patterns from the films produced from bulk reactions at temperatures above 500 °C, the broad peak near 32° is not simple to these phases can be made. This result may not be too surprising, as all of the known materials have been produced from bulk reactions at temperatures above 1000 °C. Based on x-ray data shown in Fig. 1 and the Scherrer equation, crystallite sizes for ZIO films are estimated to be smaller than 5 nm and 25–85 nm for films annealed below 500 and at 600 °C, respectively. Atomic force microscopy is used to confirm crystallite size of 600 °C-annealed films.

III. RESULTS AND DISCUSSION

A. Optical transmittance and x-ray diffraction

The optical transmittance through the channel region of a ZIO TTFT is shown in the inset of Fig. 1. The average transmittance in the visible portion of the electromagnetic spectrum (400–700 nm) is ~85%; this value represents raw transmission through the entire structure, including the substrate, i.e., the measured transmission is reduced by both absorption and reflection.

As seen in Fig. 1, x-ray data are consistent with amorphous (or nanocrystalline) films for annealing at temperatures as high as 500 °C. In the patterns from the films produced at RT and annealed at 500 °C the broad peak near 32° corresponds to scattering at dimensions representing metal–metal interatomic distances, while the peak near 58° corresponds to metal–oxygen interatomic distances. Clearly, at 600 °C the film has transformed into a crystalline form. There is no evidence in the pattern to indicate that separate phases as high as 5 nm and 25–85 nm for films annealed below 500 and at 600 °C, respectively. Atomic force microscopy is used to confirm crystallite size of 600 °C-annealed films.

B. Current–voltage characteristics

Figure 2 illustrates the drain current, drain-to-source voltage (I_D–V_DS) curves of a TTFT in which the ZIO channel layer is subjected to a 600 °C post-deposition furnace anneal; these curves exhibit qualitatively ideal transistor characteristics. Note that this device operates in depletion-mode, i.e., appreciable drain current flows at zero gate voltage, as evident from the V_GS=0 V drain current shown in Fig. 2.

Figure 3 shows I_D–V_DS curves of a TTFT in which the ZIO channel layer is subjected to a 300 °C post-deposition furnace anneal. The curves shown in Fig. 3 exhibit qualitatively ideal transistor characteristics. In contrast to the device subjected to a 600 °C anneal, this device operates in enhancement-mode, i.e., appreciable drain current flows at zero gate voltage; a positive gate voltage is required to turn on the drain current, as evident from the fact that V_GS for this figure decreases from +20 V (top curve, showing maximum current) to 0 V in 2 V steps. I_D decreases to a negligible value on the scale used in Fig. 3 for V_GS<+8 V. Additionally, the decreasing separation between I_D curves at larger currents witnessed in the I_D–V_DS characteristic shown in Fig.
3 is a non-ideal effect. This “crowded” characteristic is attributed to either an electron injection barrier at the source electrode or to mobility degradation associated with the increasing effect of interface roughness scattering as channel electrons are brought into closer physical proximity to the channel/insulator interface with increasing $V_{GS}$.27

Figure 4 shows a comparison between the log($I_D$)–$V_{GS}$ characteristics (at $V_{GS}$=20 V) of ZIO TTFTs annealed at 600 and 300 °C. The depletion- and enhancement-mode nature of devices processed at 600 and 300 °C, respectively, is clearly evident from this figure. The high temperature 600 °C processed device is depletion-mode with a turn-on voltage of −12 V, a threshold voltage (extracted from linear extrapolation of an $I_D$–$V_{GS}$ curve) of −9 V, a drain current on-to-off ratio of $\sim 10^6$, and an inverse subthreshold slope of 0.8 V/decade. Similar values for the low temperature 300 °C processed enhancement-mode device are $+6$ V, $+7$ V, $-10^6$, and 0.3 V/decade, respectively.

The charge density in the channel layer, $N_T$, corresponding to the turn-on voltage, $V_{on}$, is estimated as

$$N_T = \frac{C_t V_{on}}{q t_c},$$

where $C_t$ is the gate insulator capacitance per unit area, $q$ is the elementary charge, and $t_c$ is the thickness of the channel layer. For the TTFTs employed, $C_t$=60 nF cm$^{-2}$ and $t_c$ =85 nm, so that $N_T$=−7.1×10$^{17}$ cm$^{-3}$ for the depletion-mode TTFT with $V_T$=−9 V, and $N_T$=+3.2×10$^{17}$ cm$^{-3}$ for the enhancement-mode TTFT with $V_T$=+7 V. The negative charge responsible for the negative threshold voltage of the depletion-mode device is ascribed to delocalized electrons from shallow donors in the channel, which must be depleted from the channel layer by a negative gate voltage in order to turn off the TTFT drain current. The positive charge responsible for the positive threshold voltage of the enhancement-mode device is attributed to deep traps in the channel or at the interface, which must be filled by electrons injected from the source electrode into the channel under the application of a positive gate voltage, which confines these injected electrons to a near-interface accumulation layer.

### C. Mobility assessment

A channel mobility comparison of ZIO TTFTs annealed at 600 and 300 °C is provided in Fig. 5. Two types of channel mobility are included in this figure, average mobility ($\mu_{avg}$) and incremental mobility ($\mu_{inc}$). These types of channel mobility are derived from the basic charge transport model without neglecting the gate voltage dependence of channel mobility.14 For this reason, $\mu_{avg}$ and $\mu_{inc}$ are preferred to the more commonly known effective and field-effect mobilities,27 which are based on extractions from the ideal metal–oxide–semiconductor field effect transistor equation.

Consider the mobility characteristics shown in Fig. 5. First, note that the maximum mobilities of the ZIO TTFT processed at 600 °C are higher than those of the device processed at 300 °C. X-ray diffraction (XRD) analysis suggests that the higher mobility of the ZIO TTFT processed at 600 °C may be associated with increased crystallinity. Additionally, the mobility difference may be a result of decreased defect density at the interface and/or in the bulk. Nonetheless, the magnitude of the channel mobility difference between polycrystalline and amorphous ZIO is rather small compared to polycrystalline and amorphous Si. This is attributed to a conduction band derived primarily from spherical s orbitals rather than anisotropic p or d orbitals.18–21

Next, consider the $\mu_{inc}$–$V_{GS}$ curve shown in Fig. 5(a) for the TTFT annealed at 600 °C. At $V_{GS}$ values above a threshold voltage of $\sim$−11 V, $\mu_{inc}$ increases to a peak mobility of 53 cm$^2$ V$^{-1}$ s$^{-1}$ and then decreases. The initial rise in mobility corresponds to initiation of electron injection from the source electrode into the channel. The very first electrons injected into the channel are trapped in bulk and/or interface traps. As these trap states fill, a higher percentage of the injected channel electrons are free to drift, to the drain electrode, thereby resulting in an increase in $\mu_{inc}$.

The $\mu_{inc}$–$V_{GS}$ curve shown in Fig. 5(a) decreases at larger $V_{GS}$ values as a consequence of either an electron in-
ijection barrier at the source electrode or due to mobility degradation associated with channel/insulator interface roughness scattering, as discussed in the context of Fig. 3. More work is required to conclusively establish the relative contributions of the source electrode injection barrier and interface scattering to the mobility reduction seen in Fig. 5. In any event, it is clear from a comparison of Figs. 5(a) and 5(b) that the mobility decrease with increasing gate voltage is much more pronounced (for the $V_{GS}$ range shown) for the device processed at 300 °C. This is also evident from the fact that the separation between $I_D$ curves at larger currents decreases appreciably with increasing $V_{GS}$ in the saturation region for Fig. 3 but not for Fig. 2.

Now compare $\mu_{inc}$ and $\mu_{avg}$ characteristics shown in Fig. 5; considering the origin of both mobilities helps illustrate the observed differences. Both $\mu_{inc}$ and $\mu_{avg}$ are estimated from the linear (or triode) region of $I_D$–$V_{DS}$ characteristics. However, $\mu_{inc}$ is extracted from the differential channel conductance with respect to gate voltage while $\mu_{avg}$ is extracted from the channel conductance. Thus, $\mu_{inc}$ corresponds to the incremental mobility of induced channel charge as it is gradually added to the channel with increasing $V_{GS}$. This corresponds to the previously discussed physical description of the $\mu_{inc}$–$V_{GS}$ trend in which the rising portion of the curve corresponds to incremental trap filling and the decreasing portion of the curve corresponds to either source injection-limited behavior or interface roughness scattering. In contrast, $\mu_{avg}$ corresponds to the average mobility of all induced charge in the channel at a given $V_{GS}$. For these reasons, $\mu_{inc}$ is the mobility of greater physical significance. In contrast, $\mu_{avg}$ is the mobility of greater practical significance, i.e., $\mu_{avg}$ is more directly related to actual device and circuit performance, and is thus the more important application-related figure-of-merit.

In summary, ZIO depletion-mode TTFTs processed using an annealing temperature of 600 °C have peak incremental mobilities of 45–55 cm$^2$ V$^{-1}$ s$^{-1}$ and maximum average mobilities of 25–35 cm$^2$ V$^{-1}$ s$^{-1}$. Similarly, ZIO enhancement-mode TTFTs processed using an annealing temperature of 300 °C have peak incremental mobilities of 10–30 cm$^2$ V$^{-1}$ s$^{-1}$ and maximum average mobilities of 5–20 cm$^2$ V$^{-1}$ s$^{-1}$. Both types of devices exhibit a decrease in mobility at large $V_{GS}$, possibly due to an electron injection barrier at the source electrode or interface roughness scattering.

These estimated channel mobilities of our ZIO TTFTs compare to incremental mobilities of ~25 cm$^2$ V$^{-1}$ s$^{-1}$ for the best polycrystalline ZnO TTFT reported to date,14 ~80 cm$^2$ V$^{-1}$ s$^{-1}$ for an engineered superlattice single-crystal TTFT prepared by pulsed laser deposition and a high-temperature anneal of 1400 °C,16 and 5–15 and 20–50 cm$^2$ V$^{-1}$ s$^{-1}$ for zinc tin oxide TTFTs annealed at 300 and 600 °C, respectively.18

D. Room temperature ZIO TTFTs

ZnO TTFTs and TTFTs have recently been reported in which the ZnO channel layer is deposited by rf sputtering at near room temperature, i.e., with no intentional substrate heating or post-deposition annealing.0,15 We have successfully fabricated ZIO TTFTs using this same basic procedure. The channel layer deposition process recipe employed for these near room temperature ZIO TTFTs is specified in Table I. As evident from Table I, our near room temperature process recipe differs from that of the other two process recipes in that the oxygen flow rate, the target–substrate distance, and the power density are all larger, while the pressure is lower.

Figure 6 illustrates the $I_D$–$V_{GS}$ curves of a TTFT in which the ZIO channel layer is deposited by rf sputtering near room temperature and is not subjected to a post-deposition anneal. This device operates in enhancement-mode, as evident from the fact that $V_{GS}$ for this figure decreases from 10 V (top curve, showing maximum current) to 0 V in 1 V steps. $I_D$ decreases to a negligible value on the scale used in Fig. 6 for $V_{GS} < 6$ V. Our best ZIO TTFT results to date demonstrate a peak incremental mobility of 8 cm$^2$ V$^{-1}$ s$^{-1}$ (17 cm$^2$ V$^{-1}$ s$^{-1}$) and a drain current on-to-off ratio of 10$^4$ (3 × 10$^3$) for enhancement-mode (depletion-mode) operation.

IV. CONCLUSIONS

Zinc indium oxide (ZIO) is demonstrated as a high mobility, n-type TTFT channel material. ZIO is found to be amorphous for post-deposition annealing temperatures up to at least 500 °C and polycrystalline at 600 °C. Thus, low temperature processed ZIO is an example of a class of high performance TTFT channel materials involving amorphous oxides composed of heavy-metal cations with $(n-1)d^{10}ns^3$ $(n \geq 4)$ electronic configurations. Although mobility is higher for ZIO TTFTs with a polycrystalline channel layer, the enhancement-mode nature, smoother surface texture, and lower processing temperature of an amorphous channel layer favors its use in future transparent or flexible electronics applications.

ACKNOWLEDGMENTS

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![Fig. 6. Drain current–drain voltage ($I_D$–$V_{DS}$) characteristics of a TTFT in which the ZIO channel layer is not subjected to a post-deposition anneal. $V_{GS}$ is decreased from 10 V (top curve, showing maximum current) to 0 V in 1 V steps. This TTFT is enhancement-mode.](image-url)
22. TTO/ATO glass is supplied by Arto Pakkala, Planar Systems, Inc. Espoo, Finland (arto_pakkala@planar.com).

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