20.2: SPICE Modeling of Dynamic Space Charge in ACTFEL Devices

P. D. Keir, J. F. Wager
Oregon State University, Corvallis, OR

Abstract

Simulation of dynamic phosphor space charge in alternating-current thin-film electroluminescent (ACTFEL) devices is performed using SPICE equivalent circuit models. Two SPICE equivalent circuits are developed; one for the case of space charge creation via impact ionization and another for field emission. Both SPICE equivalent circuits are based on modeling the space charge distribution as a single sheet of charge. Simulation results show that both SPICE equivalent circuits are capable of generating electrical characteristics exhibiting capacitance overshoot.

Introduction

The increased interest in alternating-current thin-film electroluminescent (ACTFEL) phosphor materials and deposition techniques other than the traditional evaporated ZnS:Mn phosphor has turned the issue of phosphor space charge from a novelty to a very relevant topic. With evaporated ZnS:Mn ACTFEL devices traditionally used for monochrome electroluminescent displays, there is very little evidence for the existence of dynamic phosphor space charge (space charge creation and annihilation in the phosphor layer during device operation). However, in phosphors such as atomic layer epitaxy (ALE) deposited ZnS:Mn [1,2] and SrS:Ce [3,4], there is significant evidence suggesting that dynamic space charge plays a major role in determining the operation of these devices. One of the major issues in relation to the space charge effect seen in these devices is an apparent increased power consumption resulting from a dynamic space charge induced increase in the device "on" capacitance over the physically expected value.

Much of the current research aimed at development of a full-color ACTFEL display panel is based on the use of SrS:Ce as the electroluminescent phosphor. Research is focusing on SrS:Ce as a candidate phosphor for color electroluminescent applications because blue/green emitting samples of high brightness and efficiency have been demonstrated. However, one of the major drawbacks of using SrS:Ce as a phosphor for production displays is that it often exhibits a much larger "on" capacitance than would be expected from the physical capacitances of the insulating layers [3]. Since larger device capacitance means greater power consumption, a full-color display based on the SrS:Ce phosphor will potentially consume substantially more power than a similarly sized monochrome display.

The larger than expected "on" capacitance of SrS:Ce devices seems to be a byproduct of space charge generation in the phosphor layer of the device [3]. It should be noted that throughout the remainder of this article, space charge generation in the phosphor layer is termed dynamic space charge because of its time dependent nature. Several published articles have demonstrated simulation results linking dynamic space charge to anomalous electrical effects such as capacitance overshoot [5,6,7,8]. However, since the previous work involving simulation of dynamic space charge effects was performed using device physics based models and custom programming, they are not amenable to simulation of finished products, such as panels which contain many devices. An improved method for simulation of several devices is SPICE in which it is fairly painless to add additional devices once the first device works properly. Therefore, the purpose of the work described herein is the translation of the device physics based models that include dynamic space charge to a SPICE platform to demonstrate capacitance overshoot with SPICE.

Dynamic space charge SPICE models

The SPICE equivalent circuit models of dynamic space charge are analogs of the single sheet charge dynamic space charge models presented in [5]. The single sheet charge model is chosen as a starting point for the development of SPICE equivalent circuits because its simple nature makes it amenable to SPICE modeling. As discussed in [5], space charge generation in the phosphor is attributed to two different mechanisms, field emission and impact ionization. Since the physical nature of these two processes of creating dynamic space charge are quite different, it is necessary to generate an equivalent circuit for both cases.

If it is assumed that dynamic space charge is due to field emission of carriers from bulk traps in the phosphor, the equivalent circuit model of Fig. 1 is the relevant SPICE model. Several clarifications need to be made with regard to the field emission SPICE equivalent circuit shown in Fig. 1. First, the capacitors c_{p1} and c_{p2} represent the phosphor capacitance of the portion of the phosphor layer lying on either side of the assumed location of the space charge layer. The difference in the values of these two capacitors determines the amount of asymmetry in the electrical characteristics. Next, the current sources $J_1(v_{p2})$ and $J_2(v_{p1})$ represent the emission of carriers from the semiconductor-insulator interfaces of the ACTFEL device. Then, the current sources $J_{sc}(v_{p1})$ and $J_{sc}(v_{p2})$ represent the emission of carriers from the bulk phosphor sheet charge layer. Finally, the current sources $J_1^{leak}(v_{p1})$ and J_2^{leak} (v_{p2}) represent the annihilation of space charge by the trapping of interface-emitted carriers. Due to the dependence of these currents on the polarity of the applied voltage pulse,

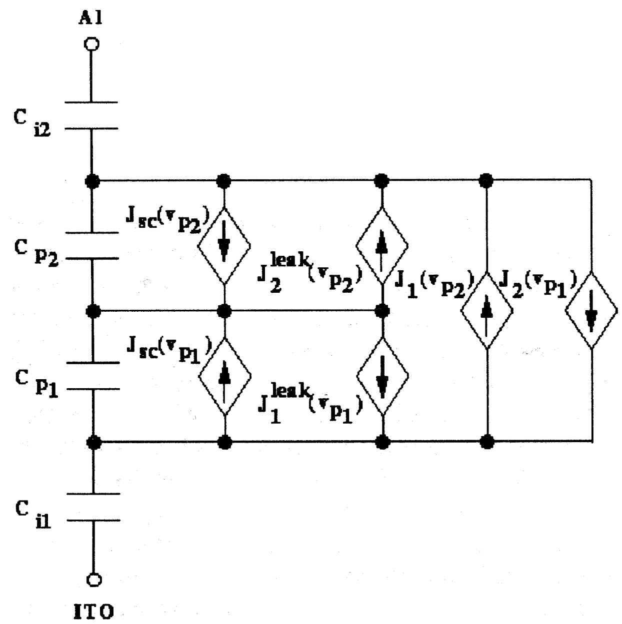

Fig. 1. Field emission SPICE equivalent circuit.

each of the current sources is active for only one polarity of the relevant phosphor field.

When it is assumed that dynamic space charge is due to impact ionization (either impact ionization of traps or trapping of holes generated by band-to-band impact ionization), the circuit of Fig. 2 applies. The only difference between the equivalent circuits shown in Figs. 1 and 2 are the circuit branches representing the creation of space charge. In the circuit of Fig. 2, it is seen that the circuit branches representing space charge generation are now composed of a current source that mirrors the carrier emission from the interface in series with an amplifier whose gain is dependent on the voltages across each portion of the phosphor. This modification is required because impact ionization is dependent on both the number of carriers arising from normal interface conduction and the field in the phosphor, whereas field emission is dependent solely on the phosphor field.

Several additional comments need to be made regarding the equivalent circuits of Figs. 1 and 2. First, for simulation of these circuit, the interface current is generally modeled as a discrete Dirac well of user-definable depth, as in [9]. Finally, it should be noted that it is possible to include carrier multiplication by

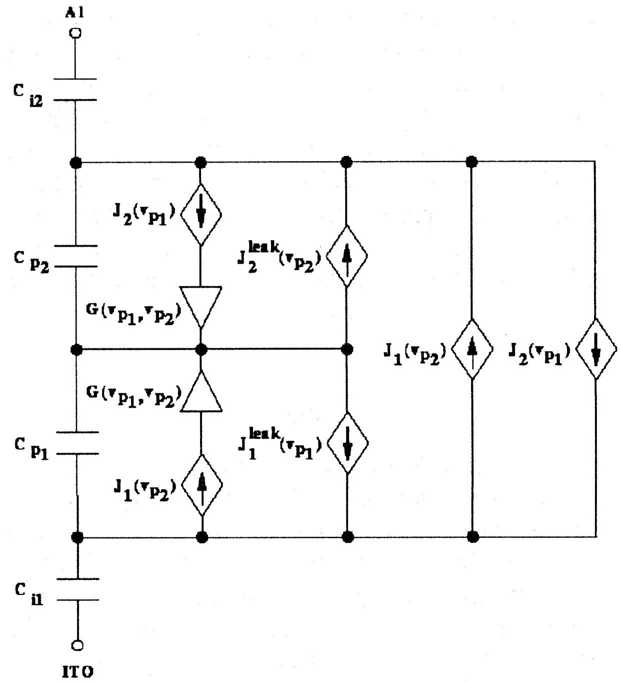

Fig. 2. Impact ionization SPICE equivalent circuit.

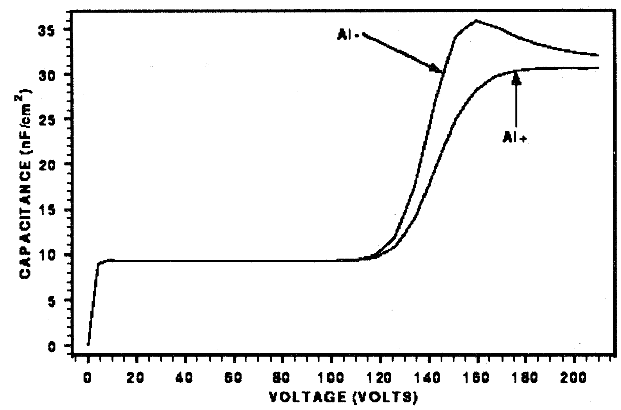

Fig. 3. C-V plot resulting from simulation of the field emission SPICE equivalent circuit.

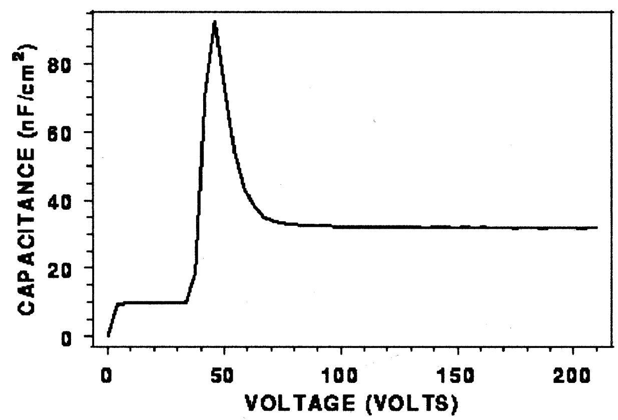

Fig. 4. C-V plot resulting from simulation of the impact ionization SPICE equivalent circuit.

band-to-band impact ionization in these SPICE models by adding an amplifier in series with the current source that is the source of the carriers that are subsequently multiplied. The gain of these amplifiers is defined similar to the amplifiers in the impact ionization model of Fig. 2 in that they are dependent on the voltage across each portion of the phosphor layer.

Results

The results of simulation of the SPICE equivalent circuits of Figs. 1 and 2 are shown in the capacitance-voltage (C-V) plots of Figs. 3 and 4, respectively. The results of both simulations show that capacitances in excess of the expected insulator capacitance (or “on” capacitance) can be generated using the equivalent circuit models shown in Figs. 1 and 2. As seen in Figs. 1 and 2, there is a much larger overshoot in the case of impact ionization. This seems to be a general trend; it is possible to produce much greater overshoot for the same phosphor trap densities with impact ionization because of the extremely strong dependence of the ionization rate on the phosphor field.

Another interesting feature of these results is seen through comparison of the turn-on voltages of the devices shown in Figs. 3 and 4. The device of Fig. 3 turns on at about 140 volts, whereas the device of Fig. 4 turns on at about 40 volts. Generally ACTFEL devices of typical phosphor thicknesses ($\sim$500nm) turn on at or above 100 volts. Note that the C-V curve of Fig. 3 shows a realistic turn-on voltage, whereas the C-V curve of Fig. 4 shows a very low turn-on voltage. This difference in turn-on voltage arises from differences in how the leakage charge is modeled in these two devices. Leakage charge is the charge which flows during the interpulse interval (*i.e.* when the applied voltage is zero) and arises from the emission of electrons in interface states [1]; an increase in leakage charge causes a reduction in the polarization charge and a concomitant increase in the turn-on voltage. Leakage charge is accounted for in Fig. 3 by the inclusion of thermal emission from the discrete interface state; since leakage charge is taken into consideration in this simulation, the turn-on voltage is in reasonable agreement with that measured experimentally. In contrast, leakage charge is not modeled in Fig. 4 (only tunneling from a discrete Dirac well is used to model interface state emission), so that the turn-on voltage is unrealistically small. (Leakage charge could have been modeled in Fig. 4, however, it was intentionally omitted so that the preceding turn-on voltage/leakage charge issues could be discussed).

As a final note, there are two primary ways to account for leakage charge in ACTFEL device-physics based simulations. First, the emission rate of the interface trap may be modified via the inclusion of thermal emission and/or phonon-assisted tunneling. Second, the trap distribution may be modified so that multiple traps or a distributed trap density is assumed. More realistic leakage charge trends may be simulated using either or both of these approaches. However, accurate modeling of leakage charge significantly increases the complexity of the simulation; furthermore, most of these simulation approaches are not SPICE-implementable. Leakage charge modeling is a topic of ongoing research in our research group.

Conclusions

The SPICE models presented herein give results that exhibit C-V overshoot. Two models of space charge generation are required to model space charge depending on whether space charge creation proceeds via impact ionization or field emission. Initial attempts to model turn-on voltage/leakage charge trends have been attempted, but further work is required to accomplish accurate simulation of these trends. Once this is accomplished, such models may lead to a better way to estimate the power consumption of an ACTFEL panel.

Acknowledgments

This work was supported by the U.S. Army Research Office under Contract No. DAAH04-94-G-0324 and by the Advanced Research Projects Agency under the Phosphor Technology Center of Excellence, Grant No. MDA 972-93-1-0030.

References

[1] A. Abu-Dayah, S. Kobayashi, and J. F. Wager, *Appl. Phys. Lett.*, **62**(7), 744 (1993).

[2] A. Abu-Dayah and J. F. Wager, *J. Appl. Phys.*, **75**(7), 3593 (1994).

[3] S. Shih, P. D. Keir, and J. F. Wager, *J. Appl. Phys.*, **78**(9), 5775 (1995).

[4] K. Ohmi, K. Ishitani, S. Tanaka, and H. Kobayashi, *Appl. Phys. Lett.*, **67**(7), 944 (1995).

[5] P. D. Keir, W. M. Ang, and J. F. Wager, *J. Appl. Phys.*, **78**(7). 4668 (1995).

[6] W. E. Howard, O. Sahni, and P. M. Alt, *J. Appl. Phys.*, **53**, 639 (1982).

[7] J. M. Jaren and V. P. Singh, *IEEE Trans. Electron Devices*, **ED-35**, 1834 (1988).

[8] K. A. Neyts, D. Corlatan, P. de Visschere, and J. van den Bossche, *J. Appl. Phys.*, **75**, 5339 (1994).

[9] G. Vincent, A. Chantre, and D. Bois, *J. Appl. Phys.*, **50**, 5484 (1979).