3. Figure 1 shows an NMOS inverter with resistive load.
   a. Qualitatively discuss why this circuit behaves as an inverter.
   b. Find $V_{OH}$ and $V_{OL}$ calculate $V_{IH}$ and $V_{IL}$.
   c. Find $NM_L$ and $NM_H$.
   d. Compute the average power dissipation for: (i) $V_{in} = 0V$ and (ii) $V_{in} = 2.5V$.
   e. Use HSPICE to sketch the VTCs for $R_L = 37k$, 75k, and 150k on a single graph.
   f. Comment on the relationship between the critical VTC voltages (i.e., $V_{OL}$, $V_{OH}$, $V_{IL}$, $V_{IH}$) and the load resistance, $R_L$.
   g. Do high or low impedance loads seem to produce more ideal inverter characteristics?

![Figure 1: Resistive-load inverter.](image)

5. The next figure shows two implementations of MOS inverters. The first inverter uses only NMOS transistors.
   a. Calculate $V_{OH}$, $V_{OL}$, $V_M$ for each case in figure 2.

![Figure 2: Inverter Implementations.](image)

   b. Use HSPICE to obtain the two VTCs. You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, $\lambda = 0.125 \mu m$, and the source/drain extensions are $5\lambda \times 5\lambda$.
   c. Find $V_{IH}$, $V_{IL}$, $NM_L$ and $NM_H$ for each inverter and comment on the results. How can you increase the noise margins and reduce the undefined region?
   d. Comment on the differences in the VTCs, robustness and regeneration of each inverter.

8. An NMOS transistor is used to charge a large capacitor, as shown in figure 3.
   a. Determine the $t_{pLH}$ of this circuit, assuming an ideal step from 0 to 2.5V at the input node.
   b. Assume that a resistor $R_S$ of 5 k$\Omega$ is used to discharge the capacitance to ground. Determine $t_{pHL}$.
c. Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in $M_1$. How much is dissipated in the pull-down resistance during discharge? How does this change when $R_S$ is reduced to 1 kΩ?

d. The NMOS transistor is replaced by a PMOS device, sized so that $k_p$ is equal to the $k_n$ of the original NMOS. Will the resulting structure be faster? Explain why or why not.

![Figure 3: Circuit diagram with annotated W/L ratios.](image1)

12. Consider the low swing driver of figure 4:

![Figure 4: Low Swing Driver.](image2)

a. What is the voltage swing on the output node ($V_{out}$)? Assume $\gamma=0$.

b. Estimate (i) the energy drawn from the supply and (ii) energy dissipated for a 0V to 2.5V transition at the input. Assume that the rise and fall times at the input are 0. Repeat the analysis for a 2.5V to 0V transition at the input.

c. Compute $t_{pLH}$ (i.e. the time to transition from $V_{OL}$ to $\frac{V_{OH}+V_{OL}}{2}$). Assume the input rise time to be 0. $V_{OL}$ is the output voltage with the input at 0V and $V_{OH}$ is the output voltage with the input at 2.5V.

d. Compute $V_{OH}$ taking into account body effect. Assume $\gamma = 0.5V^2$ for both NMOS and PMOS.

15. Sizing a chain of inverters.

a. In order to drive a large capacitance ($C_L = 20pF$) from a minimum size gate (with input capacitance $C_i = 10fF$), you decide to introduce a two-staged buffer as shown in figure 5. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.
b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

c. Describe the advantages and disadvantages of the methods shown in (a) and (b).

d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?

16. Consider scaling a CMOS technology by $S > 1$. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a. In traditional constant voltage scaling, transistor widths scale inversely with $S$, $W \propto 1/S$. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for $W$. What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation).

b. How does delay scale under this new methodology?

c. Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?