13. The two cases are shown in figure 1.

![Pass Gate Implementation](image1)

**Figure 1: Implementation of problem 13.**

15. 

a. The circuit implements an XNOR. The truth table can be seen in table 1.

<table>
<thead>
<tr>
<th>AB</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1: Truth table of XNOR.

b. The PMOS device will be velocity saturated and the NMOS passgate will be in the linear region. $I_{DN} + I_{DP} = 0$, so

$$k'_p \frac{W}{L} V_{DSAT}(V_{GT} - 0.5V_{DSAT})(1 + \lambda V_{DS}) + k'_n \frac{W}{L} V_o(V_{GT} - 0.5V_o)(1 + \lambda V_o) = 0$$

We know that $V_o = 0.3V$, so we can plug in numbers and solve for W/L for the PMOS is 7. Let the PMOS be 1.75/0.25.

c. No. If the PMOS were removed, the output node could remain low when AB=00 because it would be floating. The PMOS device pulls the output node high when it would otherwise be in a high impedance state.
18.

a. The circuit is a NAND gate.

b. When $A = B = V_{DD}$, the voltage at node $x$ is $V_X = V_{DD} - V_{tN}$. This causes static power dissipation at the inverter the pass transistor network is driving.

c. The modified circuit is shown in figure 2. The size of $M_r$ should be chosen so that when one of the inputs $A$ or $B$ equals 0, either $M_{n1}$ or $M_{n2}$, would be able to pull node $X$ to $V_{DD}/2$ or less.

d. The circuit is shown in figure 3.

e. One possible implementation is in figure 4.
25.

a. See figure 5.

![Figure 5: Solution to 25 a.](image)

b. The circuit implements $Out = A + BC$. It is in the pseudo NMOS family.

c. The circuit uses less area than a fully complementary CMOS implementation.

d. $V_{OH} = V_{DD} = 2.5V$. To find $V_{OL}$, assume that we can combine $M_B$ and $M_C$ into one NMOS with $W/L = 0.75/0.25$. Then the worst case $V_{OL}$ occurs when $A = 0$ and the combined BC NMOS is on. Assume that $V_{OL}$ is less than $V_{DSAT}$. Then the NMOS device is in the linear region. The PMOS device will be velocity saturated. Equating the currents at the output gives:

$$k'_p \frac{W}{L} V_{DSAT} (V_{GT} - 0.5 V_{DSAT}) (1 - \lambda V_{DS}) + k'_n \frac{W}{L} V_{o} (V_{GT} - 0.5 V_{o}) (1 - \lambda V_{o}) = 0$$

The only unknown in this 3rd order polynomial is $V_o$. Solving for $V_o$ gives $V_{OL} = 51.2mV$

e. Call the PMOS device $P$, and name the other devices by their input signal.

- $AD_P = AS_P = 19\lambda^2$.
- $PD_P = PS_P = 15\lambda$.
- $AS_A = 40\lambda^2$.
- $PS_A = 18\lambda$.
- $AD_A = (3x8 + 3x12)\lambda^2/2 = 30\lambda^2$.
- $PD_A = 16\lambda^2/2 = 8\lambda$. $AD_B = AD_A \cdot PD_B = PD_A$.
- $AS_B = 36\lambda^2/2 = 18\lambda^2$. $PS_B = 6\lambda^2/2 = 3\lambda$.
- $AD_C = AS_B \cdot PD_C = PS_C$.
- $AS_C = 60\lambda^2$. $PS_C = 22\lambda$.

We can narrow the number of transitions to look at for determining the worst case $t_{pHL}$. The worst case capacitance occurs when the internal node between $M_B$ and $M_C$ is charged up to $V_{DD}$. Then the worst case delay will occur when either $M_A$ or the $M_B, M_C$ pair discharges this capacitance. If the series devices are doing the discharging, we need to consider the case where $M_B$ is initially on and where $M_B$ is initially off.

The simulation shows that the worst-case transition occurs over three cycles: ABC = 010 to 000 to 011 produces the worst-case $t_{pHL}$. This is worse than when $M_A$ discharges the node (ABC = 010 to 110) or when $M_B$ is initially on (ABC = 010 to 011).

We could calculate $t_{pHL}$ using either the equivalent resistance method or the average current method. In either case, $C_L$ would include the following parasitic capacitances:

$$C_{GDPMOS} + C_{DBPMOS} + C_{GDA} (no \ Miller \ effect \ because \ input \ not \ changing) + C_{DBA} + C_{GDB} + C_{DBB} + C_{GSB} + C_{GDC} + C_{DBC}.$$
29.

a. $A(B + C)$

b. When the output is high, the worst-case leakage occurs when two transistors leak in parallel: $ABC = 100$. When the output is low, the worst-case leakage also occurs when two transistors leak in parallel: $ABC = 110$ or $ABC = 101$.

c. 

\[
\begin{align*}
    d \times P_{\text{active}} &= (1 - d)P_{\text{leakage}} \cdot P_{\text{active}} \\
    &= \alpha_{0 \rightarrow 1} f C_L V_{DD}^2 \\
    &= (3/8 \times 5/8) (100 \times 10^6) (50 \times 10^{-15}) (2.5^2) \\
    &= 7.3 \mu W
\end{align*}
\]

\[
P_{\text{leakage}}(ABC = 100) = 2V_{DD}I_{\text{leakM1}}
\]

\[
\begin{align*}
    &= 5I_o 10^{-\frac{V_T}{8}} \\
    &= 5 \times 1 \mu A \times 10^{-\frac{0.43}{8}} \\
    &= 251 \text{pW}
\end{align*}
\]

Plugging the power numbers into the activity equation and solving for $d$ gives,

\[
d = 3.4 \times 10^{-8}
\]