13. Implement the function \( S = ABC + \overline{A}BC + \overline{A}BC + \overline{A}B \overline{C} \), which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume \( A, B, C \), and their complements are available as inputs.

15. Figure 1 contains a pass-gate logic network.

   a. Determine the truth table for the circuit. What logic function does it implement?
   b. Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a \( V_{OL} = 0.3 \) V.
   c. If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?

![Figure 1: Pass-gate network.](image)

18. Pass Transistor Logic.

   ![Figure 2: Level restoring circuit.](image)

   Consider the circuit of figure 2. Assume the inverter switches ideally at \( V_{DD}/2 \), neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

   a. What is the logic function performed by this circuit?
   b. Explain why this circuit has non-zero static dissipation.
   c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.
   d. Implement the same circuit using transmission gates.
   e. Replace the pass-transistor network in figure 2 with a pass transistor network that computes the following function: \( x = ABC \) at the node \( x \). Assume you have the true and complementary versions of the three inputs \( A, B \) and \( C \).

25. For this problem, refer to the layout of figure 3.

   a. Draw the schematic corresponding to the layout. Include transistor sizes.
   b. What logic function does the circuit implement? To which logic family does the circuit belong?
c. Does the circuit have any advantages over fully complementary CMOS?

d. Calculate the worst-case $V_{OL}$ and $V_{OH}$.

e. Write the expressions for the area and perimeter of the drain and source for all of the FETs in terms of $\lambda$. Assume that the capacitance of shared diffusion's divides evenly between the sharing devices. Copy the layout into Magic, extract and simulate to find the worst-case $t_{PHL}$ time. For what input transition(s) does this occur? Name all of the parasitic capacitances that you would need to know to calculate this delay by hand (you do not need to perform the calculation).

29. Consider the circuit shown figure 4.

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5$\mu$m / 0.25$\mu$m.

b. Let the drain current for each device (NMOS and PMOS) be 1$\mu$A for NMOS at $V_{GS} = V_T$ and PMOS at $V_{SG} = V_T$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL.

c. Suppose the circuit is active for a fraction of time $d$ and idle for $(1-d)$. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr(A=1) = 0.5$, $Pr(B=1) = 0.5$, $Pr(C=1) = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle $d$ for which the active power is equal to the leakage power?

![Figure 3: Layout of complex gate.](image)

![Figure 4: CMOS logic gate.](image)