1. The circuit and paths of interest has been reproduced for convenience in figure 1.

![Sequential circuit diagram](image)

Figure 1: Sequential circuit.

Out of the four paths shown in the figure, p1 is the critical one and determines the lower bound on the clock period. Using $T \geq t_{reg} + t_{logic} + t_{setup} - \delta$, we get $T_{min} = 1 + 7 + 1 = 9$.

b. With finite clock skew, the time periods for different paths are as follows: $T_{min}(p1) = 9 - 1 = 8$, $T_{min}(p2) = 6$, $T_{min}(p3) = 7$, $T_{min}(p4) = 7 - 1 = 6$ (Note that the clock skew is 0 for paths p2 and p3). Therefore the minimum clock period is $T_{min} = 8$.

c. As the clock skew increases, the most significant path changes. Repeating the calculations in part (b) we get: $T_{min}(p1) = 9 - 4 = 5$, $T_{min}(p2) = 6$, $T_{min}(p3) = 7$, $T_{min}(p4) = 7 - 4 = 3$ (Note that the clock skew is 0 for paths p2 and p3). Therefore the minimum clock period is $T_{min} = 7$.

d. The maximum positive clock skew is determined by the inequality $\delta \leq t_{cd,reg} + t_{cd,logic}$. Assuming that the contamination delay is same as the propagation delay, we get $\delta_{max} = 1 + 3 + 2 = 6$. Note that p4 determines the maximum tolerable skew (the fastest path will produce the earliest contamination). Paths p3 and p2 do not matter since there is no skew involved.

e. The maximum positive negative skew has no bound since the clock period has no upper bound.

2.

### Table 1: Sources of Skew and Jitter

<table>
<thead>
<tr>
<th>Source</th>
<th>Skew</th>
<th>Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Uncertainty in the clock generation circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2) Process variation in devices</td>
<td>Skew</td>
<td>Jitter</td>
</tr>
<tr>
<td>3) Interconnect variation</td>
<td>Skew</td>
<td>Jitter</td>
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<tr>
<td>4) Power Supply Noise</td>
<td>Skew</td>
<td>Jitter</td>
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<tr>
<td>5) Data Dependent Load Capacitance</td>
<td>Skew</td>
<td>Jitter</td>
</tr>
<tr>
<td>6) Static Temperature Gradient</td>
<td>Skew</td>
<td>Jitter</td>
</tr>
</tbody>
</table>

a. Approach A results in lower jitter. For Approach A, the capacitance seen by CLK is independent of data (the Enable signals) to first order.
3.

![Timing diagram](image)

**Figure 2: Timing diagram.**

**a.**

b. b should be ready before the rising edge of CLK for the negative latch to latch and hold its value. d should be ready before the falling edge of CLK for the second positive latch to latch and hold its value.

c. The clock can be reduced by 20ns. In general, it may be difficult to identify how much slack can be removed from the clock because it depends on the length of the pipeline too.

7.

**a.**

\[
t_p = \frac{5 + 10 + 20}{3} + 6 = 17.67\,ns
\]

\[
f = 56.6\,MHz
\]

**b.**

\[
t_p = \frac{5 + 10 + 20}{3} + 12 = 23.67\,ns
\]

\[
f = 42.2\,MHz
\]

**c.** In setting clock frequency, we account for the longest delay:

\[
f = \frac{1}{20\,ns} = 50\,MHz
\]

Note that the delay in the handshaking circuit can be a strong factor in choosing clocking strategies.
a. The circuit works by using the overlap of two clocks from a ring oscillator to dictate the duty cycle. Longer overlap yields a greater duty cycle.

Clock signal from ANDing 1 + 4 gives 28.6% duty cycle.

b. The range of duty cycles is: 7-50%.

c. Inverting the output signal converts a 25% duty cycle to a 75% duty cycle.

Figure 3: Duty cycle.