CMOS Logic

Courtesy of Prof. Nikolic (Berkeley)
Combinational vs. Sequential Logic

Combinational Logic Circuit

Output = \( f(\text{In}) \)

Sequential Logic Circuit

Output = \( f(\text{In}, \text{Previous In}) \)

Courtesy of Prof. Nikolic
(Berkeley)
Static Complementary CMOS

PUN and PDN are dual logic networks
PUN and PDN functions are complementary
**NMOS Transistors in Series/Parallel Connection**

Transistor can be thought of as a switch controlled by its gate signal.

NMOS switch closes when switch control input is high.

![NMOS circuit diagram]

\[ Y = X \text{ if } A \text{ AND } B \]

\[ Y = X \text{ if } A \text{ OR } B \]

NMOS Transistors pass a “strong” 0 but a “weak” 1

EECS141

Courtesy of Prof. Nikolic
(Berkeley)
**PMOS Transistors in Series/Parallel Connection**

PMOS switch closes when switch control input is low

\[ Y = X \text{ if } A \text{ AND } B = A + B \]

\[ Y = X \text{ if } A \text{ OR } B = AB \]

PMOS Transistors pass a “strong” 1 but a “weak” 0

 Courtesy of Prof. Nikolic (Berkeley)
Complementary CMOS Logic Style

- PUP is the **DUAL** of PDN
  (can be shown using DeMorgan’s Theorem’s)
  \[
  \overline{A + B} = \overline{A} \overline{B} \\
  \overline{AB} = \overline{A} + \overline{B}
  \]
- The complementary gate is inverting

\[
\text{AND} = \text{NAND} + \text{INV}
\]
Example Gate: NOR

A | B | Out
---|---|---
0 | 0 | 1
0 | 1 | 0
1 | 0 | 0
1 | 1 | 0

Truth Table of a 2 input NOR gate

OUT = \overline{A + B}
Static CMOS Design

EECS141

Courtesy of Prof. Nikolic
(Berkeley)
Input Pattern Effects on Delay

- Delay is dependent on the pattern of inputs
- Low to high transition
  - both inputs go low
    - delay is \( 0.69 \frac{R_p}{2} C_L \)
  - one input goes low
    - delay is \( 0.69 R_p C_L \)
- High to low transition
  - both inputs go high
    - delay is \( 0.69 \frac{2R_n}{C_L} \)
### Delay Dependence on Input Patterns

**Graph:**
- **Voltage [V]**: Range from -0.5 to 3
- **Time [ps]**: Range from 0 to 400
- **Curves:**
  - A=B=1 → 0
  - A=1 → 0, B=1
  - A=1, B=1 → 0

**Table:**

<table>
<thead>
<tr>
<th>Input Data Pattern</th>
<th>Delay (psec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A=B=0 → 1</td>
<td>67</td>
</tr>
<tr>
<td>A=1, B=0 → 1</td>
<td>64</td>
</tr>
<tr>
<td>A=0 → 1, B=1</td>
<td>61</td>
</tr>
<tr>
<td>A=1, B=1 → 0</td>
<td>45</td>
</tr>
<tr>
<td>A=1 → 0, B=1</td>
<td>80</td>
</tr>
<tr>
<td>A=1 → 0, B=1</td>
<td>81</td>
</tr>
</tbody>
</table>

**Notes:**
- NMOS = 0.5μm/0.25 μm
- PMOS = 0.75μm/0.25 μm
- \( C_L = 100 \text{ ff} \)

**Courtesy of Prof. Nikolic (Berkeley)**
Transistor Sizing a Complex CMOS Gate

\[ \text{OUT} = D + A \cdot (B + C) \]
Transistor Sizing a Complex CMOS Gate

\[ \text{OUT} = D + A \cdot (B + C) \]
**Fan-In Considerations**

Distributed RC model (Elmore delay)

\[ t_{pHL} = 0.69 \, R_{eqn} (C_1 + 2C_2 + 3C_3 + 4C_L) \]

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.
$t_p$ as a Function of Fan-In

Gates with a fan-in greater than 4 should be avoided.

Courtesy of Prof. Nikolic (Berkeley)
$t_p$ as a Function of Fan-Out

All gates have the same drive current.

Slope is a function of "driving strength"
$t_p$ as a Function of Fan-In and Fan-Out

- Fan-in: quadratic due to increasing resistance and capacitance
- Fan-out: each additional fan-out gate adds two gate capacitances to $C_L$

$$t_p = a_1 Fl + a_2 Fl^2 + a_3 FO$$
Fast Complex Gates: Design Technique 1

- Transistor sizing
  - as long as fan-out capacitance dominates
- Progressive sizing

![Diagram of transistor sizing and RC line](image)

- Distributed RC line
  - M1 > M2 > M3 > ... > MN
  - (the FET closest to the output is the smallest)

Can reduce delay by more than 20%; Be careful: input loading, junction caps, decreasing gains as technology shrinks

Courtesy of Prof. Nikolic
(Berkeley)
Fast Complex Gates: Design Technique 2

- Transistor ordering

Diagram showing two circuits with labeled transistors and capacitors, indicating that the delay is determined by the time to discharge certain capacitors. The circuits are labeled "charged" and "discharged."
- Eight bit bus BER checking?

Courtesy of Prof. Nikolic
(Berkeley)
Fast Complex Gates: Design Technique 4

- Isolating fan-in from fan-out using buffer insertion

Courtesy of Prof. Nikolic (Berkeley)
Fast Complex Gates: Design Technique 5

- Reducing the voltage swing
  
  \[ t_{PHL} = 0.69 \left( \frac{3}{4} \left( \frac{C_L}{V_{DD}} \right) / I_{DSATn} \right) \]
  
  \[ = 0.69 \left( \frac{3}{4} \left( \frac{C_L}{V_{swing}} \right) / I_{DSATn} \right) \]

  - linear reduction in delay
  - also reduces power consumption

- But the following gate is much slower!

- Or requires use of “sense amplifiers” on the receiving end to restore the signal level (memory design)
XOR2
XNOR2

Courtesy of Prof. Nikolic
(Berkeley)
Multiplexer
Pass-Transistor Logic

Courtesy of Prof. Nikolic (Berkeley)
Pass-Transistor Logic

- N transistors
- No static consumption

Courtesy of Prof. Nikolic (Berkeley)
Example: AND Gate

$F = AB$

Courtesy of Prof. Nikolic (Berkeley)
NMOS-Only Logic

![Diagram](image-url)

Courtesy of Prof. Nikolic (Berkeley)
**NMOS-only Switch**

\[ V_B \] does not pull up to 2.5V, but 2.5V \(-V_{TN}\)

Threshold voltage loss causes static power consumption

NMOS has higher threshold than PMOS (body effect)

Courtesy of Prof. Nikolic
(Berkeley)
**NMOS Only Logic: Level Restoring Transistor**

- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

Courtesy of Prof. Nikolic (Berkeley)
Restorer Sizing

- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

![Graph showing voltage over time with different W/L ratios.](image)

EECS141

Courtesy of Prof. Nikolic (Berkeley)
Complementary Pass Transistor Logic

(a) Pass-Transistor Network

(b) Inverse Pass-Transistor Network

EECS141

Courtesy of Prof. Nikolic (Berkeley)
Solution 2: Transmission Gate

A = 2.5 V

C = 0 V

C = 2.5 V
Solution 2: Transmission Gate

![Diagram of Transmission Gate Circuits]

Courtesy of Prof. Nikolic
(Berkeley)
Resistance of Transmission Gate

![Graph showing the resistance of transmission gate]

Courtesy of Prof. Nikolic (Berkeley)
Pass-Transistor Based Multiplexer

 Courtesy of Prof. Nikolic
 (Berkeley)
Transmission Gate XOR

Courtesy of Prof. Nikolic
(Berkeley)
Delay in Transmission Gate Networks

(a)

(b)

(c)

EECS141

Courtesy of Prof. Nikolic
(Berkeley)
Delay Optimization

- Delay of RC chain

\[ t_p = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2} \]

- Delay of Buffered Chain

\[ t_p = 0.69 \left[ CR_{eq} \frac{m(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ = 0.69 \left[ CR_{eq} \frac{n(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ m_{opt} = 1.7 \sqrt{\frac{t_{buf}}{CR_{eq}}} \]
Writing into a Static Latch

Use the clock as a decoupling signal, that distinguishes between the transparent and opaque states.

Forcing the state (can implement as NMOS-only)  Converting into a MUX

 Courtesy of Prof. Nikolic (Berkeley)
**Latch Properties**

- Two phase operation
  - Clk = 1: transparent
  - Clk = 0: latches data
- Transparency can cause the data contamination
  - Often avoided by using edge-triggered registers
Master-Slave (Edge-Triggered) Register

Two opposite latches trigger on edge
Also called master-slave latch pair

EECS141
Master-Slave Register

Multiplexer-based latch pair
Inverter-Based 4 State Tri-State

- Inverter -> series pass-gate
- 4-Stack Tri-State
Reduced Clock Load
Master-Slave Register
Clk-Q Delay

![Diagram of Clk-Q Delay]

Volts

CLK

D

q(lh)

Q

q(hl)

time, nsec

0 0.5 1 1.5 2 2.5

EECS141

Courtesy of Prof. Nikolic (Berkeley)
Setup Time

(a) $T_{\text{setup}} = 0.21 \text{ nsec}$

(b) $T_{\text{setup}} = 0.20 \text{ nsec}$

Courtesy of Prof. Nikolic (Berkeley)
More Precise Setup Time

Courtesy of Prof. Nikolic
(Berkeley)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data Clock

T_{Setup-1}

EECS141

Courtesy of Prof. Nikolic
(Berkeley)
Setup-Hold Time Illustrations

Hold-1 case

Clock Data

T_{Hold-1}

T_{Clk-Q} Delay

EECS141

Courtesy of Prof. Nikolic (Berkeley)
Other Latches/Registers: $C^2$MOS

Master Stage

Slave Stage

Keepers should be added to staticize

EECS141

Courtesy of Prof. Nikolic
(Berkeley)
• Mealy
• Moore
Sequential Logic

Courtesy of Prof. Nikolic
(Berkeley)
Power Consumption of Logic

• Probability of activity

Courtesy of Prof. Nikolic
(Berkeley)
Pipelined Logic

• Figure of pipeline stages

Courtesy of Prof. Nikolic (Berkeley)
- Mealy
- Moore

Combinational vs. Sequential Logic

Combinational Logic Circuit

Output = f(In)

Sequential Logic Circuit

Output = f(In, Previous In)
Writing into a Static Latch

Use the clock as a decoupling signal, that distinguishes between the transparent and opaque states

Forcing the state (can implement as NMOS-only)  Converting into a MUX

Courtesy of Prof. Nikolic
(Berkeley)
**Latch Properties**

- Two phase operation
  - $\text{Clk} = 1$: transparent
  - $\text{Clk} = 0$: latches data
- Transparency can cause the data contamination
  - Often avoided by using edge-triggered registers
Master-Slave (Edge-Triggered) Register

Two opposite latches trigger on edge
Also called master-slave latch pair
Master-Slave Register

Multiplexer-based latch pair
Inverter-Based 4 State Tri-State

- Inverter -> series pass-gate
- 4-Stack Tri-State
- Reset/Set D-FF

Courtesy of Prof. Nikolic
(Berkeley)
Reduced Clock Load Master-Slave Register

Courtesy of Prof. Nikolic
(Berkeley)
Clk-Q Delay

Volts vs time, nsec

Courtesy of Prof. Nikolic
(Berkeley)
Setup Time

(a) $T_{\text{setup}} = 0.21$ nsec

(b) $T_{\text{setup}} = 0.20$ nsec

Courtesy of Prof. Nikolic
(Berkeley)
More Precise Setup Time

(a)

(b)

1.05 \( t_{C-Q} \)

\( t_{C-Q} \)

\( t_{SW} \)

\( t_{H} \)

\( t_{D-C} \)

EECS141

Courtesy of Prof. Nikolic
(Berkeley)
Setup-Hold Time Illustrations

Hold-1 case

Clock [Data]

Time

T_{Hold-1}

T_{clk-Q}

T_{clk-Q} Delay

Courtesy of Prof. Nikolic
(Berkeley)
Other Latches/Registers: $C^2$MOS

Keepers should be added to staticize

EECS141

Courtesy of Prof. Nikolic (Berkeley)