2. This problem examines sources of skew and jitter.
   a. A balanced clock distribution scheme is shown in Figure 0.2. For each source of variation, identify if it contributes to skew or jitter. Circle your answer in Table 0.1

![Diagram of clock distribution scheme]

**Figure 0.2** Sources of Skew and Jitter in Clock Distribution.

<table>
<thead>
<tr>
<th>Source</th>
<th>Skew</th>
<th>Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Uncertainty in the clock generation circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2) Process variation in devices</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3) Interconnect variation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4) Power Supply Noise</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5) Data Dependent Load Capacitance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6) Static Temperature Gradient</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 0.1** Sources of Skew and Jitter
b. Consider a Gated Clock implementation where the clock to various logical modules can be individually turned off as shown in Figure 0.3. (i.e., \(\text{Enable}_1, \ldots, \text{Enable}_N\) can take on different values on a cycle by cycle basis). Which approach (A or B) results in lower jitter at the output of the input clock driver? (hint: consider gate capacitance) Explain.

**Solution**

Approach A results in lower jitter. For Approach A, the capacitance seen by CLK is independent of data (the Enable signals) to first order.

5. Consider the following latch based pipeline circuit shown in Figure 0.16.

Assume that the input, \(\text{IN}\), is valid (i.e., set up) 2ns before the falling edge of \(\text{CLK}\) and is held till the falling edge of \(\text{CLK}\) (there is no guarantee on the value of \(\text{IN}\) at other times). Determine the maximum positive and negative skew on \(\text{CLK}'\) for correct functionality.
Solution

The positive and negative skew are given after the analysis below.

Positive Skew

\[ \delta^+_{\text{MAX}} = t_{D-Q} + t_{\text{CD}} = 2\text{ns} \]

Negative Skew

\[ \delta^-_{\text{MAX}} = 2 \cdot \frac{1}{2} \cdot t_p + t_{su} = 3\text{ns} \]
7. For the self-timed circuit shown in Figure 0.18, make the following assumptions. The propagation through the NAND gate can be 5 nsec, 10 nsec, or 20 nsec with equal probability. The logic in the succeeding stages is such that the second stage is always ready for data from the first.

a. Calculate the average propagation delay with $t_{hz} = 6$ nsec.

Solution

$$t_p = \frac{5 + 10 + 20}{3} + 6 = 17.67\,\text{ns}$$

$$f = 56.6\,\text{MHz}$$

b. Calculate the average propagation delay with $t_{hz} = 12$ nsec.

Solution

$$t_p = \frac{5 + 10 + 20}{3} + 12 = 23.67\,\text{ns}$$

$$f = 42.2\,\text{MHz}$$

c. If the handshaking circuitry is replaced by a synchronous clock, what is the smallest possible clock frequency?

![Figure 0.18 Self-timed circuit.](image)

Solution

In setting clock frequency, we account for the longest delay:

$$f = \frac{1}{20\,\text{ns}} = 50\,\text{MHz}$$

Note that the delay in the handshaking circuit can be a strong factor in choosing clocking strategies.