ECE 471 Midterm #1 WIN-2013

Name:

Student Number:

Midterm Score:
Problem 1 (Total 50 Points):
Problem 2 (Total 30 Points):
Problem 3 (Total 20 Points):
Total:

NOTE: Make ALL Assumptions. Some partial credit given, given that ALL assumptions are first made and written down. When in doubt, use transistor models as assumed by the book, lectures, and homework problems.

When in doubt, MAKE ALL ASSUMPTIONS. I will reward understanding, less about memorization.

ANSW KEY
PROBLEM 1: Logic Function

a) Implement the logic function: \( Y = \overline{A(C \cdot D + E)} \)

in a single CMOS logic gate.

(5-points) \[ \text{Pull up: } Y = \overline{A} + (\overline{C} + \overline{D} + \overline{E}) \quad \text{Pull down: } \overline{Y} = A(C \cdot D + E) \]

b) Size this logic gate, with its NMOS/PMOS transistors minimally sized to match the minimum-sized inverter. INV(min): PMOS=8\(\lambda\)/2\(\lambda\); NMOS=4\(\lambda\)/2\(\lambda\), where 2\(\lambda\)=0.25\(\mu\)m in your technology

(5-points) See above diagram
c) What is the input sequence that enables the fastest $t_{PLH}$? Calculate this $T_{\text{delay}}$, assuming that you only have to worry about: $R_{\text{trans}}$ (of each transistor, which is identical to the $R_{\text{trans}}$ of a minimum-sized inverter), $C_{\text{load}}$ (loading on the output $Y$), and $C_{\text{diff}}$ (Each transistor has ONLY-1 parasitic capacitance for both the source/drain regions of the transistor -- you can ignore $C_{\text{GD}}$ and assume that both $C_{\text{DB}}$ and $C_{\text{SB}}$ are equal to $C_{\text{diff}}$).

(10-points)

\[ C_{\text{total}} = C_{\text{diff}A} + C_{\text{diff}E} + C_{\text{diff}C} + C_{\text{load}} \]

\[ R_{\text{total}} = R_{\text{trans}} \left[ \frac{R_{\text{trans}}}{2} + \left( \frac{R_{\text{trans}}}{2} \right) \right] \]

\[ T_{\text{delay}} = 0.69 C_{\text{total}} R_{\text{total}} \]

\[ R_{\text{trans}} = \frac{1}{2} R_{\text{trans}} \]

\[ R_{\text{trans}} \] minimum-sized

d) What is the average, dynamic power consumption of this gate? (HINT: you need to know the probability that the output will be switching from 0 -> 1) (10-points)

make truth table \( 11 \rightarrow 1's \) \( 5 \rightarrow 0's \)

\[ P_{\text{avg}} = C_{\text{total}} \cdot V_{\text{dd}}^2 \cdot f = \frac{5}{16} \cdot \frac{11}{16} \cdot C_{\text{total}} \cdot V_{\text{dd}}^2 \cdot f \]

equal to $C_{\text{total}}$ in Part C
e) Draw a stick diagram for the logic gate from part a), with a goal to minimize the diffusion capacitance. Please use vertical lines for poly gates and horizontal lines for diffusion strips. Label your transistors. DON'T FORGET SUBSTRATE VIA CONNECTIONS.
(10-points)

f) Do this design using Pass-Gate Logic (NOT CMOS). Make sure you take care of all possible input cases.
(10-points)
PROBLEM 2. Wire Resistance / Capacitance (30-points)

a. Determine the optimal number of delay stages and the inverter sizing to drive the final output capacitance (the off-chip, pad capacitance that is bonded to the off-chip PCB). Assume the Output Pad Cap is built in top-layer M8 metal, with a $R_{\text{SQUARE}} = 0.02$ ohms/square. Assume no other wires are nearby, and the distance this M1 metal is off of the GND (GROUNDED SILICON SUBSTRATE) = 0.1um. Assume the dielectric constant in this technology is SiO2. Assume the resistance/capacitance of Wire-1 is negligible for part-a. Assume the front-stage min-size inverter is INV(min): PMOS=$8\lambda/2\lambda$; NMOS=$4\lambda/2\lambda$.

(10-points)

\[ C_{\text{pad}} = \frac{C_{\text{oxide}}}{1 + \frac{W_{\text{metal}}}{1}} = \frac{3.95 \times 10^{-12}}{0.1} \times 10^{-8} \times 0.1 = \frac{3.45 \times 10^{-17}}{0.1} \times 10^{-8} \approx 3450 \text{fF} \]

\[ C_{\text{in}} = (4\lambda/2\lambda + 8\lambda/2\lambda) = 12\lambda/2\lambda \\
= 12 \times 0.125 \mu\text{m} \times 12 \times 2.0 \text{fF} \times 0.1 \mu\text{m} = 3 \text{fF} \]

\[ W_8 = 0.1 \mu\text{m} \quad N = \frac{1 \text{fF}}{3} \times 3450 = 7.07 \approx 7 \text{fF} \]

\[ W_8 = 1 \mu\text{m} \quad N = \frac{1 \text{fF}}{3} \times 2.44 = 3.5 \text{fF} \]
b. Now due to real-world realities, the proposed design from part-A is far too optimistic, with respect to the package parasitics. In reality, a 1-pF ESD diode is located on the output pad, to prevent human static discharge. In addition, the output pad capacitance is moved from the M1 to the M8 metal layer.

Still assuming that Wire-1 resistance/capacitance is negligible, resize the tapered inverters and the final number/sizing of inverter stages to drive this M8 pad capacitor.

\[
N = \frac{C_{pad}}{C_{inv}} = \frac{1.03 \text{pF}}{5.8} = 0.18 \text{ stages}
\]

\[
N = \frac{C_{pad}}{C_{inv}} = \frac{4.95 \text{pF}}{7.3} = 0.67 \text{ stages}
\]

(10-points)

c. Now, a bad engineer who didn’t take ECE471, routed a VERY narrow M1 wire between the final inverter and the output pad capacitor (built in M1 as well). This narrow wire is 0.02um wide, and 2000um long, with a \(R_{\text{square}} = 0.2\) Ohms/square, 0.1um height above the GND plane, and over a SiO2 dielectric (use part-a for comparison).

Assuming that the output resistance of the final inverter is 1k Ohms, how much worse did the delay, with respect to part-a? (delay when Wire-1 is negligible versus when Wire-1 is 0.02um wide and 2000um long. Ignore part-b for this part-c.)

(10-points)
PROBLEM 3. (20 pts) Scaling.

a) (5pts) A company has implemented a single-core microprocessor in 65nm technology with 400mV threshold voltages, that operates at 2GHz with a 1.0V supply, with a 100W power dissipation, and a die size of 100mm². They would like to build a quad-core microprocessor in the same technology, by replicating the single-core design four times. At which frequency and supply voltage should the quad-core design be running to maintain the same size of the heat sink? (HINT: same total power consumption)

You can assume that the frequency of operation is roughly linearly proportional to the supply voltage in this technology.

\[
\frac{1}{2} CV_0^2 = 100W
\]

\[
V_T = 0.62mV
\]

\[
V_{DD} = 1.2V
\]

b) (7pts) If the single-core design is ported to a 16nm technology with a 0.6V supply, what would be its size, frequency of operation and power? You can assume that all of the power is switching power.

\[
\frac{16\text{nm}}{16\text{nm}} = 0.246
\]

\[
A_{area} = (0.246 \cdot \sqrt{1W}) \cdot (0.216 \cdot \sqrt{VDD})
\]

\[
= 0.103 \text{ \mu m}^2
\]

\[
ho L = 0.246 \cdot 2.5+T
\]

\[
T = \frac{1}{0.246} \cdot 2.6\text{GHz}
\]

\[
= 5.73 \text{GHz}
\]

\[
V = \frac{1}{2} (0.246 \cdot \mu F) (10V)^2 = 18.86\text{mV}
\]

\[= 35.9\text{mV}
\]

\[
\text{Scale by } V = \frac{0.6}{1.0} \cdot 400\text{mV}
\]

\[= 240\text{mV}
\]