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NOTE: Make ALL Assumptions. Some partial credit given, given that ALL assumptions are first made and written down. Use transistor models as assumed in the book and homework problems.
b. Determine what the worst case t\text{PHL} will be, assuming this gate is driving a minimum size inverter. Assume the gate is driving a minimum size inverter.

(8 points)

\[
C_{\text{Tot}} \mid_{z=1, \ \bar{z}=0, \ \bar{z}=0} = 1
\]

\[
R_{\text{EL}} = \frac{2}{V_{\text{DD}}} \frac{V_{\text{OH}}}{V_{\text{IH}}}
\]

\[
\Phi_{\text{min}} \left( \left[ Z C_{\text{sd}} + C_{\text{pe}} C_{\text{gs}} C_{\text{dr}} \right] + \left[ C_{\text{on}} C_{\text{co}} C_{\text{ss}} + C_{\text{st}} + C_{\text{co}} + C_{\text{so}} \right] \right)
\]

\[
+ \left[ C_{\text{sd}} C_{\text{ms}} \right] + \left[ Z C_{\text{sd}} C_{\text{pe}} \right] + Z C_{\text{sd}} + C_{\text{gs}}
\]

\[
T_{\text{PHL}} = 0.69 R_{\text{EL}} C_{\text{tot}}
\]
Input vector: $\begin{pmatrix} 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \end{pmatrix}$

$c = \begin{pmatrix} 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \end{pmatrix}$

$F = \begin{pmatrix} 0 & 0 & 1 & 1 & 1 \end{pmatrix}$

$\gamma = \frac{8}{3}$

$\overline{\gamma} = \frac{8}{3}$

Therefore, for the $f$ given, a viable distribution of $\gamma$ and $f$ is possible.

What is the dynamic power, given $\gamma$?
5 points

NOS connections. Do not forget critical contacts. Use well connected

Draw a simple layout sketch of this design using blocks/wire bonding for this
An IC has a wire that is 2 mm wide and 10 mm long. For each of the ideas given below, say whether the resulting wire will be more than 2x faster, 2x faster, same speed, or less than 2x faster. Please show your reasons. In this problem we are only worried about the RC delay of the wire. Assume the driver of the wire has no output resistance.

a) Drive the wire at the middle of the wire, rather than at one end. (4 points)

b) Double the oxide thickness between the wire and the ground plane. (4 points)

c) Quadruple the vertical thickness of the wire. (4 points)

d) Shrink all 3 dimensions of the wire by 2x. (It is 2x thick, 2x wide, and 2x long). (4 points)
delay of the input (5 points)
the driver resistor/capacitance, how much longer/shorer is the propagation
8. Since the supply voltage Vdd has been increased by kV, reflect the changes in

4 points
the increased to Vdd = 2 * Vd. How much has the power been increased by?
We are changing the line with a supply voltage of Vdd = Vd. Now, the supply

5 points

(2 points)
assumed the is isolated wire, without any wires around (1) (4 points)
Shrink wire to 3mm x 1mm, bearing thickness of wire and oxide unaffected.
Question 2: Transmission Gates

For the logic $\text{OUT} = A \cdot B + C$

Now use Transmission Gates to build up this circuit (10 points)
I have any military experience. (10 points)

For this part of the problem, you can make a lot of assumptions about the logic gate is driven by a minimum size inverter. (1)

I have to get the smallest size inverters (2) . The input to the

b) Determine what the worst case propagation delay will be assuming that