ECE 271 – Digital Logic Design

Catalog Description: A first course in digital logic design. Data types and representations, Boolean algebra, state machines, simplification of switching expressions, and introductory computer arithmetic.

Credits: 3 **Terms Offered:** Fall, Spring

Prerequisites: MTH 251 or MTH 251H or MTH 231 (concurrent enrollment acceptable)

Courses that require this as a prerequisite: ECE 272, ECE 375

Structure: Three 50-minute lectures per week

Instructors: M. Shuman

Course Content:

- Concepts and definitions used in digital logic design: notation, number systems, difference between analog and digital system, specification and implementation, analysis and design, design cycle, CAD tools, combinational systems, high-level specs, data representation and coding, binary specs, switching functions (truth tables), gates
- Boolean (switching) algebra and switching expressions
- Gate networks: definition, description. Sets of gates. NAND-NAND and NOR-NOR networks.
- Analysis of gate networks (combinational system). Characteristics of gate networks
- Design of combinational systems. 2-level networks. Minimal two-level nets, Karnaugh maps
- Standard combinational modules: decoders, encoders, priority encoders, multiplexers, demultiplexers, and combinational shifters. Multiplexers as universal modules
- Specification of sequential systems, state description of sequential systems, Mealy and Moore machines, state diagram, time behavior, and binary specification
- Sequential networks, canonical nets, gated latch and D flip-flop, other flip-flops: SR, JK, and T
- Analysis/Design of sequential networks
- Standard sequential modules: registers, shift registers, and counters
- Design of sequential systems using counters or special state assignments
- Controllers and state minimization of sequential systems
- Arithmetic combinational modules. Adders for positive integers: full-adder and carry lookahead adder. Representation of signed integers and operations: addition and subtraction. ALU and comparator modules
- Programmable devices: programmable sequential arrays (PSA), ROM, and circuits with ROMs. Networks of programmable modules and FPGAs

Measurable Student Learning Outcomes:
At the completion of the course, students will be able to…

1. **Map** the high-level description of a digital system into a binary description of it (ABET Outcomes: A,M)
2. **Analyze and design** combinational systems using standard gates and minimization methods (such as Karnaugh maps) (ABET Outcomes: A,C,N)
3. **Analyze and design** simple synchronous sequential systems (ABET Outcomes: A,C,N)
4. **Analyze and design** sequential systems composed of standard sequential modules, such as counters and registers (ABET Outcomes: A,C,N)
5. **Perform** basic arithmetic operations with signed integers represented in binary (ABET Outcomes: A,M,N)

Learning Resources:

- Harris, David Money & Harris, Sarah L., *Digital Design and Computer Architecture, 2nd Edition, Morgan Kaufmann.* ECE 272, lab to implement ECE 271 concepts.
- ECE 199, Build a TekBot Course (needed students in 272 who do not have a TekBot).
- *Lattice Diamond Software*
- *Beaversource Repository Link (for example designs)*

Students with Disabilities:
Accommodations are collaborative efforts between students, faculty and Disability Access Services (DAS). Students with accommodations approved through DAS are responsible for contacting the faculty member in charge of the course prior to or during the first week of the term to discuss accommodations. Students who believe they are eligible for accommodations but who have not yet obtained approval through DAS should contact DAS immediately at 737-4098.

Link to Statement of Expectations for Student Conduct:
http://oregonstate.edu/admin/stucon/achon.htm

Revised: 9/1/07
Revised Learning Resources and Students with Disabilities: 2/15/11
Revised: 9/15/14