DISPLAY UNIT USER’S MANUAL

Dot-Matrix LCD Units
(with built-in controllers)

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Contents

PREFACE ....................................................... 2
FEATURES .................................................... 3
OVERVIEW .................................................... 3
HARDWARE ..................................................... 4
   Interface Signals ........................................ 4
   Functional Blocks ...................................... 4
   Microprocessor Interface ............................... 11
   Reset Function .......................................... 12
INSTRUCTIONS ............................................... 15
   General Information ................................... 15
   Description of Instruction ............................. 15
ELECTRICAL CHARACTERISTICS ....................... 19
   Absolute Maximum Ratings ......................... 19
   Electrical Characteristics ........................... 19
   Timing Characteristics ................................. 19
   Power Conditions for Internal Reset ............... 20
LCD UNIT USAGE INSTRUCTIONS ....................... 21
   Interface with External Microprocessor ........... 21
   Contrast Control Voltage ............................. 24
   Sample Instruction Procedures ..................... 24
HANDLING INSTRUCTIONS ................................. 28
OPERATING RESTRICTIONS ............................... 29
PREFACE

The Sharp dot-matrix LCD units, with built-in controllers, operate under the control of a 4-bit or 8-bit microcomputer to display alphanumeric characters, symbols, etc. The LCD unit provides the user with a dot-matrix display panel featuring simple interface circuitry.

Table 1.
Dot-Matrix LCD Unit with Built-In Controllers

<table>
<thead>
<tr>
<th>MODEL NO.</th>
<th>NUMBER OF CHARACTERS</th>
<th>DISPLAY FORMAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM161XXX</td>
<td>16 × 1</td>
<td>5 × 7 dots</td>
</tr>
<tr>
<td>LM162XXX</td>
<td>16 × 2</td>
<td>5 × 7 dots</td>
</tr>
<tr>
<td>LM202XXX</td>
<td>20 × 2</td>
<td>5 × 7 dots</td>
</tr>
<tr>
<td>LM40X2XX</td>
<td>40 × 2</td>
<td>5 × 7 dots</td>
</tr>
</tbody>
</table>
FEATURES

- Interface with either 4-bit or 8-bit microprocessor.
- Display data RAM
- $80 \times 8$ bits (80 characters).
- Character generator ROM
- 160 different $5 \times 7$ dot-matrix character patterns.
- Character generator RAM
- 8 different user programmed $5 \times 7$ dot-matrix patterns.
- Display data RAM and character generator RAM may be accessed by the microprocessor.
- Numerous instructions
- Clear Display, Cursor Home, Display ON/OFF, Cursor ON/OFF, Blink Character, Cursor Shift, Display Shift.
- Built-in reset circuit is triggered at power ON.
- Built-in oscillator.

OVERVIEW

The LCD unit receives character codes (8 bits per character) from a microprocessor or microcomputer, latches the codes to its display data RAM (80-byte DD RAM for storing 80 characters), transforms each character code into a $5 \times 7$ dot-matrix character pattern, and displays the characters on its LCD screen.

The LCD unit incorporates a character generator ROM which produces 160 different $5 \times 7$ dot-matrix character patterns. The unit also provides a character generator RAM (64 bytes) through which the user may define up to eight additional $5 \times 7$ dot-matrix character patterns, as required by the application.

To display a character, positional data is sent via the data bus from the microprocessor to the LCD unit, where it is written into the instruction register. A character code is then sent and written into the data register. The LCD unit displays the corresponding character pattern in the specified position. The LCD unit can either increment or decrement the display position automatically after each character entry, so that only successive characters codes need to be entered to display a continuous character string. The display/cursor shift instruction allows the entry of characters in either the left-to-right or right-to-left direction. Since the display data RAM (DD RAM) and the character generator RAM (CG RAM) many be accessed by the microprocessor, unused portions of each RAM may be used as general purpose data areas. The LCD unit may be operated with either dual 4-bit or single 8-bit data transers, to accommodate interfaces with both 4-bit and 8-bit microprocessors. The low power feature of the LCD unit will be further appreciated when combined with a CMOS microprocessor.
HARDWARE

Interface Signals

Table 2. Interface Signals

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>INPUT/OUTPUT</th>
<th>EXTERNAL CONNECTION</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS</td>
<td>Input</td>
<td>MPU</td>
<td>MPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Register select signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;0&quot;: Instruction register (when writing)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Busy flag and address counter (when reading)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;1&quot;: Data register (when writing and reading)</td>
</tr>
<tr>
<td>R/W</td>
<td>Input</td>
<td>MPU</td>
<td>MPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Read/write select signal: &quot;0&quot;: Writing; &quot;1&quot;: Reading</td>
</tr>
<tr>
<td>E</td>
<td>Input</td>
<td>MPU</td>
<td>MPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Operation (data read/write) enable signal</td>
</tr>
<tr>
<td>DB4 - DB7</td>
<td>Input/Output</td>
<td>MPU</td>
<td>MPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>High-order lines of data bus with three-state, bidirectional function for use in data transactions with the MPU. DB7 may also be used to check the busy flag.</td>
</tr>
<tr>
<td>DB0 - DB3</td>
<td>Input/Output</td>
<td>MPU</td>
<td>MPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Low-order lines of data bus with three-state, bidirectional function for use in data transactions with the MPU. These lines are not used when interfacing with a 4-bit microprocessor.</td>
</tr>
<tr>
<td>VDD, VSS</td>
<td>Power Supply</td>
<td></td>
<td>Vdd: +5 V, Vss: GND</td>
</tr>
<tr>
<td>V0</td>
<td>Power Supply</td>
<td></td>
<td>Contrast adjustment voltage</td>
</tr>
</tbody>
</table>

Functional Blocks

Registers

The LCD unit has two 8-bit registers - an instruction register (IR) and a data register (DR). The instruction register stores instruction codes such as "clear display" or "shift cursor", and also stores address information for the display data RAM and character generator RAM. The IR can be accessed by the microprocessor only for writing.

The data register is used for temporarily storing data during data transactions with the microprocessor. When writing data to the LCD unit, the data is initially stored in the data register, and is then automatically written into either the display data RAM or character generator RAM, as determined by the current operation. The data register is also used as a temporary storage area when reading data from the display data RAM or character generator RAM. When address information is written into the instruction register, the corresponding data from the display data RAM or character generator RAM is moved to the data register. Data transfer is completed when the microprocessor reads the contents of the data register by the next instruction. After the transfer is completed, data from the next address position of the appropriate RAM is moved to the data register, in preparation for subsequent reading operations by the microprocessor. One of the two registers is selected by the register select (RS) signal.

Table 3. Register Selection

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Write to instruction register, and execute internal operation (clear display, etc.)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Read busy flag (DB7) and address counter (DB6 - DB4)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write to data register, and execute internal operation (DR → DD RAM or DR → CG RAM)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read data register and execute internal operation (DD RAM → DR or CG RAM → DR)</td>
</tr>
</tbody>
</table>
Busy Flag (BF)

When the busy flag is set at a logical "1", the LCD unit is executing an internal operation, and no instruction will be accepted. The state of the busy flag is output on data line DB7 in response to the register selection signals RS = 0, R/W = 1 as shown in Table 3. The next instruction may be entered after the busy flag is reset to logical "0".

Address Counter (AC)

The address counter generates the address for the display data RAM and character generator RAM. When the address set instruction is written into the instruction register, the address information is sent to the address counter. The same instruction also determines which of the two RAM's is to be selected.

After data has been written to or read from the display data RAM or character generator RAM, the address counter is automatically incremented or decremented by one. The contents of the address counter are output on data lines DB0 - DB6 in response to the register selection signals RS = 0, R/W = 1 as shown in Table 3.

Display Data RAM (DD RAM)

This 80 x 8 bit RAM stores up to 80 8-bit character codes as display data. The unused area of the RAM may be used by the microprocessor as a general purpose RAM area.

The display data RAM address, set in the address counter, is expressed in hexadecimal (HEX) numbers as follows:

![Hexadecimal Address Format](image)

The address of the display data RAM corresponds to the display position on the LCD panel as follows:

<table>
<thead>
<tr>
<th>Display Position</th>
<th>Digit</th>
<th>Line 1</th>
<th>Line 2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>11</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>13</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

When a display shift takes place, the addresses shift as follows:

- **Left Shift**
  - Line 1: $01_h$, $02_h$, $03_h$, $04_h$, $05_h$, $06_h$, $07_h$, $08_h$, $09_h$, $27_h$, $00_h$
  - Line 2: $41_h$, $42_h$, $43_h$, $44_h$, $45_h$, $46_h$, $47_h$, $48_h$, $49_h$, $67_h$, $40_h$

- **Right Shift**
  - Line 1: $27_h$, $00_h$, $01_h$, $02_h$, $03_h$, $04_h$, $05_h$, $06_h$, $07_h$, $25_h$, $26_h$
  - Line 2: $67_h$, $40_h$, $41_h$, $42_h$, $43_h$, $44_h$, $45_h$, $46_h$, $47_h$, $65_h$, $66_h$

The addresses for the second line are not continuous to the addresses for the first line. A 40-character RAM area is assigned to each of the two line as follows:

- **First Line**
  - Line 1: $00_h$ - $27_h$
  - Line 2: $40_h$ - $67_h$

- **Second Line**
  - Line 1: $00_h$ - $27_h$
  - Line 2: $40_h$ - $67_h$

For an LCD unit with a display capacity of less than 40 characters per line, characters equal in number to the display capacity, as counted from display position 1, are displayed.

b. Address type b . . . .For single-line display with logically dual-line addressing

When a display shift takes place, the addresses shift as follows:

- **Left Shift**
  - Line 1: $01_h$, $02_h$, $03_h$, $04_h$, $05_h$, $06_h$, $07_h$, $27_h$, $41_h$, $42_h$, $43_h$, $44_h$, $45_h$, $46_h$, $47_h$, $48_h$

- **Right Shift**
  - Line 1: $27_h$, $00_h$, $01_h$, $02_h$, $03_h$, $04_h$, $05_h$, $06_h$, $07_h$, $25_h$, $26_h$

The addresses of the second line are not continuous to the addresses of the first line. A 40-character RAM area is assigned to each of the two line as follows:

- **First Line**
  - Line 1: $00_h$ - $27_h$
  - Line 2: $40_h$ - $67_h$

- **Second Line**
  - Line 1: $00_h$ - $27_h$
  - Line 2: $40_h$ - $67_h$

For an LCD unit with a display capacity of less than 40 characters per line, characters equal in number to the display capacity, as counted from display position 1, are displayed.
**Character Generator ROM (CG ROM)**

This ROM generates a 5 x 7 dot-matrix character pattern for each of 160 different 8-bit character codes. The correspondence between character codes and character patterns is shown in Tables 4 and 5. Inquiries are invited for units with custom character patterns.

**Character Generator RAM (CG RAM)**

This RAM stores eight arbitrary 5 x 7 dot-matrix character patterns, as programmed by the user. For displaying a character pattern stored in the CG RAM, a character code corresponding to the left-most column in Tables 4 and 5 is written into the display data RAM.

For the relationship among the CG RAM address, the display data, and the displayed pattern, see Table 6. As shown in Table 6, the unused portion of the CG RAM may be used as a general purpose RAM area.

**Timing Generator**

The timing generator produces timing signals used for the internal operation of the display data RAM, character generator ROM, and character generator RAM. Timing in controlled so that read-out of the RAM for display and access to the RAM by the external microprocessor do not interfere. Display flicker when data is written to the display data RAM is eliminated.

**Cursor/Blink Controller**

This circuit can be used to generate a cursor or blink a character in the display position indicated by the DD RAM address, which is set in the address counter (AC). The following example shows the cursor position when the address counter contains "08" (HEX).

**Parallel-to-Serial Converter**

This circuit converts parallel data read from the CG ROM or CG RAM to serial data for use by the display driver.

**Bias Voltage Generator**

This circuit provides the bias voltage level required for driving the liquid crystal display. Some models incorporate a temperature compensation circuit which generates a temperature dependent bias voltage in order to provide constant display contrast at all ambient temperature levels.

**LCD Driver**

This circuit receives display data, timing signals, and bias voltage, and produces the common and segment display signals.

**LCD Panel**

This is a dot-matrix liquid crystal display panel arranged in either 1 row of 16 characters, 2 rows of 16 characters, 2 rows of 20 characters, or 2 rows of 40 characters.
NOTES:
1. LM16152 incorporates a temperature compensation circuit within the bias voltage generator. See Table 12.
2. For the inverters of EL backlights, please contact your representative.

Figure 1. Functional Block Diagram
### Table 4. Character Codes

<table>
<thead>
<tr>
<th>HIGH-ORDER 4 BIT</th>
<th>LOW-ORDER 4 BIT</th>
<th>0000</th>
<th>0010</th>
<th>0011</th>
<th>0100</th>
<th>0101</th>
<th>0110</th>
<th>0111</th>
<th>1010</th>
<th>1011</th>
<th>1100</th>
<th>1101</th>
<th>1110</th>
<th>1111</th>
</tr>
</thead>
<tbody>
<tr>
<td>xxx0000 CG RAM</td>
<td>(1)</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
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<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td></td>
</tr>
<tr>
<td>xxx0001</td>
<td>(2)</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td>🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉 🎉</td>
<td></td>
</tr>
<tr>
<td>xxx0010</td>
<td>(3)</td>
<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
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<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
<td></td>
</tr>
<tr>
<td>xxx0011</td>
<td>(4)</td>
<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
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<td>￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦ ￦</td>
<td></td>
</tr>
<tr>
<td>xxx0100</td>
<td>(5)</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
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<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td></td>
</tr>
<tr>
<td>xxx0101</td>
<td>(6)</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
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<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td></td>
</tr>
<tr>
<td>xxx0110</td>
<td>(7)</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td></td>
</tr>
<tr>
<td>xxx0111</td>
<td>(8)</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td>☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞ ☞</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. The CG RAM generates character patterns in accordance with the user's program.
2. Shaded areas indicate 5 x 10 dot character patterns.
### Table 5. Character Codes

<table>
<thead>
<tr>
<th>High-Order 4 bit</th>
<th>Low-Order 4 bit</th>
<th>0000</th>
<th>0010</th>
<th>0011</th>
<th>0100</th>
<th>0101</th>
<th>0110</th>
<th>0111</th>
<th>1010</th>
<th>1011</th>
<th>1100</th>
<th>1101</th>
<th>1110</th>
<th>1111</th>
</tr>
</thead>
<tbody>
<tr>
<td>CG RAM (1)</td>
<td></td>
<td>0</td>
<td>@</td>
<td>P</td>
<td>\</td>
<td>p</td>
<td>-</td>
<td>タ</td>
<td>キ</td>
<td>セ</td>
<td>モ</td>
<td>サ</td>
<td>ポ</td>
<td></td>
</tr>
<tr>
<td>(2)</td>
<td></td>
<td>!</td>
<td>1</td>
<td>A</td>
<td>Q</td>
<td>a</td>
<td>q</td>
<td>ア</td>
<td>チ</td>
<td>タ</td>
<td>ム</td>
<td>ア</td>
<td>ク</td>
<td></td>
</tr>
<tr>
<td>(3)</td>
<td></td>
<td>&quot;</td>
<td>2</td>
<td>B</td>
<td>R</td>
<td>b</td>
<td>r</td>
<td>イ</td>
<td>ツ</td>
<td>エ</td>
<td>ヤ</td>
<td>ヒ</td>
<td>ョ</td>
<td></td>
</tr>
<tr>
<td>(4)</td>
<td></td>
<td>#</td>
<td>3</td>
<td>C</td>
<td>S</td>
<td>c</td>
<td>s</td>
<td>ウ</td>
<td>レ</td>
<td>ェ</td>
<td>メ</td>
<td>エ</td>
<td>オ</td>
<td></td>
</tr>
<tr>
<td>(5)</td>
<td></td>
<td>S</td>
<td>4</td>
<td>D</td>
<td>T</td>
<td>d</td>
<td>t</td>
<td>エ</td>
<td>ト</td>
<td>ヤ</td>
<td>マ</td>
<td>オ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(6)</td>
<td></td>
<td>%</td>
<td>5</td>
<td>E</td>
<td>U</td>
<td>e</td>
<td>u</td>
<td>オ</td>
<td>ナ</td>
<td>ウ</td>
<td>オ</td>
<td>ウ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(7)</td>
<td></td>
<td>&amp;</td>
<td>6</td>
<td>F</td>
<td>V</td>
<td>f</td>
<td>v</td>
<td>カ</td>
<td>ニ</td>
<td>ヨ</td>
<td>ピ</td>
<td>ロ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(8)</td>
<td></td>
<td>;</td>
<td>7</td>
<td>G</td>
<td>W</td>
<td>g</td>
<td>w</td>
<td>キ</td>
<td>ヌ</td>
<td>ラ</td>
<td>キ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(9)</td>
<td></td>
<td>)</td>
<td>8</td>
<td>H</td>
<td>X</td>
<td>h</td>
<td>x</td>
<td>イ</td>
<td>ネ</td>
<td>ト</td>
<td>ユ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(10)</td>
<td></td>
<td>(</td>
<td>9</td>
<td>I</td>
<td>Y</td>
<td>i</td>
<td>y</td>
<td>ケ</td>
<td>ノ</td>
<td>オ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(11)</td>
<td></td>
<td>*</td>
<td>10</td>
<td>J</td>
<td>Z</td>
<td>j</td>
<td>z</td>
<td>コ</td>
<td>ハ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(12)</td>
<td></td>
<td>+</td>
<td>11</td>
<td>K</td>
<td>[</td>
<td>k</td>
<td>]</td>
<td>ヒ</td>
<td>ロ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(13)</td>
<td></td>
<td>,</td>
<td>12</td>
<td>L</td>
<td>¥</td>
<td>l</td>
<td></td>
<td></td>
<td>シ</td>
<td>フ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(14)</td>
<td></td>
<td>-</td>
<td>13</td>
<td>M</td>
<td>]</td>
<td>m</td>
<td>]</td>
<td>ス</td>
<td>ヘ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(15)</td>
<td></td>
<td></td>
<td>14</td>
<td>N</td>
<td>^</td>
<td>n</td>
<td>→</td>
<td>セ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(16)</td>
<td></td>
<td>/</td>
<td>15</td>
<td>O</td>
<td>_</td>
<td>o</td>
<td>←</td>
<td>ソ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(17)</td>
<td></td>
<td>?</td>
<td>16</td>
<td>_</td>
<td>O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The character codes are for Dot-Matrix LCD units.
### Table 6. Relationship Among Character Code (DD RAM), CG RAM Address, and Character Pattern (CG RAM)

<table>
<thead>
<tr>
<th>Character Code (DD RAM Data)</th>
<th>CG RAM Address</th>
<th>Character Pattern (CG RAM Data)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 6 5 4 3 2 1 0</td>
<td>5 4 3 2 1 0</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>High-order bit</td>
<td>Low-order bit</td>
<td>High-order bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low-order bit</td>
</tr>
<tr>
<td>0 0 0 0 * 0 0 0</td>
<td>0 0 0 0 1</td>
<td>0 0 0 0 * 0 0 1</td>
</tr>
<tr>
<td></td>
<td>1 1 1 1 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 0 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 1</td>
<td></td>
</tr>
</tbody>
</table>

#### Sample Character Pattern (1)

- Cursor Position

#### Sample Character Pattern (2)

- Cursor Position

#### NOTES:

1. Character code bits 0 - 2 correspond to CG RAM address bits 3 - 5. Each of the 8 unique bit strings designates one of the 8 character patterns.
2. CG RAM address bits 0 - 2 designate the row position of each character pattern. The 8th row is the cursor position. CG RAM data in the 8th row is OR'ed with the display cursor. Any ‘1’ bits in the 8th row will result in a displayed dot regardless of the cursor status (ON/OFF). Accordingly, if the cursor is to be used, CG RAM data for the 8th row should be set to ‘0’.
3. CG RAM data bits 0 - 4 correspond to the column position of each character pattern bit 4 corresponding to the left most column of the character pattern. CG RAM data bits 5 - 7 are not used for displaying character patterns, but may be used as a general purpose RAM area.
4. As shown in tables 4 and 5, character patterns in the CG RAM are accessed by character codes with bits 4 - 7 equal to ‘0’. For example, the character pattern 'R', shown in the first sample character pattern of the table, is selected by the character code ‘00’ (HEX) or ‘08’ (HEX), since bit 3 of the character code is a ‘don’t care’ bit (i.e., can take either value, ‘00’ or ‘1’).
5. CG RAM data ‘1’ produces a dark dot, and data ‘0’ produces a light dot in the corresponding position on the display panel.
6. * = Signifies a “don’t care” bit
Microprocessor Interface

The LCD unit performs either dual 4-bit or single 8-bit data transfers, allowing the user to interface with either a 4-bit or 8-bit microprocessor.

4-Bit Microprocessor Interface.

Data lines DB4 - DB7 are used for data transfers. Data transactions with the external microprocessor take place in two 4-bit data transfer operations.

8-bit Microprocessor Interface

Each 8-bit piece of data is transferred in a single operation using the entire data bus DB0 - DB7.

![4-Bit Data Transfer Diagram](image-url)
**Reset Function**

*Initialization by Internal Reset Circuit*

The LCD unit has an internal reset circuit for implementing an automatic reset operation at power-on. During the initialization operation, the busy flag is set. The busy state lasts for 10 msec after VDD reaches 4.5 V. The following instructions are executed in initializing the LCD unit.

1. Clear Display

2. Function Set
   - DL = 1 . . . . 8-bit data length for interface
   - N = 0 . . . . Single-line display
   - F = 0 . . . . 5 × 7 dot-matrix character font

3. Display ON/OFF Control
   - D = 0 . . . . Display OFF
   - C = 0 . . . . Cursor OFF
   - B = 0 . . . . Blink function OFF

4. Entry Mode Set
   - I/D = 1 . . . . Increment Mode
   - S = 0 . . . . Display shift OFF

**CAUTION**

If the power conditions stated in Table 11, "Power conditions applicable when internal reset circuit is used," are not satisfied, then internal reset circuit will not operate properly and the LCD unit will not be initialized. In this case, the initialization procedure must be executed by the external microprocessor.
Initialization by Instructions

If the power conditions for the normal operation of the internal reset circuit are not satisfied (see Table 11), then LCD unit must be initialized by executing a series of instructions. The procedure for this initialization process is as follows:

![Flowchart showing the initialization process]

- Power ON
  - Wait 15 ms or more after VDD reaches 4.5 V
  - \[ \text{RS R/W DB}_7 \text{ DB}_6 \text{ DB}_5 \text{ DB}_4 \text{ DB}_3 \text{ DB}_2 \text{ DB}_1 \text{ DB}_0 \]
    \[ \begin{array}{ccccccccc}
    0 & 0 & 0 & 0 & 1 & 1 & \ast & \ast & \ast \\
    \end{array} \]
  - Busy flag can’t be checked before execution of this instruction
  - Function Set (8-Bit Interface)

- Wait 4.1 ms or more
  - \[ \text{RS R/W DB}_7 \text{ DB}_6 \text{ DB}_5 \text{ DB}_4 \text{ DB}_3 \text{ DB}_2 \text{ DB}_1 \text{ DB}_0 \]
    \[ \begin{array}{ccccccccc}
    0 & 0 & 0 & 0 & 1 & 1 & \ast & \ast & \ast \\
    \end{array} \]
  - Busy flag can’t be checked before execution of this instruction
  - Function Set (8-Bit Interface)

- Wait 100 µs or more
  - \[ \text{RS R/W DB}_7 \text{ DB}_6 \text{ DB}_5 \text{ DB}_4 \text{ DB}_3 \text{ DB}_2 \text{ DB}_1 \text{ DB}_0 \]
    \[ \begin{array}{ccccccccc}
    0 & 0 & 0 & 0 & 1 & 1 & \ast & \ast & \ast \\
    \end{array} \]
  - Busy flag can’t be checked before execution of this instruction
  - Function Set (8-Bit Interface)

- Busy flag can be checked after the following instructions are completed. If the busy flag is not going to be checked, then a wait time longer than the total execution time of these instructions is required (See Table 7.)
  - \[ \text{RS R/W DB}_7 \text{ DB}_6 \text{ DB}_5 \text{ DB}_4 \text{ DB}_3 \text{ DB}_2 \text{ DB}_1 \text{ DB}_0 \]
    \[ \begin{array}{ccccccccc}
    0 & 0 & 0 & 0 & 1 & 1 & N & F & \ast \\
    0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
    0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
    0 & 0 & 0 & 0 & 0 & 0 & 1 & I/D & S \\
    \end{array} \]
  - Function Set (8-Bit Interface, Single/Dual Line Display, Display Font)
  - Display Off
  - Display Clear
  - Entry Mode Set

Caution: At this point, the display format can’t be changed.

Figure 3. 8-Bit Interface
4-Bit Interface

![Figure 4. 4-Bit Interface](image-url)

- **Power ON**: Wait 15 ms or more after \(V_{DD}\) reaches 4.5 V.
- **RS R/W DB\(_7\) DB\(_6\) DB\(_5\) DB\(_4\)**
  - \(0 0 0 0 1 1\)
- **Wait 4.1 ms or more**
- **RS R/W DB\(_7\) DB\(_6\) DB\(_5\) DB\(_4\)**
  - \(0 0 0 0 1 1\)
- **Wait 100 \(\mu\)s or more**
- **RS R/W DB\(_7\) DB\(_6\) DB\(_5\) DB\(_4\)**
  - \(0 0 0 0 1 1\)
- **Busy flag can't be checked before execution of this instruction**
- **Function Set (8-Bit Interface)**
- **Busy flag can't be checked before execution of this instruction**
- **Function Set (8-Bit Interface)**
- **Busy flag can't be checked before execution of this instruction**
- **Function Set (8-Bit Interface)**

- **(a) Busy flag can be checked after the following instructions are completed. If the busy flag is not going to be checked, then a wait time longer than the total execution time of these instructions is required (See Table 7.)**

- **I Function Set (4-Bit Interface)**
  - This instruction signals the LCD unit to begin accepting and sending data in dual 4-bit transfers for all subsequent transfers for all subsequent transactions. This is the only 4-bit instruction recognized by the LCD unit.

- **II Function Set**
  - 4-Bit Interface, Single/Dual Line
  - Display, Display Font

- **Caution: At this point, the display format can't be changed.**

- **III Display Off**
  - Single/Dual Line

- **Display Font**

- **IV Display Clear**

- **V Entry Mode Set**

End of Initialization
INSTRUCTIONS

General Information

When the LCD unit is controlled by an external microprocessor, the only registers which can be directly accessed by the microprocessor are the instruction register (IR) and data register (DR). Control information is buffered to allow the LCD unit to interface with various microprocessors and peripheral control devices with different operating speeds. The internal operation of the LCD unit is determined by the signals sent from the external microprocessor. These signals include the register select (RS) signal, the read/write (R/W) signal, and the data bus (DB0 - DB7) signals.

Table 7 lists the instructions available to the LCD unit, with their execution times. The instructions fall into the following four categories.

1. Instructions for setting LCD unit functions, such as display format and data length
2. Instructions for addressing the internal RAM's
3. Instructions for transferring data to or from the internal RAM's
4. Other instructions

In normal operation, instructions from category (3) are used most frequently. The internal RAM address may be incremented or decremented automatically after each data transaction, to reduce the programming requirements of the microprocessor. The display may also be shifted automatically after each display data write (see Sample Instruction Procedures section for examples). These features facilitate the construction of efficient systems.

During the internal execution of an instruction, no instruction other than the "busy flag/address counter read" instruction will be accepted. During internal operation the busy flag is set to "1". It is necessary for the microprocessor to check that the busy flag is reset to "0" before sending the next instruction.

NOTE

Either the microprocessor must check that the busy flag is not set to "1" before sending each instruction, or the interval waited before sending each instruction must be made sufficiently longer than the execution time of the previous instruction. For the execution time of each instruction, see Table 7.

Description of Instruction

Display Clear

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0000 000 0 1</td>
</tr>
</tbody>
</table>

The display data RAM is filled with the "space" code, 20H. The address counter is reset to zero. If the display has been shifted, the original position is restored. By execution of this instruction, the display goes off, and the cursor and character blink functions, if activated, are moved to the upper, leftmost display position.

Display/Cursor Home

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0000 000 0 0</td>
</tr>
</tbody>
</table>

The address counter is reset to zero. If the display has been shifted, the original position is restored. The content of the DD RAM is not affected. The cursor and character blink functions, if activated, are moved to the upper, leftmost display position.

Entry Mode Set

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB5</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0000 000 0 0</td>
</tr>
</tbody>
</table>

I/D: The address counter is incremented (I/D = 1) or decremented (I/D = 0) by one, following the reading or writing of each display data RAM character code. The cursor and character blink functions move one display position to the right (I/D = 1) or left (I/D = 0). The same operation takes place when data is written to or read from the character generator RAM.

S: When S = 1, the entire display is shifted one position to the left (I/D = 1) or right (I/D = 0) following the writing of a display data RAM character code. The cursor and character blink functions do not move relative to the display position. When S = 0, the display is not shifted. The display is not shifted when writing data to the character generator RAM.
Display ON/OFF

D: When D = 1, the display is turned on. When D = 0, the display is turned off with the display data retained in the display data RAM.

C: When C = 1, the cursor is displayed in the position specified by the address counter. When C = 0, the cursor is not displayed. The cursor is made up of five dots displayed across the 8th display row, below the 5 x 7 dot-matrix character block. For 5 x 10 dot-matrix character blocks, 5 dots are displayed across the 11th row.

B: When B = 1, the character at the cursor position blinks on and off. When this function is activated, at fCP or fosc = 250 kHz, alternating between all dots black, and the display character, the character is alternately displayed for 409.6 ms and blanked for 409.6 ms. The cursor may be used simultaneously with the character blink function. (Blink frequency varies in proportion to the reciprocal of fCP or fOSC. 409.6 x 250/270 = 379.2 ms; fCP = 270 kHz.)

Display/Cursor Shift

The display and/or cursor are shifted to the right or left. For two-line displays, the cursor moves from the 40th position of the top line to the first position of the second line. From the 40th position of the second line, the cursor does not move back to the home position, but rather to the first position of the second line.

Function Set

DL: Selects the interface data length. When DL = 1, 8-bit data transfers are used. When DL = 0, 4-bit data transfers are used.

N: Selects display format (single or dual line). See Table 12 for the correct input value for each model.

CAUTION

The function set instruction must be executed at the beginning of the microprocessor program, before all other instructions except the busy flag/address counter read instruction. The function set instruction cannot be executed again except to change the interface data length. Once set, the display format cannot be changed.
**CG RAM Address Set**

<table>
<thead>
<tr>
<th>RS/R/W DB7</th>
<th>A A A A A A A A</th>
</tr>
</thead>
</table>

The address counter is loaded with a character generator RAM address, expressed as a 6-digit binary number. Following the execution of this instruction, subsequent data transactions will be between the external microprocessor and the character generator RAM.

**DD RAM Address Set**

<table>
<thead>
<tr>
<th>RS/R/W DB7</th>
<th>A A A A A A A A</th>
</tr>
</thead>
</table>

The address counter is loaded with a display data RAM address, expressed as a 7-digit binary number. Following the execution of this instruction, subsequent data transactions will be between the external microprocessor and the display data RAM. For N = 0 (single line display), the binary number, ADD may have a value ranging from 00H to 4FH. For N = 1 (dual line display), the binary number, ADD, may have a value ranging from 00H to 27H for the first line, or 40H to 67H for the second line.

**Busy Flag/Address Counter Read**

<table>
<thead>
<tr>
<th>RS/R/W DB7</th>
<th>A A A A A A A A</th>
</tr>
</thead>
</table>

The busy flag (BF) is read out, and indicates whether or not the LCD unit is still executing the previous instruction. BF = 1 indicates the busy state (internal operation), and the next instruction will not be accepted until BF = 0. This instruction also reads out the contents of the address counter, expressed as a 7-digit binary number. The address counter is used for accessing both the character generator RAM and the display data RAM. On read-out, the address counter will contain either a character generator RAM address or a display data RAM address, as determined by the most recently executed address set instruction.

**CG RAM/DD RAM Data Write**

<table>
<thead>
<tr>
<th>RS/R/W DB7</th>
<th>D D D D D D D D D D</th>
</tr>
</thead>
</table>

An 8-bit data word is written into either the character generator RAM or display data RAM, as determined by the most recently executed address set instruction. The data is written into the RAM location specified by the address counter. After the data is written into the RAM, the address counter is either incremented or decremented by one, as determined by the current entry mode. A display shift may also take place after the data is written.

**CG RAM/DD RAM Data Read**

<table>
<thead>
<tr>
<th>RS/R/W DB7</th>
<th>D D D D D D D D D D</th>
</tr>
</thead>
</table>

An 8-bit data word is read from either the character generator RAM or display data RAM, as determined by a previously executed address set instruction. The data is read from the RAM location specified by the address counter. This instruction must be immediately preceded by the CG RAM address set instruction, the DD RAM address set instruction, the cursor shift instruction, or a previous CG RAM/DD RAM data read instruction. Any other preceding instruction will cause invalid data to be read. The address set instructions cause the address counter to be loaded with a valid data read address.

The cursor shift command allows selected DD RAM data to be read without the necessity of resetting the DD RAM address. Following the cursor shift instruction, the CG RAM/DD RAM data read instruction will read data from the DD RAM.

After the execution of each data read instruction, the address counter is either incremented or decremented by one, as determined by the current entry mode. It is not necessary to reset the RAM address before the execution of subsequent data read instructions if the same RAM is to be read. The display is not shifted by the data read instruction.

**NOTE**

After the execution of the CG RAM/DD RAM data write instruction, the address counter is incremented or decremented automatically. However, the contents of the RAM location specified by the address counter cannot be read by a subsequent CG RAM/DD RAM data read instruction. The correct procedure for reading data from the CG RAM or DD RAM is to execute an address set or cursor shift instruction. Once a data read instruction has been executed, successive data read instructions may be executed, with no requirement for intervening instructions.
Table 7. Instruction Set

<table>
<thead>
<tr>
<th>INSTRUCTION</th>
<th>CODE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display Clear</td>
<td></td>
<td>Clear entire display area, restore display from shift, and load address counter with DD RAM address 00H.</td>
</tr>
<tr>
<td>Display/Cursor Home</td>
<td></td>
<td>Restore display from shift and load address counter with DD RAM address 00H.</td>
</tr>
<tr>
<td>Entity Mode Set</td>
<td></td>
<td>Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.</td>
</tr>
<tr>
<td>Display ON/OFF</td>
<td></td>
<td>Specify active bit of display (D), cursor (C), and blinking of character at cursor position (B).</td>
</tr>
<tr>
<td>Display/Cursor Shift</td>
<td></td>
<td>Shift display or move cursor.</td>
</tr>
<tr>
<td>Function Set</td>
<td></td>
<td>Set interface data length (DL) and number of display lines (N).</td>
</tr>
<tr>
<td>CG RAM Address Set</td>
<td></td>
<td>Load the address counter with a CG RAM address. Subsequent data is CG RAM data.</td>
</tr>
<tr>
<td>DD RAM Address Set</td>
<td></td>
<td>Load the address counter with a DD RAM address. Subsequent data is DD RAM data.</td>
</tr>
<tr>
<td>Busy Flag Address Counter Read</td>
<td></td>
<td>Read busy flag (BF) and contents of address counter (AC).</td>
</tr>
<tr>
<td>CG RAM/DD RAM Data Read</td>
<td></td>
<td>Write data Read data from CG RAM or DD RAM.</td>
</tr>
<tr>
<td>CG RAM/DD RAM Data Write</td>
<td></td>
<td>Write data to CG RAM or DD RAM.</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Symbol "*" signifies a "don't care" bit.
2. Correct input value for "N" is predetermined for each model (see Table 12).
ELECTRICAL CHARACTERISTICS

Absolue Maximum Ratings

See the device specifications for each LCD unit model.

Electrical Characteristics

See the device specifications for each LCD unit model. Some of the currently available specifications do not describe the test conditions for the high-level and low-level output voltages. These conditions are as follows:

Timing Characteristics

![Timing Characteristics Diagram]

Figure 5. Write Operation Timing Diagram
(For data sent from the external microprocessor to the LCD unit)

Table 9. Write Operation Timing Characteristics
(V_{DD} = 5.0 \pm 5\%, V_{SS} = 0 V, T_A = 0 \sim 50^\circ C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable Cycle Time</td>
<td>t_{CYC E}</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td>Enable Pulse Width</td>
<td><em>High Level</em> t_{PW EH}</td>
<td>450</td>
<td>ns</td>
</tr>
<tr>
<td>Enable Rise/Fall Time</td>
<td>t_{ER, TF}</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time</td>
<td>RS, RW-E t_{AS}</td>
<td>140</td>
<td>ns</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>t_{AH}</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>t_{DSW}</td>
<td>195</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>t_{H}</td>
<td>10</td>
<td>ns</td>
</tr>
</tbody>
</table>
If the above conditions are not satisfied, the internal reset circuit will not operate normally. In such a case, the LCD unit must be initialized by executing a series of instructions (see the Execution by Instructions section).

### Table 10. Read Operation Timing Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable Cycle Time</td>
<td>$t_{qE}$</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td>Enable Pulse Width</td>
<td>PW$_{EH}$</td>
<td>450</td>
<td>ns</td>
</tr>
<tr>
<td>Enable Rise/Fall Time</td>
<td>$t_{EF}$</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time</td>
<td>RS, RW-E</td>
<td>$t_{AS}$</td>
<td>140</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>$t_{AH}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Data Delay Time</td>
<td>$t_{DDR}$</td>
<td>320</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>$t_{OHR}$</td>
<td>20</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Table 11. Power Conditions for Internal Reset**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Build-Up Time</td>
<td>$t_{BC}$</td>
<td>0.1</td>
<td>10 ms</td>
</tr>
<tr>
<td>Power-Off Period</td>
<td>$t_{OFF}$</td>
<td>1</td>
<td>ms</td>
</tr>
</tbody>
</table>

If the above conditions are not satisfied, the internal reset circuit will not operate normally. In such a case, the LCD unit must be initialized by executing a series of instructions (see the Execution by Instructions section).

**Figure 6. Read Operation Timing Diagram**

(For data sent from the LCD unit to the external microprocessor)

**Figure 7.**

**Figure 7.**

**NOTE:** *$t_{OFF}$ indicates Power-off Period.*
LCD UNIT USAGE INSTRUCTIONS

Interface with External Microprocessor

1. 8-bit Microprocessor

![Diagram of 8-bit Interface Timing](image1)

**Figure 8. 8-Bit Interface Timing (Example)**

a. Interface to 8-Bit Microprocessor via Peripheral Interface Adaptor (PIA). The following exemplifies the connection of the LCD unit to an 8-bit microprocessor chip through a PIA or I/O port. The interface is TTL compatible. PB₀ – PB₇ of the interface device are connected to DB₀ – DB₇ of the LCD unit, and PA₀ – PA₂ are connected to E, R/W, and RS respectively.

When the PIA is used, care must be taken to insure the proper relationship between the E signal and other signals when reading and writing data.
b. Direct Connection to 8-Bit Microprocessor

![Diagram](image)

VMA
Φ2
A15
A0
R/W
D0 - D7

MC6800

E
RS
R/W
DB0 - DB7

LCD UNIT

---

c. Interface with MC6805 Microprocessor

![Diagram](image)

A0 - A7

MC6805

C0
C1
C2

E
RS
R/W

DB0 - DB7

LCD UNIT

d. Interface with Z-80 Microprocessor

![Diagram](image)

D0 - D7

A0
A4
A5
A6
A7

MI

Z80

IORQ
RD

A
B
C
G1A
G2A
G2B

1 KΩ

200 pF

LS138

E

RS

DB0 - DB7

LCD UNIT

R/W
2. 4-Bit Data Transfer with a Single-Line, 16-Character Display (Using Internal Reset). Table 14 shows a sample operating procedure for an LCD unit in this mode. After power has been turned on, the 8-bit data transfer mode is in effect, and the first write operation is assumed to be an 8-bit data transfer. Since the data lines DB₀ - DB₃ are not connected, this data is not accepted and must be written again (i.e. the function set instruction must be written twice). Subsequent data transfers are completed in two 4-bit transfer operations (see Table 14).

![Figure 9. 4-Bit Interface Timing (Example)](image)

**Figure 9. 4-Bit Interface Timing (Example)**

![Figure 10. Connection to SM200](image)

**Figure 10. Connection to SM200**
Contrast Control Voltage

The LCD unit has three power terminals, $V_{DD}$, $V_{SS}$, and $V_O$. A contrast control voltage is supplied to the terminal $V_O$. The panel is driven by the voltage difference between $V_{DD}$ and $V_O$ (i.e., $V_{DD} - V_O$). Figure 11 shows an example of the contrast control voltage supply circuit, in which $VR$ is adjusted to obtain the best display quality.

![Figure 11. Contrast Adjustment Circuit](image)

Sample Instruction Procedures

1. 8-Bit Data Transfer with a Single-Line, 16-Character Display (Using Internal Reset).

   Table 13 shows a sample operating procedure for an LCD unit in this mode. Initially, the function of the LCD unit must be selected by executing the function set instruction. Up to 80 characters may be stored in the display data RAM, and may be displayed by using the display shift operation. The contents of the display data RAM are not affected by the display shift operation, and the display/cursor home instruction enables the restoration of the initial display position.

2. 4-Bit Microprocessor

   The LCD unit can be connected to the I/O port of a 4-bit microprocessor. If the I/O port is not limited, 8-bit data may be transferred between the devices. Otherwise, 4-bit split data may be transferred in two operations, after selecting the 4-bit data length function. For the timing waveform, see Figure 9. Figure 10 shows a sample connection to an SM-200 microprocessor. It should be noted that the busy flag check requires a two-step operation.

3. 8-Bit Data Transfer with a Dual-Line, 16-Character Display (Using Internal Reset).

   Table 15 shows a sample operating procedure for an LCD unit in this mode. The cursor is automatically moved from the first line to the second line after column 40 of the first line has been written. In the example (Table 15), where only 16 characters are displayed on each line, the display data RAM address must be reset after the 16th character has been written. When a display shift is executed, both lines are shifted simultaneously. When the display shift operation is repeated, characters on one line are not moved to the other line, but rather are looped back onto the same line.

   **NOTE**

   To use the internal reset function, the power conditions must be satisfied. Otherwise, the LCD unit must be initialized by the execution of a series of instructions, as shown in the Initialization by Instructions section.
<table>
<thead>
<tr>
<th>NO.</th>
<th>INSTRUCTION</th>
<th>DISPLAY</th>
<th>OPERATION</th>
</tr>
</thead>
</table>
| 1   | Power ON  
    (Internal reset circuit is triggered) |         | The LCD unit is initialized. No display. |
| 2   | Function Set  
    DS RW DBy - DBx  
    000001100** |         | Set for 8-bit data transfer and address type a. |
| 3   | Display ON/OFF  
    000000011110 |         | Turn on the display and cursor. After initialization, the DD RAM is filled with the "space" code. |
| 4   | Entry Mode Set  
    00000001110 |         | Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift. |
| 5   | CG RAM/DD RAM  
    Data Write  
    1001010011 | S       | Write "S" into the DD RAM. The cursor shifts to the right. |
| 6   | CG RAM/DD RAM  
    Data Write  
    1001001001 | SH      | Write "H" into the DD RAM. |
| 7   |            |         |            |
| 8   | CG RAM/DD RAM  
    Data Write  
    1000100000 | SHARP LCD UNIT | Write "space" into the DD RAM. |
| 9   | Entry Mode Set  
    00000001111 |         | Set display to shift after each data write. |
| 10  | CG RAM/DD RAM  
    Data Write  
    1001001100 | HARP LCD UNIT L_ | Write "L" into the DD RAM. |
| 11  |            |         |            |
| 12  | CG RAM/DD RAM  
    Data Write  
    1000110001 | LCD UNIT LM171_ | Write "1" into the DD RAM. |
| 13  | Display/Cursor Shift  
    00000100** | LCD UNIT LM171_ | Shift the cursor to the left. |
| 14  | Display/Cursor Shift  
    00000100** | LCD UNIT LM171_ | Shift the cursor to the left. |
| 15  | CG RAM/DD RAM  
    Data Write  
    1000110110 | LCD UNIT LM161_ | Write "0" into the DD RAM. |
| 16  | Display/Cursor Shift  
    00000111** | LCD UNIT L161_ | Shift the display and cursor to the right. |
| 17  | Display/Cursor Shift  
    00000101** | LCD UNIT LM161_ | Shift the cursor to the right. |
| 18  | CG RAM/DD RAM  
    Data Write  
    1000110101 | LCD UNIT L1615_ | Write "5" into the DD RAM. |
| 19  |            |         |            |
| 20  | Display/Cursor Home  
    0000000010 | SHARP LCD UNIT L_ | Restore the display and cursor to their initial positions. |
### Table 14. 4-Bit Data Transfer with Single Line
(16-Character Display (*Using Internal Reset*))

<table>
<thead>
<tr>
<th>NO.</th>
<th>INSTRUCTION</th>
<th>DISPLAY</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power On (Internal reset circuit triggered)</td>
<td></td>
<td>The LCD unit is initialized. No display.</td>
</tr>
<tr>
<td>2</td>
<td>Function Set</td>
<td></td>
<td>Set for 4-bit data transfer. This instruction is transferred in a single operation since up to this point the LCD unit is in the 8-bit mode.</td>
</tr>
<tr>
<td>3</td>
<td>Function Set</td>
<td></td>
<td>Set for 4-bit data transfer and address type C. Data is transferred in two operations.</td>
</tr>
<tr>
<td>4</td>
<td>Display On/Off</td>
<td></td>
<td>Turn on the display and cursor. After initialization, the DD RAM is filled with the &quot;space&quot; code.</td>
</tr>
<tr>
<td>5</td>
<td>Entry Mode Set</td>
<td></td>
<td>Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.</td>
</tr>
<tr>
<td>6</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;S&quot; into the DD RAM. The cursor shifts to the right.</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;P&quot; into the DD RAM.</td>
</tr>
<tr>
<td>9</td>
<td>DD RAM Address Set</td>
<td></td>
<td>Set DD RAM address to the first position on the right half of the display (character position 9).</td>
</tr>
<tr>
<td>10</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;L&quot; into the DD RAM.</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;space&quot; into the DD RAM.</td>
</tr>
<tr>
<td>13</td>
<td>Entry Mode Set</td>
<td></td>
<td>Set the display to shift after each data write.</td>
</tr>
<tr>
<td>14</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;U&quot; into the DD RAM. Right and left halves of display shift left one character.</td>
</tr>
<tr>
<td>15</td>
<td>Entry Mode Set</td>
<td></td>
<td>Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.</td>
</tr>
<tr>
<td>16</td>
<td>DD RAM Address Set</td>
<td></td>
<td>Set DD RAM address to the 9th position on the left half of the display (address 08h)</td>
</tr>
<tr>
<td>17</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;L&quot; into the DD RAM.</td>
</tr>
<tr>
<td>18</td>
<td>DD RAM Address Set</td>
<td></td>
<td>Set DD RAM address to the 6th position on the right half of the display (address 45h)</td>
</tr>
<tr>
<td>19</td>
<td>Entry Mode Set</td>
<td></td>
<td>Set the display to shift after each data writer.</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>CG RAM DDR RAM Data Write</td>
<td></td>
<td>Write &quot;T&quot; into the DD RAM.</td>
</tr>
<tr>
<td>22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Display/Cursor Home</td>
<td></td>
<td>Restore the display and cursor to their initial positions.</td>
</tr>
</tbody>
</table>
### Table 15. 8-Bit Data Transfer with Dual-Line

(16-Character Display (Using Internal Reset))

<table>
<thead>
<tr>
<th>NO.</th>
<th>INSTRUCTION</th>
<th>DISPLAY</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power ON (Internal reset circuit is triggered).</td>
<td></td>
<td>The LCD unit is initialized. No display.</td>
</tr>
<tr>
<td>2</td>
<td>Fact b Set DD RW DB7 - DB0 00001110**</td>
<td></td>
<td>Set for 8-bit data transfer and address type b.</td>
</tr>
<tr>
<td>3</td>
<td>Display On/OFF 0000001110</td>
<td></td>
<td>Turn on the display and cursor. After initialization, the DD RAM is filled with the &quot;space&quot; code.</td>
</tr>
<tr>
<td>4</td>
<td>Entry Mode Set 0000000110</td>
<td></td>
<td>Set the LCD unit to increment the address counter and shift the cursor to the right after each data transaction. The display does not shift.</td>
</tr>
<tr>
<td>5</td>
<td>CG RAM/DD RAM Data Write 1001010011</td>
<td>S</td>
<td>Write &quot;S&quot; into the DD RAM. The cursor shifts to the right.</td>
</tr>
<tr>
<td>7</td>
<td>CG RAM/DD RAM Data Write 1000100000</td>
<td>SHARP LCD UNIT</td>
<td>Write &quot;space&quot; into the DD RAM.</td>
</tr>
<tr>
<td>8</td>
<td>DD RAM Address Set 0011000000</td>
<td>SHARP LCD UNIT</td>
<td>Set DD RAM address to the first position of the second line.</td>
</tr>
<tr>
<td>9</td>
<td>CG RAM/DD RAM Data Write 1001001100</td>
<td>SHARP LCD UNIT L</td>
<td>Write &quot;L&quot; into the DD RAM.</td>
</tr>
<tr>
<td>11</td>
<td>CG RAM/DD RAM Data Write 1001000001</td>
<td>SHARP LCD UNIT LM16251 : 16CHA</td>
<td>Write &quot;A&quot; into the DD RAM.</td>
</tr>
<tr>
<td>12</td>
<td>Entry Mode Set 0000001111</td>
<td>SHARP LCD UNIT LM16251 : 16CHA</td>
<td>Set the display to shift after each data write.</td>
</tr>
<tr>
<td>13</td>
<td>CG RAM/DD RAM Data Write 1001011001</td>
<td>SHARP LCD UNIT M16251 : 16CHAR</td>
<td>Write &quot;R&quot; into the DD RAM. Both lines shift to the left.</td>
</tr>
<tr>
<td>14</td>
<td>: : : :</td>
<td></td>
<td>: : : :</td>
</tr>
<tr>
<td>15</td>
<td>Display/Cursor Home 0000000010</td>
<td>SHARP LCD UNIT M16251 : 16CHAR</td>
<td>Restore the display and cursor to their initial positions.</td>
</tr>
</tbody>
</table>
HANDLING INSTRUCTIONS

1. Operate the LCD unit within the allowable ranges of temperature and power supply voltage. Avoid operating the LCD unit in high humidity. Avoid operating the LCD unit for extended periods under direct sunlight.

2. Mechanical shock and pressure on the glass LCD panel should be avoided. Care must be taken to insure that no torsional or compressive forces are applied to the LCD unit when it is mounted. If leakage of the liquid crystal material should occur, all contact with the material, particularly accidental ingestion, must be avoided. If the body or clothing become contaminated by the liquid crystal material, wash thoroughly with water and soap.

3. The reflector and polarizers attached to the LCD unit are made of soft materials. Care must be taken not to scratch these materials. To clean the display, use a soft, dry cloth. Do not use organic solvents or water. If dirt cannot be removed by this method, a small amount of petroleum benzine may be used.

4. The LCD unit uses CMOS LSI’s. Precautions must be taken to protect the unit from electrostatic charges.

5. Do not apply the power supply voltages to the LCD unit while the input signal terminals are open. Also, it is better if the input signal and LCD unit power supply voltages are switched on and off simultaneously.

6. The LCD unit should be stored in its original packing case at a temperature of 0 to 35°C and at a relative humidity of 60% or less. The LCD unit should be stored in a dark place, not exposed to direct sunlight or fluorescent lamps.

7. The following precautions should be taken when mounting the LCD unit.

   a. The LCD unit may be mounted on either the inside or outside of a cabinet, as shown in Figure 12. To determine the optimum mounting angle, refer to the viewing angle range in the device specification for each model.

b. An acrylic sheet, or the like, may be used to protect the LCD panel. A spacing of 0.5 mm to 1.0 mm should be used between the protective plate and the LCD panel. (See Figure 13.) To prevent stress on the LCD panel, the unit should be mounted with a nominal height accuracy of ±0.1 mm.

c. An anti-glare (anti-reflection) sheet may be used in place of the protective acrylic sheet. The mounting considerations will be the same.
OPERATING RESTRICTIONS

The LSI (HD44780AXX) used in the LCD units is reported to have the following defects:

HD44780AXX Defective Functions
1. When the display clear or display/cursor home instruction is executed when the display has been shifted from its original position, original display position may not be restored.
2. When the display/cursor home instruction is executed, the data in the following display data RAM locations may be lost.

To counteract these defects, the following restrictions should be followed (Table 16).

In the production facility, the LSI device in question is now being replaced with a modified version, HD44780RAXX. The above mentioned restrictions do not apply to products using the "RA" version of the LSI. The "RA" version devices have an "R" printed in the upper, right corner, as shown.

<table>
<thead>
<tr>
<th>A. Address type a.</th>
<th>Address HEX</th>
<th>00 01 02 03 04 05 06 07 - - - - - - 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F</th>
</tr>
</thead>
</table>

Total: 80 Characters

The contents of addresses (43), (47), (4B), and (4F) may be destroyed.

<table>
<thead>
<tr>
<th>B. Address type b and c.</th>
<th>Address HEX</th>
<th>00 01 02 03 04 05 06 07 - - - - - - 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Address HEX</td>
<td>40 41 42 43 44 45 46 47 - - - - - - 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67</td>
</tr>
</tbody>
</table>

Total: 40 Characters x 2 Lines

The contents of address locations 23, 27, 63, and 67 may be lost during the execution of the display/cursor home instruction.

NOTE: Although address type C is for a single-line display its address structure is logically the same as for address type b.

Table 16.

<table>
<thead>
<tr>
<th>NO.</th>
<th>OPERATION</th>
<th>RESTRICTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Execution of the display clear or display/cursor home instruction when the display has been shifted from its original position.</td>
<td>The display/cursor home instruction should be executed after the defective instruction, but after a time interval not equal to any multiple of 400 fosc (kHz) seconds. Since fosc = 250 kHz, the following timing intervals should be avoided: 1.6 seconds, 3.2 seconds, 4.8 seconds, etc.</td>
</tr>
<tr>
<td>2</td>
<td>Execution of the display/cursor home instruction.</td>
<td>Before executing the display/cursor home instruction, the data in the four address locations in question should be saved elsewhere by the microprocessor. After execution of the display/cursor home instruction, the data may be restored to the DD RAM.</td>
</tr>
</tbody>
</table>
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