

## ECE 418/518 – Semiconductor Processing

**Catalog Description:** Theory and practice of basic semiconductor processing techniques. Introduction to process simulation.

**Credits:** 4                      **Terms Offered:** Spring

**Prerequisites:** ECE 416 or ECE 317 or equivalent

**Courses that require this as a prerequisite:** None

**Structure:** Two 50-minute lectures and one 2-hour lecture per week for the first 4 weeks; one 110-minute lecture/discussion and two 2-hour labs per week for the last 6 weeks

**Instructors:** T. Plant (primary), P. Dhagat (secondary)

### Course Content:

- Introduction to semiconductor processing
- SUPREM process modeling software use
- Thermal oxidation of silicon and oxide characterization
- Diffusion and ion implantation
- Photolithography, thin film deposition and etching
- MOS and bipolar process integration
- Current topics in microelectronic fabrication
- Laboratory Projects: MOS capacitor fabrication and characterization; MOS transistor, PN diode, integrated resistor, and simple inverter circuit fabrication and characterization; laboratories take students through experiences with wafer cleaning, oxidation, contacts & measurement, field oxidation, source/drain diffusion, gate area patterning, gate oxidation, gate contacts and measurement, and transistor characterization

### Measurable Student Learning Outcomes:

At the completion of the course, students will be able to...

1. **Design and perform** dry and wet oxidation of silicon wafers in the laboratory, calculate the expected thickness of the oxide from the process conditions, and measure the resulting oxide thickness comparing with predicted values (ABET outcomes a, B, C, e, K, m, O)
2. **Fabricate** Al gate MOS capacitors on silicon wafers in the laboratory and perform capacitance-voltage (C-V) measurements (ABET outcomes a, B, C, e, K, O)
3. **Determine** the substrate type and calculate the doping concentration in the substrate, flat band voltage, threshold voltage and the oxide charge from the measured C-V curves (ABET outcomes a, B, e, K, m)
4. **Design and perform** a dopant diffusion process in the laboratory and calculate the junction depth and sheet resistance of the diffused layer from the process conditions (ABET outcomes a, B, C, e, K, m, O)
5. **Fabricate** a simple MOS transistor (gate length ~ 10mm) using a four stage photolithography process and measure the current vs voltage (I-V) characteristics Determine

the threshold voltage and the transconductance from the measured I-V curves (ABET outcomes a, B, C, e, K, O)

6. **Simulate** the MOS capacitor and MOS transistor using SUPREM and compare with measured results after fabrication (ABET outcomes a, B, c, K, O)
7. **Prepare** two reports on projects involving fabrications and characterizations of MOS capacitors and transistors (ABET outcomes a, G, p)

Graduate students are expected to learn about a new device from recently published literature, and explain in a written technical report the processing choices made for that device in the context of current processing technology.

#### **Learning Resources:**

- Richard Jaeger, *Introduction to Microelectronic Fabrication*, 2nd edition, (Vol. V of the Modular Series on Solid State Devices), NJ: Prentice Hall, 2002
- ECE 418/518 Lab Manual – available at bookstore

#### **Students with Disabilities:**

Accommodations are collaborative efforts between students, faculty and Services for Students with Disabilities (SSD). Students with accommodations approved through SSD are responsible for contacting the faculty member in charge of the course prior to or during the first week of the term to discuss accommodations. Students who believe they are eligible for accommodations but who have not yet obtained approval through SSD should contact SSD immediately at 737-4098.

#### **Link to Statement of Expectations for Student Conduct:**

<http://oregonstate.edu/admin/stucon/achon.htm>

Revised: 9/24/07