

## **ECE 471/571 – Advanced Digital Logic and Integrated Circuit Design**

**Catalog Description:** Finite state machine design and analysis, digital system testing and design for testability, custom digital integrated circuit design, CMOS scaling and process variability

**Credits:** 4                   **Terms Offered:** Winter 2008; in later years, Spring

**Prerequisites:** ECE 375 and ECE 271; basic knowledge of Verilog/VHDL recommended

**Courses that require this as a prerequisite:** None

**Structure:** Two 80-minute lectures and one 3-hour lab per week

**Instructors:** P. Chiang

### **Course Content:**

- Review of topics in combinational digital logic: Boolean algebra, analysis and design
- Introduction to digital integrated circuits—gate sizing, power dissipation, rise/fall delay, logical effort and fanout definitions
- Clock skew, timing jitter, dynamic logic and noise margins, pass-gate logic
- Design for testability (DFT): definition of DFT, scan paths, and built-in self test (BIST)
- Transistor scaling, power scaling, interconnect bandwidth, process variability
- Laboratory work – projects/labs on the use of HDL, CAD, digital circuit design schematic, layout, and optimization

### **Measurable Student Learning Outcomes:**

At the completion of the course, students will be able to...

1. **Design and analyze** median complexity combinational and sequential systems (ABET Outcomes: a, c, k, m, n)
2. **Compare** the advantages/disadvantages between HDL synthesis and layout versus custom digital circuit design (ABET Outcomes: b, c, e, j, k, o)
3. **Analyze and understand** various engineering tradeoffs – process scaling, supply voltage reduction, interconnect delay, power consumption, power supply noise (ABET Outcomes: a, b, c, d, e, g, j, o, q)

Graduate students must also apply course techniques to a research problem, including the layout, simulation, and optimization of a complete circuit block.

### **Learning Resources:**

- Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, *Digital Integrated Circuits* (2nd Edition) Prentice Hall, 2002

### **Students with Disabilities:**

Accommodations are collaborative efforts between students, faculty and Services for Students with Disabilities (SSD). Students with accommodations approved through SSD are responsible for contacting the faculty member in charge of the course prior to or during the first week of the

term to discuss accommodations. Students who believe they are eligible for accommodations but who have not yet obtained approval through SSD should contact SSD immediately at 737-4098.

**Link to Statement of Expectations for Student Conduct:**

<http://oregonstate.edu/admin/stucon/achon.htm>

Revised: 9/24/07