A 4.2 GHz PLL Frequency Synthesizer with an Adaptively Tuned Coarse Loop

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Abstract

A 4.2 GHz integer-N PLL frequency synthesizer for WLANs is described. An analog split tuned LC-VCO is controlled by coarse and fine loops to achieve both a large frequency tuning range and a small VCO gain. An averaging varactor is employed to reduce the amplitude sensitivity of the varactor, thereby reducing the AM-to-FM noise conversion. A new adaptively tuned switched capacitor integrator is used in the coarse loop for a fast lock time. The prototype test chip in a 0.13-μm CMOS process has a measured phase noise of -110dBc/Hz at 1 MHz offset, and a settling time of 50 μs.

I. Introduction

The design of PLL frequency synthesizers is a difficult task due to the conflicting requirements of small integrated phase noise, fast settling time, small spur levels, and low power consumption. This is made even more challenging due to increased process, voltage, and temperature (PVT) variations in scaled CMOS processes. For example, the designed frequency tuning range must be much wider than the specifications in order to overcome the PVT variations.

In this paper, we evaluate architectural choices for wide tuning range frequency synthesizers. This leads to the development of an analog split-tuned LC-VCO based 4.2 GHz PLL frequency synthesizer with a wide tuning range and a small VCO gain. In addition, AM-to-FM phase noise conversion is reduced with the use of an averaging varactor and a fast settling time is achieved with a new adaptively tuned switched capacitor integrator.

The paper is organized as follows. In Section II, frequency synthesizer architectures for wide tuning range are compared and an analog split-tuned LC-VCO based architecture is identified as a suitable candidate. This is followed by a linear analysis of the split-tuned PLL in Section III and provides guidance on the selection of the loop parameters. The circuit design is presented in Section IV, followed by measurement results in Section V. The paper is concluded in Section VI.

II. Frequency Synthesizer Architectures

There are several architectural approaches for designing wide frequency tuning range PLL synthesizers. Fig. 1(a) shows a traditional LC-VCO based PLL. A wide tuning range can be achieved by making the control voltage V_{ctrl} swing rail-to-rail and by keeping the VCO gain high. However, a full swing of V_{ctrl} makes the design of a high performance charge pump (CP) with matched UP and DN currents very difficult. In addition, the high VCO gain increases the control voltage sensitivity to both random and deterministic noise.

In order to alleviate these issues, a digital split-tuned LC-VCO based PLL (Fig. 1(b)) can be used. The VCO is controlled by a small varactor as well as a bank of switched capacitors. An auto-tuning circuitry controls the bank of switched capacitors and brings the VCO frequency close to lock. By doing so, both a wide tuning range and a low VCO gain are achieved. However,

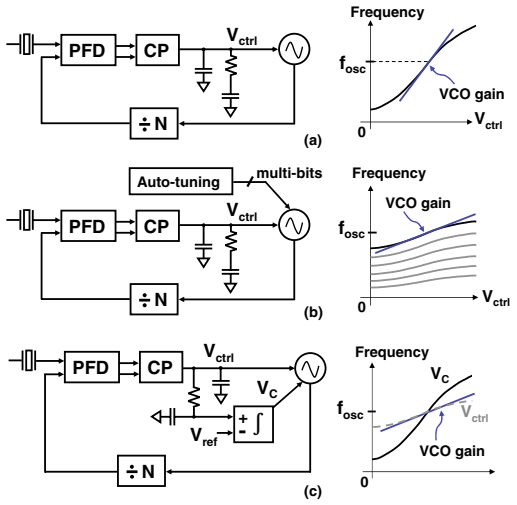

Figure 1: Different PLL frequency synthesizer architectures. (a) Traditional LC-VCO PLL. (b) Digital split-tuned LC-VCO PLL. (c) Analog split-tuned LC-VCO PLL.

a robust frequency calibration algorithm is needed to ensure frequency lock under PVT variations. This not only increases the design complexity but also results in a slow settling time.

An alternative technique is the analog split-tuned VCO based PLL, as shown in Fig. 1(c). This architecture has been implemented using both ring VCOs [1, 2] and LC-VCOs [3]. The VCO is controlled by two varactors: a small varactor tuned by a fine control voltage V_{ctrl} and a large varactor tuned by a coarse control voltage V_C. An additional frequency locking path integrates the voltage across the loop filter integrator capacitor and generates the coarse control voltage V_C to drive the VCO towards frequency lock. The integrator also biases the fine control voltage V_{ctrl} to a known reference voltage V_{ref}, which is set to be $V_{DD}/2$. This offers two advantages over other techniques. First, the design of a high performance CP is made much simpler. Second, the VCO gain variations are reduced, resulting in reduced loop bandwidth variations. Therefore, the analog split-tuned technique is adopted in our prototype 4.2 GHz PLL frequency synthesizer.

Table 1 provides a comparison of the different PLL architectures. In the analog split-tuned technique, the PLL settling is primarily determined by the coarse loop, and is typically slow. To reduce the settling time, a novel adaptively tuned coarse loop is used in this work.

Compared to the digital split-tuned VCO, an analog split-tuned VCO makes use of a large varactor. Due to the varactor's nonlinearity, any amplitude variations on the VCO output node modulate the effective capacitance of the varactor and, hence,

Table 1: Comparison of PLL frequency synthesizers.

Architecture	Traditional	Digital split-tuned	Analog split-tuned
Tuning range	large	large	large
VCO gain	high	low	low
V_{ctrl} swing	extreme	moderate	fixed
PLL Settling	fast	slow	slow
Varactor size	big	small	big
VCO AM-FM	high	low	high

the oscillation frequency. This mechanism, called amplitude-modulation (AM) to frequency-modulation (FM) noise conversion, is a significant source of VCO phase noise. It has been shown that [4], this noise is related to the amplitude sensitivity, $\Delta C/\Delta A$, where ΔC is the change in the varactor capacitance due to a change in the VCO output voltage ΔA. To reduce the AM-FM noise conversion, an averaging varactor is employed in this work. The averaging varactor improves the varactor's linearity and reduces the amplitude sensitivity, thereby lowering the VCO phase noise.

III. Linear Analysis

Fig. 2(a) shows the linear model for the analog split-tuned VCO based PLL, where K_{of} and K_{oc} are the VCO gain for the fine and coarse control nodes, respectively. The fine loop has a 2^{nd}-order loop filter with a zero frequency of $\omega_z = \frac{1}{R_2 C_2}$ and a pole frequency of $\omega_r = \frac{1}{R_2 C_r}$. The coarse loop employs a first order integrator with a transfer function $(1/sR_3C_3 = \omega_3/s)$. Assuming $\omega_z \ll \omega_r$ $(C_2 \gg C_r)$, the fine loop gain $G_F(s)$ and the coarse loop gain $G_C(s)$ can be found to be

$$G_F(s) \approx \frac{\omega_c}{s}(1+\frac{\omega_z}{s})\frac{\omega_r}{s+\omega_r}$$
$$G_C(s) \approx \frac{\omega_c \omega_z \omega_3}{s^3}\frac{K_{oc}}{K_{of}}\frac{\omega_r}{s+\omega_r} \quad (1)$$

where ω_c is approximately the loop bandwidth, and is given by $(I_{CP}R_2/2\pi)\cdot(K_{of}/N)$. The PLL overall loop gain $G_T(s)$ can be expressed as the sum of $G_F(s)$ and $G_C(s)$. ¿From (1),

$$G_T(s) = \frac{\omega_c}{s}\frac{\omega_r}{s+\omega_r}(1+\frac{\omega_z}{s}+\frac{K_{oc}}{K_{of}}\frac{\omega_z\omega_3}{s^2}) \quad (2)$$

The bode plot of the loop gains are conceptually shown in Fig. 2(b). A point of interest is the frequency where the fine loop gain and coarse loop gain are equal. It can be shown that this frequency ω_e is approximated by

$$\omega_e = \frac{K_{oc}}{K_{of}}\omega_3 \quad (3)$$

In the overall loop gain $G_T(s)$, the coarse loop gain $G_C(s)$ is dominant at frequencies below ω_e, and the fine loop gain $G_F(s)$ is dominant at frequencies larger than ω_e. In order for the coarse loop to have a negligible impact on the PLL dynamic and stability, the frequency ω_e should be lower than ω_z. As a result,

$$\frac{K_{oc}}{K_{of}}\frac{1}{R_3C_3} < \frac{1}{R_2C_2} \Rightarrow R_3C_3 > \frac{K_{oc}}{K_{of}}R_2C_2 \quad (4)$$

Eq. (4) illustrates a lower limit for the coarse loop parameters R_3C_3 due to the loop stability constraint. On the other hand,

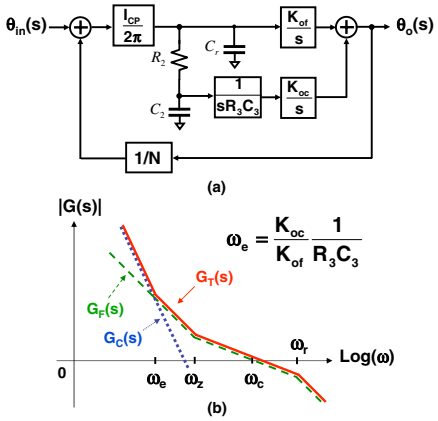

Figure 2: (a) Linear model for the analog split-tuned VCO based PLL. (b) Bode plot of open loop gains.

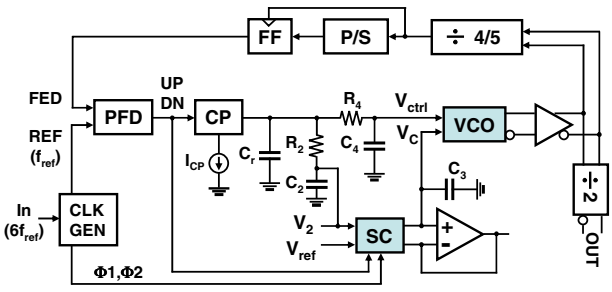

Figure 3: The proposed analog split-tuned LC-VCO based PLL frequency synthesizer.

during lock-in process, the charge-pump output voltage V_{ctrl} would saturate to either the power or ground rail. The coarse loop aids the PLL frequency lock by slewing up or down the coarse control voltage V_C to the desired value. Assume the PLL settling time is dominated by the settling time of the coarse control voltage. If the PLL is required to switch an output frequency from ω_{osc} to $(\omega_{osc} \pm \Delta\omega_{osc})$ within a time period of T_S, then

$$\frac{V_{DD}}{2R_3C_3}T_S K_{oc} > \Delta\omega_{osc} \Rightarrow R_3C_3 < \frac{V_{DD}}{2}T_S\frac{K_{oc}}{\Delta\omega_{osc}} \quad (5)$$

Eq. (5) yields an upper limit for R_3C_3. As a consequence, the design of the coarse control loop must trade off between the loop stability and settling time. To decouple this trade-off and to reduce the settling time, new techniques need to be developed.

IV. Circuit Design

A. Overall Architecture

The proposed PLL frequency synthesizer depicted in Fig. 3 consists of a PFD, a CP, a 3^{rd}-order loop filter, an analog split-tuned LC-VCO, and a pulse-swallow counter. With a 16 MHz reference frequency and a division ratio between 256 to 263, this PLL synthesizer operates in the 4.2 GHz frequency range*. A switched-capacitor (SC) integrator is employed in the coarse

*RF in the 5 GHz WLAN 802.11a lower band can be achieved by mixing the VCO output and its divided-by-4 output [5].

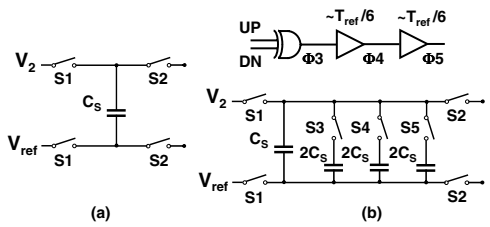

Figure 4: Switched-capacitor circuitry in the coarse loop. (a) Conventional design. (b) Proposed adaptively tuned design.

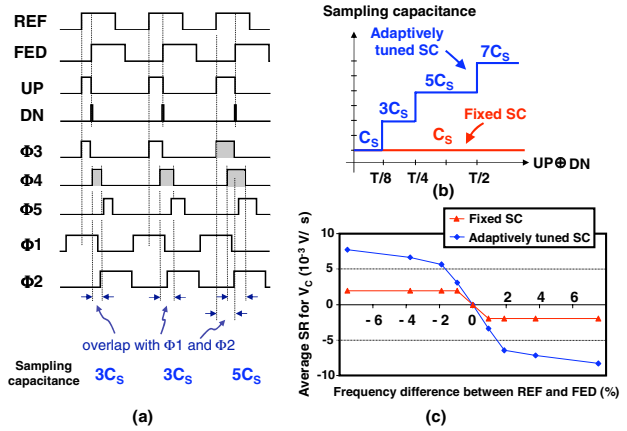

Figure 5: (a) Timing diagram of the adaptively tuned SC integrator. (b) Effective sampling capacitance. (c) Comparison of the simulated slew rates for the coarse control voltage V_C.

loop. A clock generator produces the reference clock for the PLL. It also generates two non-overlapping clock phases, $\Phi 1$ and $\Phi 2$, with the same frequency as the reference for the SC integrator. The exclusive-OR (XOR) of UP and DN pulses from the PFD is also fed into the SC integrator. This will adaptively bring the PLL into lock, hence reducing the settling time.

B. Adaptively Tuned SC Integrator

Fig. 4(a) shows the conventional switched-capacitor circuitry with a sampling capacitance of C_S. In this work as shown in Fig. 4(b), three additional sampling capacitors with capacitance values of $2C_S$ are inserted and controlled by signals $\Phi 3$, $\Phi 4$, and $\Phi 5$, respectively. To generate $\Phi 3$, the PFD output UP and DN pulses are fed into an XOR gate. The pulses $\Phi 4$ and $\Phi 5$ are simply the delayed outputs of $\Phi 3$. The timing diagram is shown in Fig. 5(a). When the loop is in lock, the XOR output is zero. The additional sampling capacitors have no impact on the original SC integrator. When the loop is unlocked, an increased phase error between the reference and feedback clocks leads to an increased pulse width of the XOR output. If the XOR and its delayed outputs have an overlap with both phases $\Phi 1$ and $\Phi 2$, the additional sampling capacitors are effectively added in parallel with the original capacitor C_S. As a result, the effective sampling capacitance is still C_S when the loop is in lock, but it will become $3C_S$, $5C_S$, and $7C_S$ when the XOR output pulse width is larger than $1/8$, $1/4$, and $1/2$ of the reference clock period (Fig. 5(b)). The increased sampling capacitance will reduce the time constant of the SC integrator, thereby improving the PLL settling behavior.

Fig. 5(c) shows the simulated average slew rate (SR) for the coarse control voltage V_C as a function of the frequency difference between the reference clock and the feedback clock. When the two frequencies are close, the adaptively tuned SC circuit behaves the same as the conventional SC circuit. When the two frequencies differ from each other, i.e., the loop is unlocked, the adaptively tuned SC integrator provides an increased slew rate for V_C with an increased frequency difference. As a result, the settling time is reduced without any penalty in the loop stability.

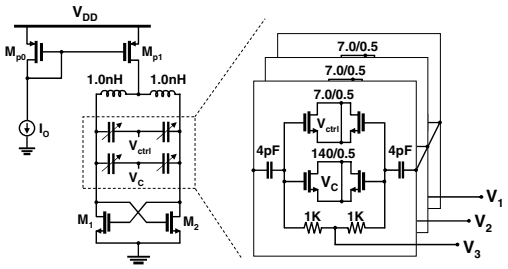

Figure 6: LC-VCO with an averaging varactor.

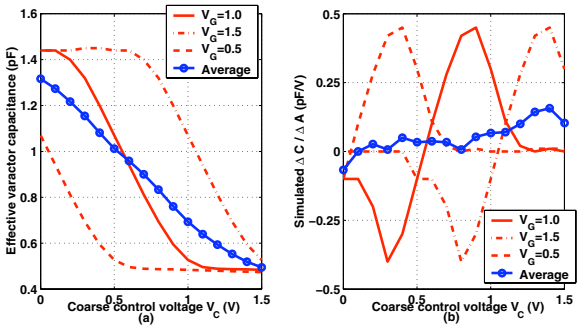

Figure 7: Comparisons of simulated (a) effective capacitance of varactor, (b) sensitivity of VCO output voltage.

C. Split-Tuned VCO with an Averaging Varactor

The split-tuned VCO with an averaging varactor is shown in Fig. 6. Two varactors are sized with a ratio of 20 and controlled by V_{ctrl} and V_C, respectively. For each varactor, three MOS varactors are connected in parallel with DC bias voltages V_1 to V_3. Rather than using a fixed DC bias voltage (i.e., $V_1 = V_2 = V_3$) as in the traditional varactor designs, the averaging varactor uses distributed voltage values for V_1 to V_3. As a result, the nonlinearities of the three varactors are cancelled to a first order. Fig. 7(a) shows the simulated effective capacitance of the conventional varactor when the DC bias voltage V_G is set to be 0.5, 1.0, and 1.5, respectively, compared to the capacitance of the averaging varactor. The averaging varactor also reduces the amplitude sensitivity, $\Delta C/\Delta A$, as shown in Fig. 7(b). Simulation results also show that at 1 MHz offset, a 3 dB improvement in phase noise is achieved in the 4.2 GHz operating frequency range. Although this averaging varactor is similar to the varactor proposed in [6], the focus of this work is on reducing the VCO phase noise by reducing AM-FM noise conversion.

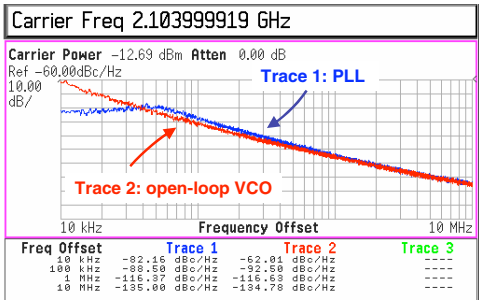

Figure 8: Measured phase noise for the PLL and open-loop VCO at the divided output (half of the oscillation frequency).

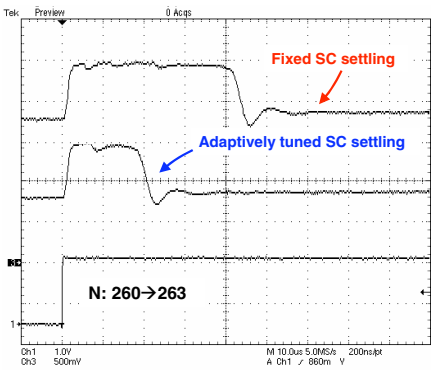

Figure 9: Comparison of the measured settling on the fine control voltages for the fixed and adaptively tuned SC circuits.

V. Measurements Results

The prototype IC was fabricated in a 0.13μm CMOS technology. Operating at 4.208 GHz, the PLL synthesizer draws 32 mA at a 1.5 V supply voltage. The measured phase noise plots for the PLL and the open-loop VCO at half the oscillation frequency are shown in Fig. 8. At 1 MHz offset, the measured PLL phase noise is -116.4 dBc/Hz, which implies a phase noise of -110.4 dBc/Hz (+6 dB due to the division) for the 4.2 GHz PLL. The measured reference spurs level is -48 dBc/Hz and the loop bandwidth is 200 kHz.

To evaluate the adaptively tuned SC circuits, the settling behavior is measured when the division ratio N is changed from 260 to 263. In Fig. 9, the fine control voltages (V_{ctrl}) are initially close to V_{ref}. When N is increased, V_{ctrl} is increased and saturates to V_{DD} until the coarse loop brings the PLL close to lock. Finally V_{ctrl} decreases and settles to V_{ref} when the PLL is in lock. Compared to the fixed SC circuit, the adaptively tuned SC circuit improves the settling time from 75 μs to 50 μs by a factor of 1.5.

The die photo of the prototype chip is shown in Fig. 10. The die area of the PLL synthesizer is 1.5 mm^2 (1.3 mm $\times$ 1.15 mm). Table 2 summarizes a comparison of this prototype to previous work reported on integer-N frequency synthesizers. The noise performance of the proposed PLL frequency synthesizer compares well with previous publications. Additionally, a much faster settling time is measured in the PLL compared to the conventional analog split-tuning PLL [3].

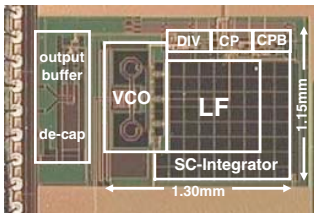

Figure 10: Die photo.

Table 2: Comparison of the proposed PLL frequency synthesizer with prior work.

	[7]	[8]	[3]	This work
Architecture	Traditional	Digital split-tuned	Analog split-tuned	Analog split-tuned
CMOS	0.4-μm	0.25-μm	0.12-μm	0.13-μm
Supply	2.6 V	2.5 V	1.5 V	1.5 V
Reference	11.75 MHz	13.3 MHz	25 MHz	16 MHz
Freq. (GHz)	2.585-2.644	3.2-4.0	2.4	4.096 - 4.208
Die area	2.0 mm^2	1.7 mm^2	0.7 mm^2	1.5 mm^2
Power	47 mW	93 mW	31.8 mW	48 mW
Phase noise dBc/Hz (offset)	-115 (10 MHz)	-118 (1 MHz)	-108 (1 MHz)	-110 (1 MHz)
Settling time	40 μs	150 μs	few ms	50 μs

VI. Conclusions

We have presented a 4.2 GHz fully integrated analog dual-tuned LC-VCO PLL frequency synthesizer. An averaging varactor improved the phase noise by reducing the varactor voltage sensitivity. A fast lock time has been demonstrated using a novel adaptively tuned switched-capacitor circuit in the coarse loop.

Acknowledgments

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