Lab 6 Pre Lab

Create and simulate a module that generates a signal that is logic **LOW** for 96 continuous cycles of an arbitrary clock, and Logic **HIGH** for 704 continuous cycles of the same clock.
This makes for a total of 800 cycles per period.

Pg 37 of the DE10-Lite manual has information about the timing of this signal.

Submit a screenshot of the module you created and it's Modelsim simulation.