A Continuous Time Frequency Translating Delta Sigma Modulator

by

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

A CONTINUOUS TIME FREQUENCY TRANSLATING DELTA SIGMA MODULATOR

1. INTRODUCTION

1.1 Analog-to-Digital Conversion

Analog-to-digital converters are important building blocks of many electronic systems. The signals from the real world are continuously varying analog signals. The general trend in communication system design is to convert the input analog signals in to digital 1's and 0's and do the subsequent signal processing in digital domain. Signal processing in the digital domain is robust, programmable and suited for integration.

Delta Sigma modulators [16] are an important class of analog-to-digital converters. Switched capacitor based lowpass delta sigma modulators have been developed for digitizing analog signals in the voice band with high resolution. Bandpass delta sigma modulators have been developed for the analog-to-digital conversion of IF signals [1], [2], [3], [4], [5], [6]. Delta Sigma modulators are more suited for medium speed, high resolution applications. This translates to bandwidth of the order of hundreds of kHz and 12-20 bits of resolution. The real advantage of delta sigma modulators is that high precision analog components are not required for achieving good performance.

1.2 Contributions

As mentioned earlier, it is desirable to do analog-to-digital conversion as early as possible in communication systems like radio receivers. This could eventually lead to the development of single chip, multi-standard radio receivers. An ideal digital radio will consist of a super analog-to-digital converter, which will digitize RF signal at frequencies of the order of GHz with good dynamic range. Unfortunately, the design of such an A/D converter in CMOS process will be a Herculean task. Even the design of A/D converter for digitizing IF signal at hundreds of MHz, with good resolution is challenging as the designer has to contend with a number of problems.

Bandpass delta sigma modulators have the potential for digitizing IF signals at hundreds of MHz [2], [4], [5]. But this requires the design of accurately tuned, high Q bandpass resonators. The resonators should have good linearity and noise performance. Moreover the jitter in the clock, which synchronizes DAC feedback, pulses [7], [10], [11], [12], [13] can limit the maximum achievable SNR.

This thesis presents a new architecture for digitizing IF signals at hundreds of MHz. The new architecture makes use of frequency translation inside the delta sigma loop [5]. The requirement of the bandpass resonator is much relaxed in the frequency translating delta sigma modulator. A simple design methodology is developed for the system level design of the frequency translating modulator. A prototype frequency translating delta sigma modulator is designed in 0.35μm CMOS process. Methods of simulating continuous time delta sigma modulators to include finite opamp gain, bandwidth, DAC jitter, are presented. Methods to reduce sensitivity of delta sigma modulator to DAC jitter are discussed.

1.3. Thesis Organization

Chapter 2 gives an overview of delta sigma modulators. The basic principle of operation of delta-sigma modulator is described. Delta sigma modulator implementation in discrete time and continuous time is discussed.

Chapter 3 presents the transformation of discrete time, delta sigma loop transfer functions in to *s*-domain loop transfer functions for continuous time delta sigma modulators [19]. Simulation of continuous time delta sigma modulators using state space techniques [15], [20] and impulse invariant transformation are also discussed. The simulation of the effects of finite opamp gain, bandwidth in continuous time delta sigma using impulse invariance is presented.

Chapter 4 deals with the simulation and theoretical estimation of noise due to clock jitter in discrete as well as continuous time delta sigma modulators [7], [10], [11], [12], [13]. It is shown that the jitter sensitivity in continuous time delta sigma modulators is considerably less if we use multi-bit quantizer and feedback DAC. Continuous time low pass delta sigma modulators are shown to be insensitive to time delay jitter in the DAC feedback pulse [11]. A modified DAC feedback to reduce jitter sensitivity in single-bit, lowpass continuous-time delta-sigma modulators is introduced.

Chapter 5 introduces the concept of frequency translating delta sigma modulators in continuous time. A simple design technique for the design of loop transfer function of the frequency translating delta sigma modulator is introduced. It is shown that frequency translating delta sigma modulator are less sensitive to time delay jitter in DAC feedback pulse. The effect of phase noise in the sinusoidal DAC feedback is simulated.

Chapter 6 discusses the transistor level design of a prototype frequency translating delta sigma modulator at 100 MHz IF and 200 kHz bandwidth. All the important blocks in the system are characterized interms of intermodulation and input referred noise. Transistor level simulations show that 80 dB SNR can be achieved at 100 mW static power dissipation.

Chapter 7 provides the conclusions for the thesis

2. OVERVIEW OF DELTA-SIGMA MODULATORS

2.1. Quantization Noise in A/D Converters

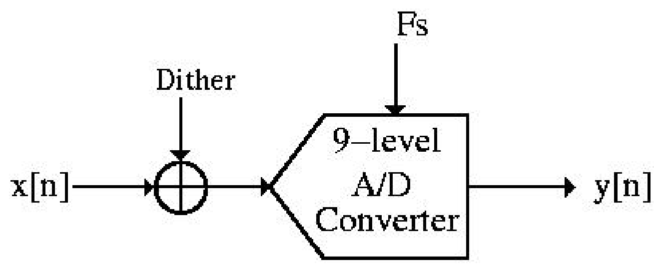

Figure 2.1 9-level analog-to-digital converter

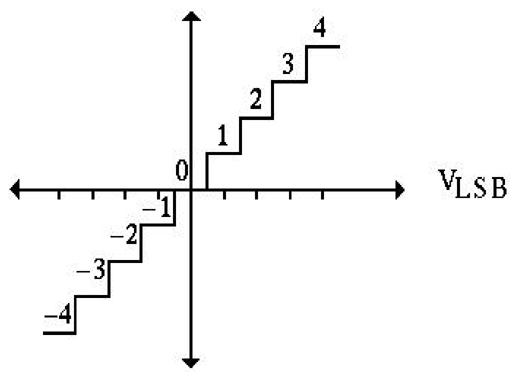

Figure 2.2 ADC transfer curve

Consider a 9 level analog-to-digital converter shown in Figure 2.1. The input voltage range of the A/D converter is divided into 9 equal divisions, each indexed by a digital code, Figure 2.2. The digital output of the A/D converter depends on the voltage interval in which the sampled input signal falls . It is evident from the input-output transfer curve, Figure 2.2, that, the same digital code is produced by a range of input voltages. Thus there is a loss of information inherent in analog to digital conversion. The A/D converter output consists of input signal and quantization error.

If the input signal is varying randomly, then the quantization error is a random variable, uniformly distributed between $\frac{-V_{LSB}}{2}$ and $\frac{V_{LSB}}{2}$, where V_{LSB} is the quantization step. This is called the additive white noise approximation of quantization noise [16]. An input sine wave at a frequency of 100 kHz, sampled at 400 kHz is digitized using a 9-level A/D converter shown in Figure 2.1. A dither signal one-twentieth of V_{LSB} is added to the input signal so that the input signal is sufficiently randomized and the additive white noise approximation of quantization noise holds good. The spectrum of the digitized output is shown in Figure 2.3, consists of a single tone at 100 kHz, corresponding to the input signal and a noise floor corresponding to the quantization noise.

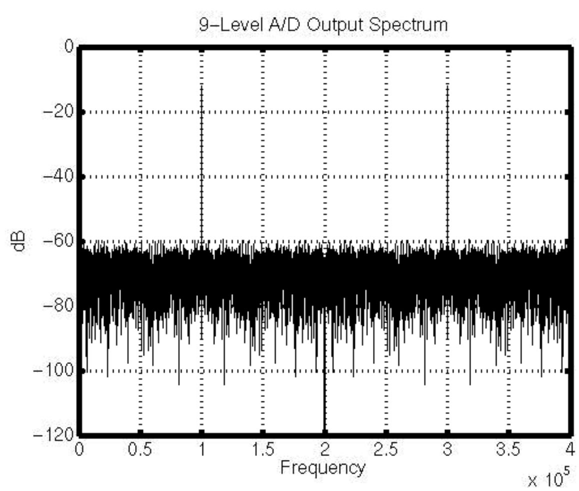

Figure 2.3 9-Level ADC output spectrum

The quantization noise introduced by the A/D converter is approximately white noise, with uniform distribution. This is the additive white noise approximation. The total quantization noise in frequency band from $-f_b$ to f_b is given by Eq 2.1, where f_b is the maximum input signal frequency.

$$P_Q = \frac{V_{LSB}^2}{12 \cdot OSR}, \tag{2.1}$$

Where V_{LSB} is the quantization step and OSR is the oversampling ratio given by Eq 2.2.

$$OSR = \frac{F_s}{2 f_b}, \tag{2.2}$$

Where Fs is the sampling frequency. The quantization noise power reduces by 3dB, for every doubling of oversampling ratio.

2.2. Delta-Sigma Modulators

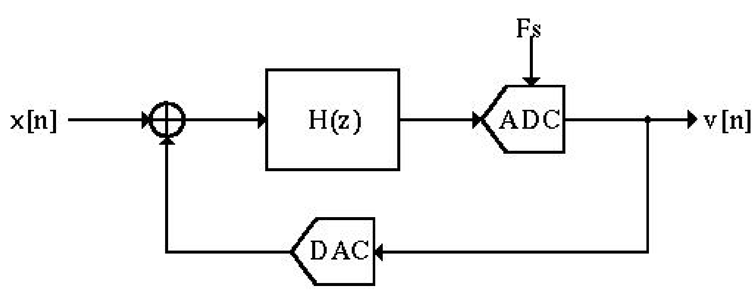

Figure 2.4 General discrete time delta sigma modulator

The generic delta sigma architecture is shown in Figure 2.4. A low resolution A/D converter is embedded in a feedback loop consisting of a high gain loop filter and a linear DAC. Usually single bit A/D converter and

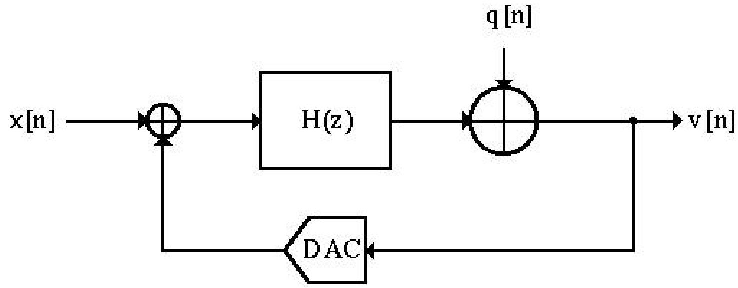

Figure 2.5 Linear Model of delta sigma modulator

DAC are used in delta-sigma modulators, since they are inherently linear. Assuming additive white noise approximation for quantization noise, the linear model for delta sigma modulator is shown in Figure 2.5. u[n], q[n] and v[n] are sampled input signal, quantization noise and digitized output signal of the delta sigma modulator. The signal and noise transfer functions of the delta-sigma modulator are given by Eq 2.3 and Eq 2.4 respectively.

$$STF = \frac{V(z)}{X(z)} = \frac{H(Z)}{1+H(Z)} \qquad (2.3)$$

$$NTF = \frac{V(z)}{Q(z)} = \frac{1}{1+H(Z)} \qquad (2.4)$$

The loop transfer function $H(Z)$ is designed such that the loop filter has a high gain in the band of interest. Thus the signal transfer function is approximately unity and the quantization noise is suppressed by the loop gain of the feedback loop in the band of interest. Let us consider a discrete-time, first order lowpass delta-sigma modulator. The loop filter, $H(Z)$ is a delaying integrator. The signal transfer function and noise transfer function of the discrete time first order lowpass delta sigma modulator is given by Eq. 2.6 and Eq. 2.7 respectively. It is evident from Eq. 2.7 that the quantization noise is highpass filtered and thus suppressed for low frequency signals.

$$H(Z) = \frac{Z^{-1}}{1 - Z^{-1}} \tag{2.5}$$

$$STF = \frac{V(Z)}{X(Z)} = Z^{-1} \tag{2.6}$$

$$NTF = \frac{V(Z)}{Q(Z)} = 1 - Z^{-1} \tag{2.7}$$

2.3. Continuous Time and Discrete Time Delta Sigma Modulators

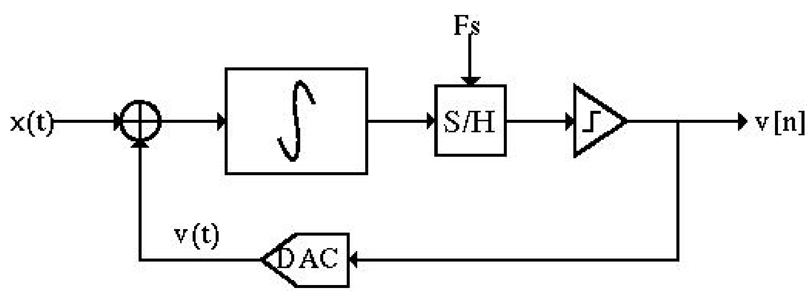

Figure 2.6 First order continuous time delta sigma modulator

The input of the delta sigma modulator in section 2.2 is a sampled signal and its loop transfer function is a discrete time *z*-domain transfer function. We can design the loop transfer function in the s-domain [15]. In this case the front end sample and hold is moved inside the loop, infront of the quantizer. The block diagram of the continuous time delta sigma modulator is shown in Figure 2.6.

Continuous time delta sigma modulators have some advantages over their discrete-time counter parts [5]. The front-end sample and hold in a discrete time delta sigma modulator should be as accurate as the delta sigma modulator. In the case of a continuous time delta sigma modulator the nonidealities of the S/H is suppressed since it is inside the delta sigma loop. Continuous time delta sigma modulators can provide inherent antialias filtering. For a given power dissipation, continuous time delta sigma modulators can operate at a higher speed than its discrete time counterpart. This is because the bandwidth requirement of the opamps in discrete time delta sigma modulators is high due to the slewing and settling in each clock cycle.

2.4. Lowpass and Bandpass Delta-Sigma Modulators

Delta sigma modulators can be used to digitize signals in the baseband. In this case the loop filter will be a lowpass filter with high gain in the frequency band around DC. The delta sigma modulator shown in Figure 2.6 is a first order lowpass continuous time delta sigma modulator. If the loop filter is realized using bandpass resonators tuned to a center frequency, then the delta-sigma modulator can digitize narrowband signals around the center frequency [1], [2], [4], [5], [6]. The output spectrum of lowpass and bandpass delta sigma modulators are shown in Figure 2.7 and Figure 2.8 respectively.

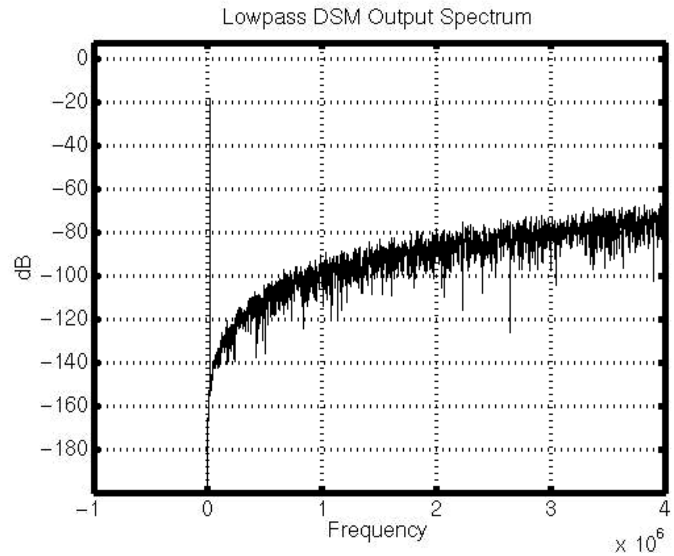

Figure 2.7 Output Spectrum of Lowpass Delta sigma Modulator

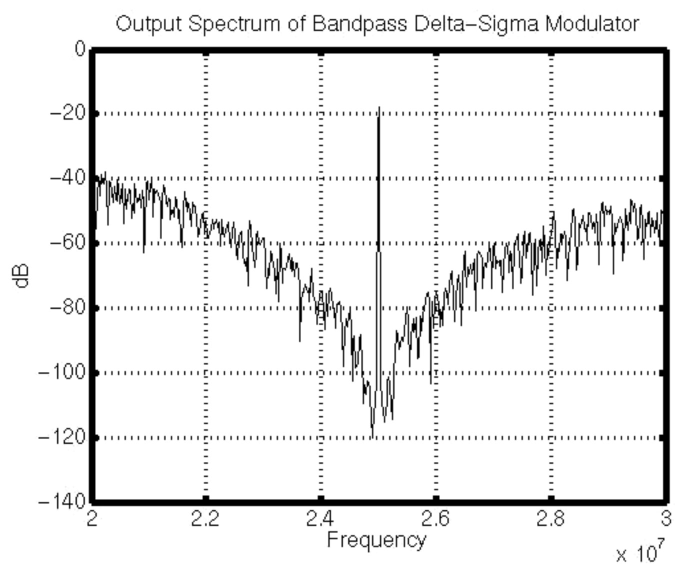

Figure 2.8 Output Spectrum of bandpass delta sigma modulator

3. DESIGN AND SIMULATION OF CONTINUOUS TIME DELTA SIGMA MODULATORS

3.1. Design of Loop Transfer Function of Continuous time Delta Sigma Modulators

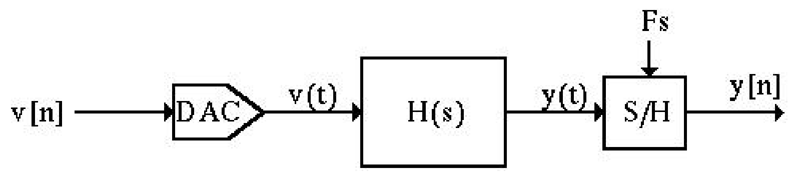

Figure 3.1 Open loop block diagram

Let us break the continuous time delta sigma loop, in order to find the loop gain. The delta-sigma open loop block diagram is given in Figure 3.1. The DAC input in a delta-sigma modulator is updated once in every clock period. Hence the DAC input is inherently discrete time in nature. The analog output of the DAC is the input to the high gain loop filter. The loop filter output is sampled every clock period, to derive the output signal , $v[n]$. The input and output of the open loop block are discrete time signals. Thus the loop transfer function of a continuous-time delta sigma modulator is a discrete time z domain transfer function [19].

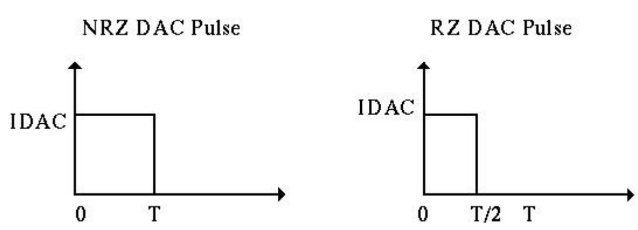

Figure 3.2 Typical DAC feedback pulses

3.1.1 Pulse Invariant Transformation

For a single bit delta-sigma modulator the DAC output is usually a rectangular pulse. The polarity of the rectangular pulse depends on the quantizer output. Typical DAC output pulses used in delta-sigma modulator are shown in Figure 3.2 [19]. The Laplace transform of the NRZ DAC pulse is given by Eq. 3.1, where T is the sampling time period. Thus in a single bit delta-sigma modulator, the

$$H_{DAC}(s) = \frac{1 - e^{-sT}}{s} \tag{3.1}$$

NRZ pulse response of the loop filter is sampled at the output to complete the loop. Mathematically this can be written as

$$H(z) = Z\left\{ L^{-1}\left[H(s)\frac{(1 - e^{-sT})}{s} \right]_{t=nT} \right\}, \tag{3.2}$$

Where T is the sampling period, $H(z)$ is the equivalent discrete time transfer function and $H(s)$ is the actual continuous time loop transfer function. $H(s)$ is chosen such that the resulting $H(z)$ is equal to standard discrete-time loop transfer function, which is already known. The transformation of continuous time loop transfer function to discrete time loop transfer function is called pulse invariant transformation [19], since the impulse response of the equivalent discrete time transfer function is equal to the sampled pulse response o f the continuous time loop transfer function.

3.2. Simulation of Continuous Time Delta Sigma Modulators with State Space Techniques

Any linear, causal, lumped system can be described using a rational s domain transfer function of the form $\frac{Y(s)}{X(s)}$. The equivalent time domain description of the system is in the form of an n^{th} order differential equation. It is convenient to break up the n^{th} order differential equation in to n first order differential equations to predict the time domain behaviour of the LTI system. This system of first order differential equations is called state space formulation of the LTI system [20].

3.2.1 State Space Formulation of a Simple LTI System

Let us consider an LTI system whose s domain transfer function is given by Eq. 3.3. The equivalent differential equation describing the time

$$\frac{Y(s)}{X(s)} = \frac{1}{(s+1)^2} \tag{3.3}$$

$$\frac{d^2 y(t)}{dt^2} + 2\frac{dy(t)}{dt} + y(t) = x(t) \tag{3.4}$$

domain behavior of the system is given by Eq. 3.4. Let us define a new variable, $y_1(t)$, given by Eq. 3.5

$$y_1(t) = \frac{dy(t)}{dt} + y(t) \tag{3.5}$$

The second order differential equation given in Eq. 3.4 can be rewritten as

$$\frac{dy_1(t)}{dt} + y_1(t) = x(t) \tag{3.6}$$

Note that Eqs 3.5 and 3.6 are first order differential equations and can be represented in the form of a matrix. This is an example of state space formulation of a second order LTI system.

$$\begin{bmatrix} \dot{y}(t) \\ \dot{y}_1(t) \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} y(t) \\ y_1(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} x(t) \tag{3.7}$$

The general state space formulation of an LTI system are given by Eqs. 3.8 and 3.9 [20]. The state vector, $X(t)$ of an LTI system represents the memory of the system. Thus for a lowpass delta-sigma modulator, the state vector consists of all the integrator outputs. For a bandpass delta-sigma, based on LC resonators, the current through the inductor and the voltage across the capacitor in the LC tank circuit determines the state vector.

$$\dot{X}(t) = AX(t) + BX_{in}(t), \tag{3.8}$$

$$Y(t) = CX(t) + DX_{in}(t), \tag{3.9}$$

Where $X(t)$, $X_{in}(t)$, $Y(t)$ are state vector, input vector and output vector respectively.

3.2.2 State Space Formulation of Delta Sigma Modulator

Let us formulate the state space equation of a second order lowpass continuous time delta sigma modulator [15]. The block diagram of the delta sigma modulator is given in Figure 3.3. If we know the input signal, $x_{in}(t)$, integrator outputs, $x_1(t)$ and $x_2(t)$ at time $t = t_o$, then all the other signals in the system, including the quantizer output, $v[n]$ and the DAC output, $v(t)$ are known. The state space formulation of the delta sigma modulator are given by Eqs 3.10, 3.11, 3.12 and 3.13. It is assumed that the integrator time constant, T is equal to the time period of the sampling clock

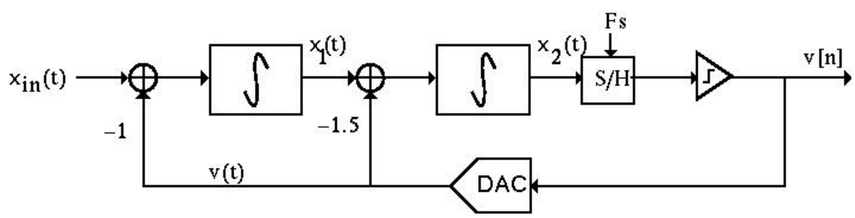

Figure 3.3 Second Order Continous time lowpass delts sigma modulator

$$\dot{x}_1(t) = \frac{1}{T}x_{in}(t) - \frac{1}{T}v(t) \qquad (3.10)$$

$$\dot{x}_2(t) = \frac{1}{T}x_1(t) - \frac{1.5}{T}v(t) \qquad (3.11)$$

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \frac{1}{T}\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \frac{1}{T}\begin{bmatrix} 1 & -1 \\ 0 & -1.5 \end{bmatrix}\begin{bmatrix} x_{in}(t) \\ v(t) \end{bmatrix} \qquad (3.12)$$

$$V[n] = \mathrm{sgn}(x_2(nT)) \qquad (3.13)$$

3.2.3 Solving State Space Equations of LTI Systems

There are several ways to describe an LTI system. For example the frequency domain behaviour of an LTI system can be characterized as a rational s domain transfer function. As we saw earlier, we can formulate differential equations to predict the time domain response of LTI system to input signals. The steady state response of LTI systems is characterized by its impulse response. The time domain response of a causal, LTI system with impulse response, $h(t)$, to an input signal $x(t)$ is given by Eq. 3.8.

$$y(t) = \int_{-\infty}^{t} h(t-\tau)x(\tau)d\tau \tag{3.14}$$

However the general time domain response also depends on the initial state of the system. The general time domain response of a causal, LTI system is given by Eq. 3.15

$$y(t) = z(t) + s(t), \tag{3.15}$$

Where $z(t)$ is the zero state response of the LTI system, determined by the initial condition and $s(t)$ is the steady state response of the LTI system. The solution of the state space equations is also given by the sum of zero state response and steady state response. However the impulse response of an LTI system with state space formulation is a matrix containing time domain responses of the states to an impulse input. The time derivative of the state vector is given by Eq. 3. 16. The matrix A in the state equation is called the transition matrix. The impulse response of the state vector is given by the matrix exponential of the transition matrix of the system.

$$\dot{X}(t) = AX(t) + BU(t) \tag{3.16}$$

$$h_s(t) = e^{At} = I + At + \frac{1}{2!}(At)^2 + \frac{1}{3!}(At)^3 + ..., \tag{3.17}$$

Where $h_s(t)$ is the impulse response of the state vector. The general solution to the state equation is given by

$$X(t) = e^{A(t-t_0)}X(t_o) + \int_{t_0}^{t} e^{A(t-\tau)}U(\tau)d\tau, \tag{3.18}$$

Where $X(t_o)$, represents the initial state of the system. The detailed derivation of Eq. 3.18 [20] is beyond the scope of this thesis. However it is possible to intuitively understand the significance of each term in the solution. The first term, $e^{A(t-t_o)}X(t_o)$ solely depends on the initial condition and is the zero state response of the system. The second term, $\int_{t_o}^{t} e^{A(t-\tau)}u(\tau)d\tau$ is similar to the steady state response of an LTI system given by Eq. 3.14.

Let us try to further compare the solution of state space equations given by Eq. 3.18 to the time domain behaviour of a first order system, say a simple RC lowpass filter. This makes sense because state space equations are basically a set of first order differential equations. Let the initial charge in the capacitor be $v_{initial}$. The impulse response of the RC lowpass filter is given by Eq. 3.19.

$$h(t) = ae^{-at}, \tag{3.19}$$

Where a is the RC time constant. The input is a unit step input, applied at time $t = 0$. We know that step response is the integral of impulse response and also the initial charge in the capacitor should exponentially decay to zero volts. Therefore the time domain response of the RC lowpass filter is given by Eq. 3.20. Note the similarity of the general state space solution and the time domain behavior of first order RC lowpass filter.

$$y(t) = e^{-at} v_{initial} + \int_0^t a e^{-a(t-\tau)} d\tau \qquad (3.20)$$

3.2.4 Solutions of State Space Equations of Delta Sigma Modulator

The general solution to the state equation can be used to compute the integrator states in a lowpass delta-sigma modulator at $t = nT$. More often than not, the computation of the matrix exponential is very difficult. However in the case of second order lowpass delta sigma modulator shown in Figure 3.3, it is possible to hand calculate the matrix exponential. The transition matrix of the delta sigma modulator is given by Eq. 3.21. In this case $A^n = 0$, n is an integer. Thus the matrix exponential is given by Eq. 3.22.

$$A = \frac{1}{T}\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \qquad (3.21)$$

$$e^{At} = I + At = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \frac{t}{T}\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \qquad (3.22)$$

$$e^{At} = \begin{bmatrix} 1 & 0 \\ \frac{t}{T} & 1 \end{bmatrix} \qquad (3.23)$$

We only need to know the integrator outputs at $t = nT$, where T is the sampling frequency. Therefore substituting $t = nT$ and $t_o = (n-1)T$, we get Eq. 3.24.

$$X[nT] = e^{AT} X[(n-1)T] + \int_{(n-1)T}^{nT} e^{A(nT-\tau)} BU(\tau) d\tau \qquad (3.24)$$

$$e^{AT} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \qquad (3.25)$$

The DAC output is a NRZ rectangular pulse modulated by the quantizer output V[(n-1)T]. Thus, the integration of DAC pulse is easy. Solving Eq. 3.24, we derive a set of difference equations, Eq. 3.26 [15], which model the operation of continuous time delta sigma modulator. There are absolutely no approximations involved and the state space equations also model the antialias filtering of continuous time delta sigma modulator. The output spectrum of the second order continuous time delta sigma modulator based on state space equations is shown in Figure 3.4. The simulated SNR is 93.9 dB for a bandwidth of 400 kHz and sampling frequency of 100 MHz.

$$\begin{bmatrix} X_1[n] \\ X_2[n] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} X_1[(n-1)] \\ X_2[(n-1)] \end{bmatrix} + \begin{bmatrix} -1 \\ -2 \end{bmatrix} V[n-1] + \begin{bmatrix} \dfrac{1}{T} \displaystyle\int_{(n-1)T}^{nT} U(t) dt \\ \dfrac{1}{T} \displaystyle\int_{(n-1)T}^{nT} (nT - t) U(t) dt \end{bmatrix} \qquad (3.26)$$

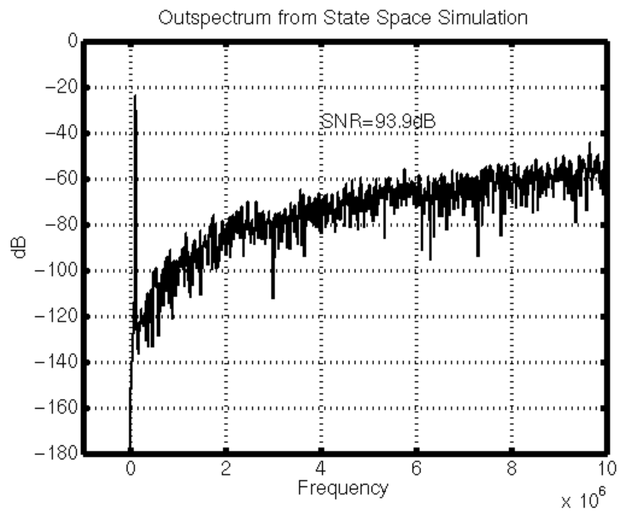

Figure 3.4 Output Spectrum from state space simulation

3.3. Simulation of Continuous Time Delta Sigma Modulator with Impulse Invariance

State space simulation of delta sigma modulator is accurate and very fast. However solving the state equations can be tedious and time consuming. The solving state space equation can be extremely difficult if we try to include nonidealities like finite opamp gain, finite opamp bandwidth, timing jitter in DAC feedback pulse etc. Even solving state space equations for ideal bandpass delta sigma modulators can be difficult.

3.3.1 Impulse Invariance Transformation

Let $x(t)$, be a band limited signal. We know that if we sample $x(t)$ at a rate higher than the Nyquist rate, then there is no loss of information. The continuous time signal $x(t)$ can be reconstructed from the sampled signal $x[n]$. Consider the system shown in Fig. 3.4. The signal $x(t)$ is the input to a continuous time LTI system with impulse response $h(t)$. We are only interested in the output signal $y(t)$ at time, $t = nT$. It the input is bandlimited, the output is also bandlimited. It may be possible to move the sample and hold at the output to the input as shown in Figure 3.5. The continuous time loop filter is replaced by an equivalent discrete time filter, such that the output of the discrete time filter $y_1[n] = y[nT]$. It can be shown that the impulse response of the equivalent discrete time loop filter is given by Eq. 3.22. This is called the impulse invariant transformation.

$$h_1[n] = h[nT] \qquad (3.27)$$

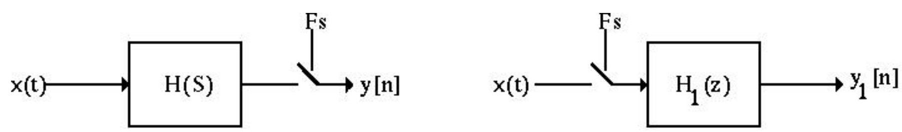

Figure 3.5 Signal processing in continuous time and discrete time

In order to simulate continuous time delta sigma modulators with impulse invariant transformation, we split the sampling time period in to smaller time intervals. we replace the continuous-time loop transfer function with its impulse invariant transformation [5] corresponding to the smaller time interval. Thus simulation is done in discrete time and can be easily implemented with standard matlab functions. The loop gain is determined by the DAC pulse response of the loopfilter of delta-sigma modulator. The DAC pulse response of the loopfilter of the delta-sigma modulator shown in Figure 3.3 is predicted from theory and impulse invariance transformation were found to match very closely, as shown in Figure 3.6.

3.3.2 Modeling of Nonidealities with Impulse Invariance

An important advantage is that the nonidealities like finite opamp gain, finite opamp bandwidth, DAC feedback jitter, delay in the DAC feedback etcetra can be easily modeled. The continuous-time loop transfer function with finite opamp gain and bandwidth can be easily computed. These nonidealities will be represented in the impulse invariant transfer function. DAC feedback jitter is simulated by randomly varying the number of time steps in the sampling clock period from one cycle to another.

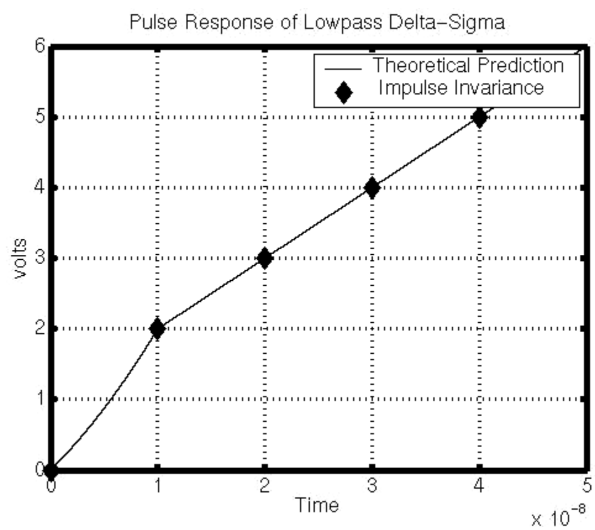

Figure 3.6 Pulse response of CTLPΔΣM

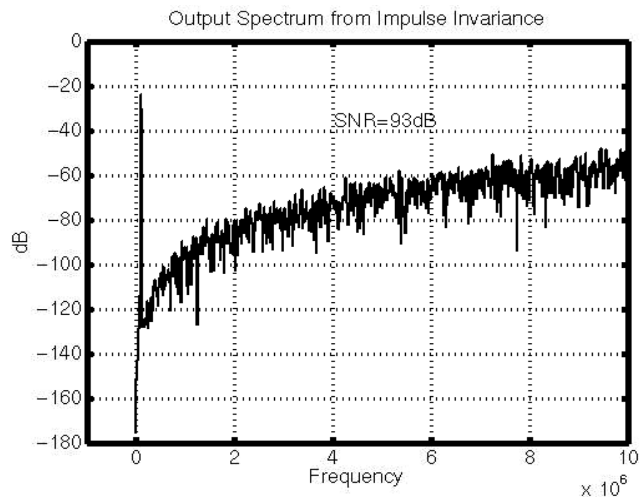

Figure 3.7 Output Spectrum from simulation using impuse invariance

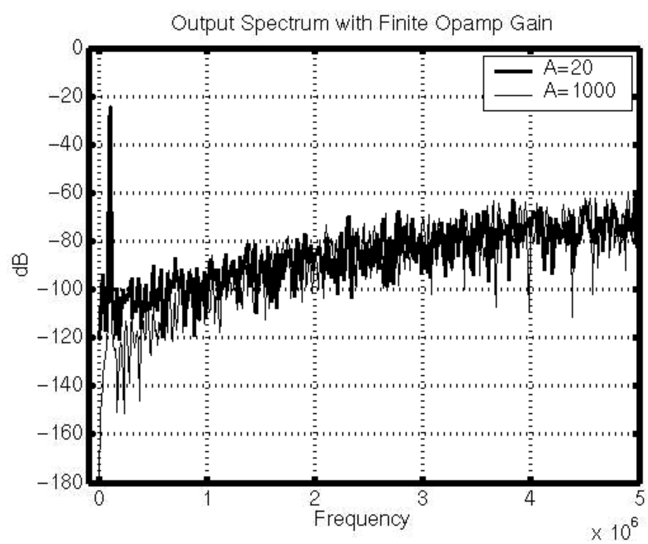

Figure 3.8 Effect of opamp gain on CTLPΔΣM performance

The effect of finite opamp gain on the operation of continuous time delta sigma modulator is shown in Figure 3.8. Impulse invariance method was used for simulation. The noise floor flattens in the baseband when the opamp gain if small. The effect of finite opamp bandwidth is shown in Figure 3.9. The delta-sigma modulator was simulated assuming opamp unity gain bandwidth of 1 MHz. The sampling frequency is 100 MHz. The opamp finite bandwidth seems to introduce a high frequency pole in the noise transfer function.

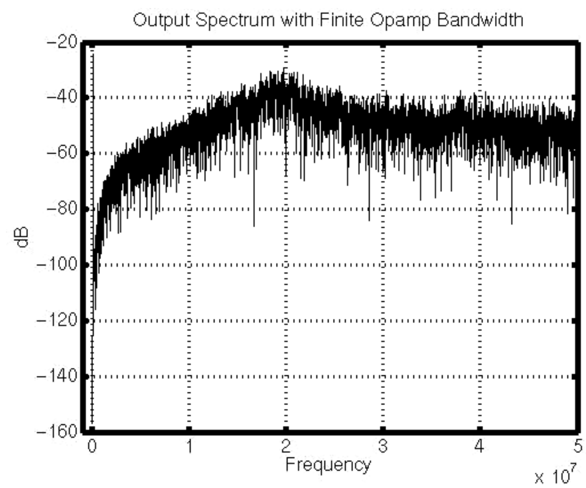

Figure 3.9 CTLPΔΣM output specturm with finite opamp bandwidth

4. JITTER PERFORMANCE OF DELTA SIGMA MODULATOR

4.1. Jitter Performance of Discrete Time Delta Sigma Modulators

In discrete time delta sigma modulators, the input signal is a discrete time sampled signal. Therefore a front end S/H circuit is required in a discrete time delta sigma modulator. The error due to the jitter in the clock synchronizing the S/H appears directly as noise in the input signal, limiting the maximum achievable SNR. The voltage error due to uncertainty in the sampling instant is given by Eq 4.1.

$$e[n] = A\sin[\omega(nT + \delta t[n])] - A\sin[\omega nT], \tag{4.1}$$

$$e[n] \approx A\omega\delta t[n]\cos(\omega nT), \tag{4.2}$$

Where $e[n]$ is the voltage error, $\delta t[n]$ is the uncertainty in the sampling time instant. The signal power and noise power are given by Eq 4.3 and Eq 4.4 respectively.

$$P_s = \frac{A^2}{2}, \tag{4.3}$$

$$P_e = \frac{A^2\omega^2\sigma_{\delta t}^2}{2}, \tag{4.4}$$

Where $\sigma_{\delta t}^2$ is the variance of the timing error. The signal to noise ratio, after integrating the jitter noise in the band of interest is given by Eq 4.5 [7], [10].

$$SNR = 10\log\left(\frac{OSR}{4\pi^2 f_b^2 \sigma_{\delta t}^2}\right) \quad (4.5)$$

4.2. Jitter Performance of Lowpass Delta Sigma Modulator

The DAC feedback in continuous time delta sigma modulator is usually a rectangular pulse of certain duration, whose polarity depends on the single bit quantizer output. The DAC feedback pulse is shown in Figure. 4.1. The delay of the DAC feedback pulse and the pulse width can vary randomly from one clock cycle to another. This results in noise at the output spectrum of the delta sigma modulator.

The DAC pulse is assumed to be NRZ pulse. Therefore there is only pulse width jitter, no time delay jitter. A timing error is associated with each clock edge. The voltage error due to DAC pulse width jitter and the maximum signal amplitude are given by Eq 4.6 and Eq 4.7 respectively.

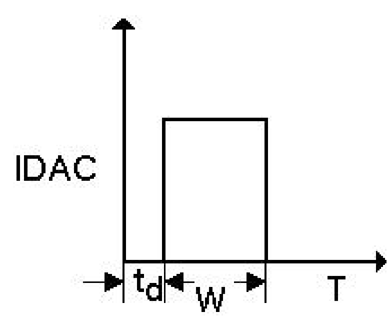

Figure 4.1 DAC feedback pulse

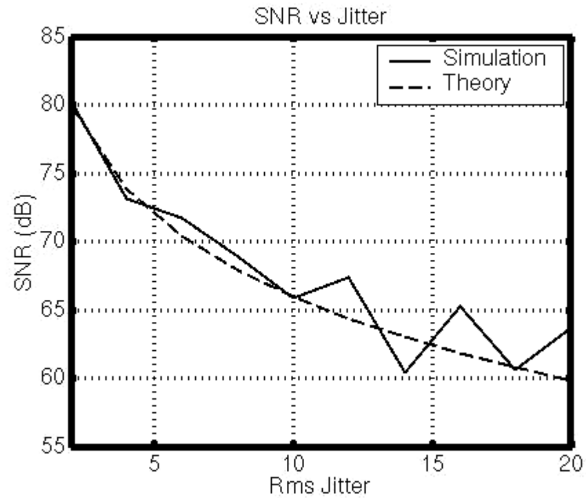

Figure 4.2 SNR vs jitter plot for CTLPΔΣM

$$e[n] = \delta t[n]\frac{I_{fb}}{C_o}, \tag{4.6}$$

$$A_{\max} = \frac{I_{fb}T}{2C_0}, \tag{4.7}$$

Where I_{fb} is the DAC feedback current, T is the sampling time period, C_o is the integrating capacitance. The maximum SNR is given by [7], [10]

$$SNR_{\max} = 10\log\left(\frac{A_{\max}^2}{\sigma_e^2}\right) = 10\log\left(\frac{1}{16 \cdot OSR \cdot f_b^2 \cdot \sigma_{\delta t}^2}\right) \tag{4.8}$$

The simulated and theoretically predicted SNR is given in Figure. 4.2.

4.3. Jitter Performance of Continuous Time Delta Sigma Modulator with Multi Bit Quantizer

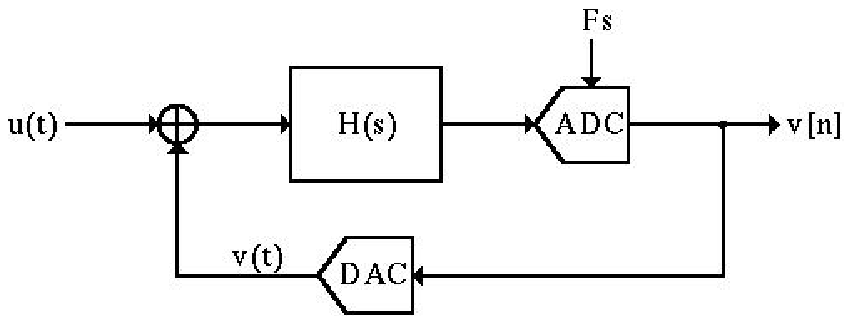

Figure 4.3 General CTΔΣM

Let us calculate the jitter induced error at the output of a general continuous-time delta-sigma modulator shown in Figure 4.3. The DAC output can be expressed as in Eq. 4.9, in the absense of DAC jitter.

$$V(t) = \sum_{k=-\infty}^{k=\infty} v[k]\left[u(t-kT) - u(t-(k+1)T)\right], \qquad (4.9)$$

Where $u(t)$ is the unit step function. Assuming a DAC jitter of $\delta t[k]$, Eq. 4.9 can be rewritten as in Eq. 4.10. The DAC output given in Eq. 4.10 passes through the loop filter and the loop filter output is given by Eq. 4.11.

$$V(t) = \sum_{k=-\infty}^{k=\infty} \left[v[k] - v[k-1]\right] u(t-kT+\delta t[k]), \qquad (4.10)$$

$$Y(t) = \sum_{k=-\infty}^{k=\infty} \left[v[k] - v[k-1]\right] h_b(t-kT+\delta t[k]), \qquad (4.11)$$

Where $h_b(t)$ is the step response of the loop filter. Expanding Eq. 4.11 in Taylor series we get the error induced by the DAC jitter. The error induced by the DAC at the output of the delta-sigma modulator is given by Eq. 4.12, where $h(t)$ is the impulse response of the loop filter [10].

$$Y(t) = \sum_{k=-\infty}^{k=\infty} [v[k] - v[k-1]][h_b(t-kT) + h(t-kT)\delta t[k]] \tag{4.12}$$

$$Y[nT] = \sum_{k=-\infty}^{k=\infty} [v[k] - v[k-1]]\, h_b(n-k) + \sum_{k=-\infty}^{k=\infty} [v[k] - v[k-1]]\delta t[k] h(n-k) \tag{4.13}$$

$$error[n] = ([v[n] - v[n-1]] \cdot \delta t[n]) * h[n] \tag{4.14}$$

The sequence $v[n] - v[n-1]$ is modulated by the timing error sequence, $\delta t[n]$. Thus high frequency quantization noise is modulated in to the band of interest, there by severely degrading the SNR. One way to reduce sensitivity is to reduce the power of the sequence, $v[n] - v[n-1]$.

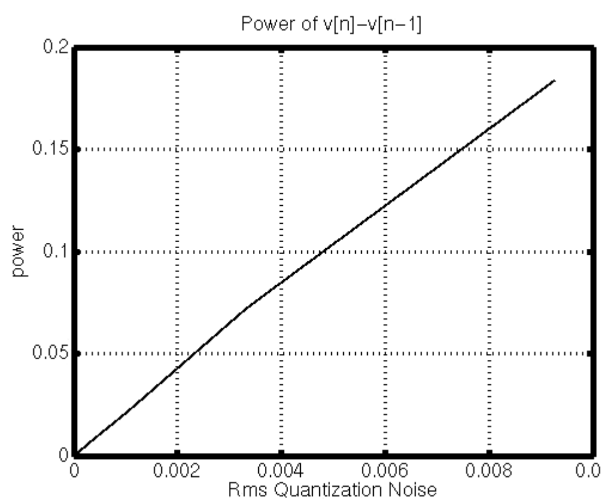

Figure 4.4 Power pf v[n]-v[n-] vs quantiztion noise power

This translates to reducing the cycle to cycle voltage or current transitions at the DAC output. In a multi-bit delta-sigma modulator with NRZ DAC , the cycle to cycle voltage or current change at the DAC output is smaller . Thus multi-bit continuous-time delta-sigma modulators are less sensitive to DAC jitter. The power of the sequence $v[n]-v[n-1]$ is plotted as a function of quantization noise power in Figure 4.4. The power of the sequence $v[n]-v[n-1]$ is directly proportional to the quantization noise power. This means that jitter performance improves by 6dB with each bit in the quantizer.

4.4. Time Delay Jitter Performance of Lowpass Delta Sigma Modulators

Consider a first order lowpass delta sigma modulator with RZ DAC feedback. As explained in section 4.2, the time delay and pulse width of the RZ DAC pulse can vary randomly from one clock cycle to another. The

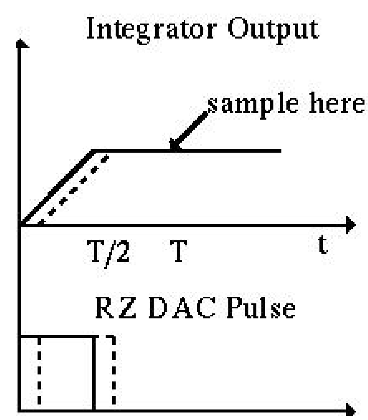

Figure 4.5 Open loop response to RZ DAC pulse with time delay jitter

open loop response of the integrator to a single RZ DAC pulse is shown in Figure 4. 5. The integrator output is a constant at the sampling time T and is a measure of the area under the DAC pulse. So if the RZ DAC pulse has only time delay jitter associated with it, then the area under the RZ DAC pulse is a constant. The open loop response of the first order continuous time lowpass delta sigma modulator does not change with time delay jitter. Thus a first order lowpass continuous time delta sigma modulator is insensitive to time delay jitter. This is true for any general, continuous time lowpass delta sigma modulator [11]. The SNR vs time delay jitter plot of a second order lowpass continuous time delta sigma modulator with RZ DAC feedback is shown in Figure 4.6.

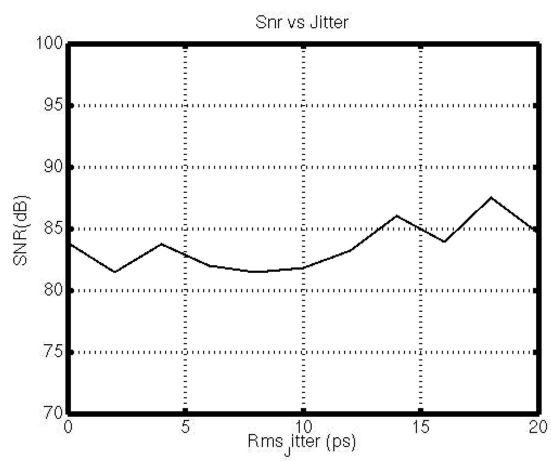

Figure 4.6 SNR vs jitter plot for time delay jitter

4.5. DAC Feedback with Reduced Jitter Sensitivity

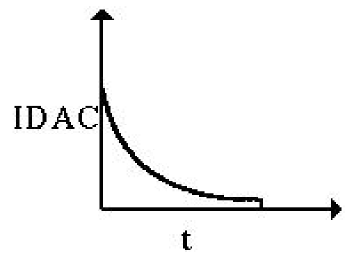

Figure 4.7 Modified DAC feedback pulse

As discussed in section 4.4, a continuous time delta sigma modulator is less sensitive to time delay jitter associated with the DAC pulse. Thus if we use an edge triggered monostable pulse generator, the jitter performance of continuous time delta sigma modulators will be much better. Another alternative is to reduce the amplitude of the DAC pulse before the second clock edge occurs. This is achieved by charging a capacitor and discharging in to the virtual ground of the integrator through a resistor.

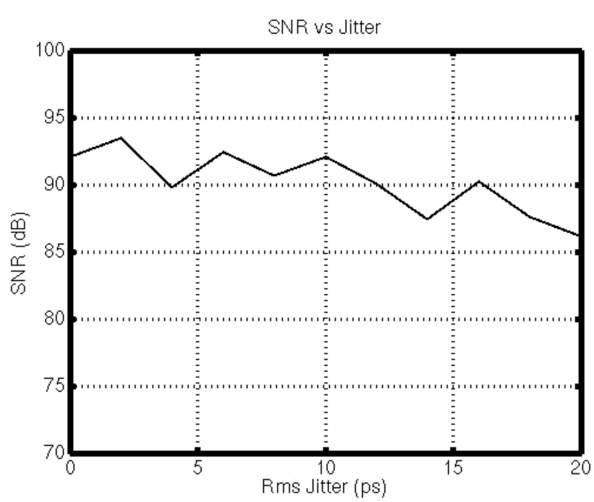

Figure 4.8 SNR vs jitter plot for CTLPΔΣM with modified DAC feedback

4.5.1 Feedback Coefficents of CTLPΔΣM with Modified DAC Feedback

A second order continuous time lowpass delta sigma modulator was simulated using the modified DAC feedback, Figure 4.7. The feedback coefficients of the delta sigma modulator are calculated by equating the open loop response to that of a standard continuous time lowpass delta sigma modulator with NRZ DAC feedback, whose feedback coefficients are already known. Consider the open loop block diagram, Figure 3.1, of a standard continuous time lowpass delta sigma modulator with NRZ DAC feedback. The feedback coefficients are $a_1 = -1$, $a_2 = -1.5$. Let us give a NRZ pulse as the input to the open loop block. The integrator time constant is equal to the period of the sampling clock, T. The output signals the output nodes of integrators are given by Eq.

$$x_1(t) = \begin{cases} a_1 \dfrac{t}{T}, & \mathrm{t} \le \mathrm{T} \\ a_1, & \mathrm{t} > \mathrm{T} \end{cases} \tag{4.15}$$

$$x_2(t) = \begin{cases} a_1 \dfrac{t^2}{2T^2} + a_2 \dfrac{t}{T}, & \mathrm{t} \le \mathrm{T} \\ \mathrm{a}_1 \dfrac{t}{T} + a_2 - \dfrac{a_1}{2}, & \mathrm{t} > \mathrm{T} \end{cases} \tag{4.16}$$

Let the feedback coefficients of the delta sigma modulator with modified DAC feedback be $a_1^{\sim}$ and $a_2^{\sim}$. It can be shown that the open loop response of the delta sigma modulator or $x_2^{\sim}(t)$ for $t > T$ is given by Eq. 4.22.

$$x_2^{\sim}(t) = b_1 \frac{(t-T)}{T} + b_2 \,, \quad t \leq T \tag{4.17}$$

$$b_1 = \frac{a_1^{\sim}}{\omega_o T}(1 - e^{-\omega_o T}), \tag{4.18}$$

$$b_2 = \frac{a_1^{\sim}}{\omega_o T} - \frac{a_1^{\sim}}{(\omega_o T)^2}(1 - e^{-\omega_o T}) + \frac{a_2^{\sim}}{\omega_o T}(1 - e^{-\omega_o T}), \tag{4.19}$$

Where $\omega_o = \dfrac{1}{RC}$. The RC time constant was set such that the, DAC feedback waveform decays by 99.99% at the second clock edge. The open loop response in delta sigma modulator with modified DAC feedback should be equal to the open loop response of the delta sigma modulator with NRZ DAC feedback.

$$x_2^{\sim}(t) = x_2(t), \quad t \geq T \tag{4.20}$$

The values of $a_1^{\sim}$ and $a_2^{\sim}$ are found out from Eq. 4.23.

$$a_1^{\sim} = -5$$

$$a_2^{\sim} = -6$$

Note that the values of $a_1^{\sim}$ and $a_2^{\sim}$ are much higher than a_1 and a_2. This means that to achieve the same dynamic range, the DAC feedback current is much higher. Thus the power dissipation in the delta sigma modulator with modified DAC feedback will be more. The SNR vs jitter plot for second order lowpass delta-sigma modulator with the new DAC feedback is shown in Figure 4.8.

5. FREQUENCY TRANSLATING DELTA SIGMA MODULATOR

5.1. Frequency Translation Inside Delta-Sigma Loop

Bandpass delta sigma modulators are well suited for the digitization of narrowband signals digitized on a carrier signal. In a conventional bandpass delta-sigma modulator, the input IF signal is amplified by a high gain loop filter accurately tuned to the desired center frequency. The output of the loopfilter is digitized and the digitized output is fedback to the loopfilter by a single bit DAC [1], [2], [3], [4], [5], [6].

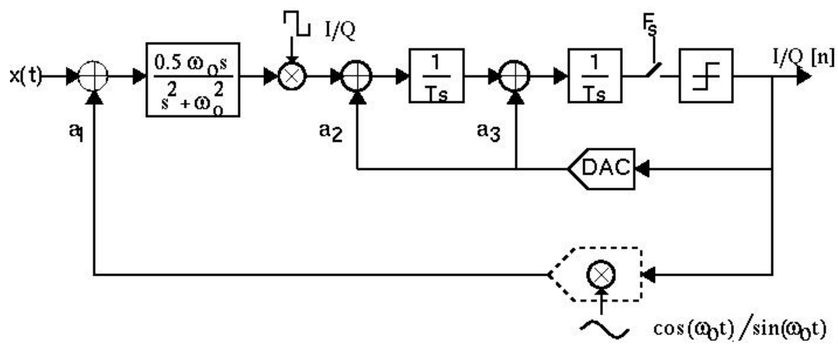

Figure 5.1 Frequency translating bandpass delta sigma modulator

In a frequency translating bandpass delta sigma, Figure 5.1, input IF signal is amplified by a low gain wideband bandpass resonator [5]. The amplified IF signal is down converted to baseband. The down converted signal is digitized using a continuous time lowpass delta sigma modulator. The digitized output is up converted and fedback to the bandpass resonator. Thus most of the signal processing is done in the low frequency domain. The main purpose of the bandpass filter is to reduce the design requirement of blocks inside the delta sigma loop.

5.2. Motivation

It is desirable to do analog-to-digital conversion as early as possible in communication systems like radio receivers. This could eventually lead to the development of single chip, multi-standard radio receivers. Direct digitization of RF signals is very difficult since it requires A/D converters to digitize signals at frequencies of the order of GHz. However design of A/D converters for direct digitization of IF signal is possible although it is very challenging.

5.2.1 Conventional Bandpass Delta Sigma Modulators

Conventional bandpass delta sigma modulators for direct digitization of IF signals of the order of hundreds of MHz are very difficult to design in CMOS technology. The main reason is that bandpass delta sigma modulators require precisely tuned, high Q, low noise and linear bandpass pass filter in the loop filter. Conventional bandpass delta sigma modulators are also very sensitive to time delay and random jitter in the DAC feedback pulse.

5.2.2 Frequency Translating Architecture Reduces design Requirements of Important Analog Blocks

A simple solution is to down convert the IF signal to baseband and digitize using lowpass delta sigma modulators [8]. Let us consider the conventional direct conversion receiver architecture, Figure 5.2. The low noise amplifier amplifies the weak input signal prior to down conversion. This effectively reduces the noise figure of the mixer by the power gain of the low noise amplifier. However we cannot have a huge gain in the low noise amplifier because a large input signal in the mixer degrades the

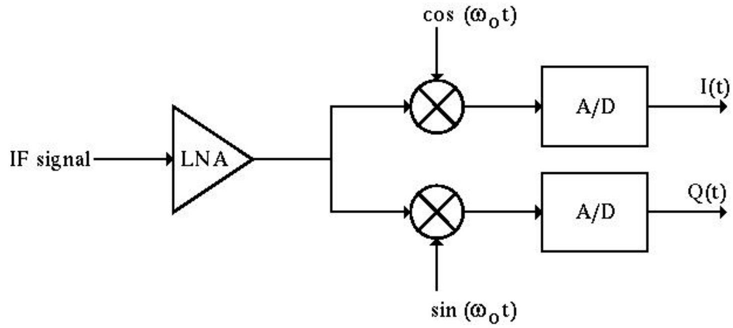

Figure 5.2 Direct conversion receiver

intermodulation performance. Thus there is a trade off here, which limits achievable dynamic range.

The basic idea of frequency translating delta sigma modulators is to integrate the low noise amplifier and mixer in a big feedback loop, where the low noise amplifier suppresses both the noise and intermodulation in the mixer as well as other blocks in the loop. Simplified analysis and system level simulation shows that a 15dB passband gain is enough to achieve good performance. Bandpass filters with 15dB gain are low Q and wideband . Hence do not require accurate tuning. Thus, the design requirements of bandpass resonators are considerably reduced.

5.2.3 Bandpass Basis Function

In conventional delta sigma modulators, the DAC feedback is derived by switching a reference DC current, depending on the quantizer output. Thus, the feedback signal or the basis function is DC. The DAC feedback is usually a rectangular current pulse, the width of the pulse depends on the clock synchronizing the DAC. Random variations in the DAC pulse width appear as noise in the output spectrum of the delta sigma modulator.

In a frequency translating delta sigma modulator, the down converted signal is digitized using a continuous time lowpass delta sigma modulator. The digitized output of the lowpass delta sigma modulator has to be up converted before feeding back to the bandpass filter. Since the digitized lowpass delta sigma output is only two level, we can feedback sinusoid pulse, whose polarity depends on the digitized lowpass delta sigma output. Thus the basis function, in this case is bandpass.

In Chapter 4, we saw that lowpass continuous time delta sigma modulators are insensitive to time delay jitter in DAC feedback pulse. It will be shown in Section 5.6 that conventional bandpass delta sigma are sensitive to time delay jitter. It will be shown that frequency translating delta sigma modulator can be mapped to an equivalent lowpass delta sigma modulator. Frequency translating delta sigma modulators are also insensitive to time delay jitter in the DAC feedback pulse. If we use edge triggered sinusoid pulses for feedback, the DAC jitter performance of frequency translating delta sigma modulator will be better than that of conventional bandpass delta sigma modulator.

5.3. Analysis of Frequency Translating Delta Sigma Modulator

One of the most basic issues in the design of frequency translating delta sigma modulators is that the feedback loop has blocks that are not time invariant. The loop has a down conversion mixer in the forward path and an up conversion mixer in the feedback path. It is well known that mixers are not time invariant. It may seem that the stability of the loop cannot be ensured by traditional method of calculating the poles of the loop transfer function and confining them to the left half plane of $j\omega$ axis.

5.3.1 Linearity of Mixer

Fortunately for the system level designer, this problem solves by itself. First of all an ideal mixer is a linear system. Let $LO(t)$ be the modulating signal. Let the input to the mixer be sum of two signals, $x_1(t)$ and $x_2(t)$. Then the output signal $y(t)$ is given by Eq. 5.1

$$y(t) = (x_1(t) + x_2(t))LO(t) = x_1(t)LO(t) + x_2(t)LO(t) \qquad (5.1)$$

Thus, Eq. 5.1 shows that an ideal mixer is a linear system.

5.3.2 Response of Frequency Translating Block to a Lowpass Input

Although the loop has time variant systems, let us cut the loop to find the loop gain since we don't have anything better to do at the moment. We find that the quantizer output is modulated up by the mixer in the feedback path. The resulting signal is amplified by the bandpass filter. The amplified high frequency signal is down converted to the baseband by the

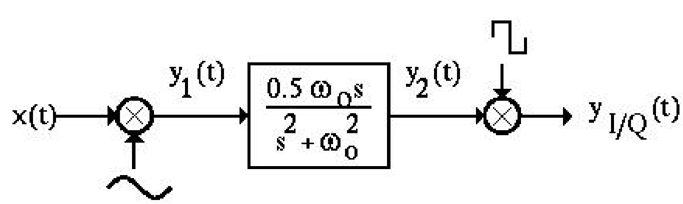

Figure 5.3 Cascade of up conversion mixer, bandpass filter, down conversion mixer

mixer in the forward path. The cascade of up conversion mixer, bandpass filter and down conversion mixer are shown in Figure 5.3.

Let us assume that the input signal, $x(t)$ is a bandlimited lowpass signal, centered around the baseband. The local oscillator frequency is same as the center frequency of the bandpass filter. The input of the bandpass filter is given by Eq. 5.2

$$y_1(t) = x(t)\sin(\omega_o t) \tag{5.2}$$

since the bandpass filter is an LTI system, the output of the bandpass filter is given by Eq. 5.3, where $h(t)$ is the impulse response of the bandpass filter.

$$y_2(t) = h(t) * y_1(t) = \int_{-\infty}^{\infty} h(\tau)x(t-\tau)\sin(\omega_o(t-\tau))d\tau \tag{5.3}$$

$$\sin(\omega_o(t-\tau)) = \sin(\omega_o t)\cos(\omega_o \tau) - \cos(\omega_o t)\sin(\omega_o \tau) \tag{5.4}$$

Substituting Eq. 5.4 in Eq. 5.3, we get

$$y_2(t) = Q_{bp}(t)\sin(\omega_o t) - I_{bp}(t)\cos(\omega_o t), \tag{5.5}$$

$$I_{bp}(t) = \int_{-\infty}^{\infty} h(\tau)\sin(\omega_o \tau)x(t-\tau)d\tau = [h(t)\sin(\omega_o t)] * x(t) \tag{5.6}$$

$$Q_{bp}(t) = \int_{-\infty}^{\infty} h(\tau)\cos(\omega_o \tau)x(t-\tau)d\tau = [h(t)\cos(\omega_o t)] * x(t) \tag{5.7}$$

Thus, the output of the bandpass filter has an inphase component and a quadrature component given by Eqs. 5.6 and 5.7 respectively. The inphase and quadrature signals together determine the output of the bandpass filter. Hence we need to multiply $y_2(t)$, with an inphase LO signal, $\cos(\omega_o t)$ and a quadrature LO signal , $\sin(\omega_o t)$ separately, to get the inphase and quadrature signals.

Let us first focus on the demodulation of the quadrature component of the output of the bandpass filter. The output of the bandpass filter, $y_2(t)$ is demodulated to baseband by a square wave. The square wave is inphase with $\sin(\omega_o t)$ and also has the same frequency. Let us assume that all the high frequency components resulting from the frequency translation is filtered away. Then the down converted quadrature output is given by Eq. 5.8.

$$y_Q(t) = \frac{2}{\pi}\left[h(t)\cos(\omega_o t)\right] * x(t) \tag{5.8}$$

Thus, the cascade of the up conversion mixer, bandpass filter and the down converstion mixer can be replaced with an equivalent filter of impulse response, $h_{eq}(t) = \frac{2}{\pi}\left[h(t)\cos(\omega_o t)\right]$. The impulse response of the bandpass filter in the frequency translating delta sigma modulator shown in Figure 5.1 is given by Eq. 5.9.

$$h(t) = 0.5\omega_o \cos(\omega_o t)u(t), \tag{5.9}$$

Where $u(t)$ is the unit step function. Since we assumed that the input signal is bandlimited, and the high frequency components resulting from demodulation are filtered away, the equivalent impulse response is given by Eq. 5.10.

$$h_{eq}(t) = \frac{2}{\pi}\left[0.5\omega_o \cos(\omega_o t)u(t)\right]\cos(\omega_o t) = \frac{\omega_o}{2\pi}u(t) \tag{5.10}$$

It is obvious that the equivalent impulse response given in Eq. 5.10 is that of an integrator with time constant, $\frac{\omega_o}{2\pi}$. Thus, as far as the quantizer output in the frequency translating delta sigma modulator is concerned, it is processed by an integrator, with time constant, $\frac{\omega_o}{2\pi}$. Note that in an actual frequency translating delta sigma modulator, the high frequency components resulting from the demodulation are filtered away by the lowpass continuous time delta sigma modulator in the loop. Remember that continuous time delta sigma modulators provide free anti alias filtering.

5.3.3 Time Invariance of Frequency Translating Block

Let us delay the input signal by $t = t_o$. Then the input of the bandpass filter is given by Eq. 5.11.

$$y_1(t) = x(t - t_o)\sin(\omega_o t) \tag{5.11}$$

The output of the bandpass filter, $y_2(t)$ is given by Eq. 5.12.

$$y_2(t) = \int_{-\infty}^{\infty} h(\tau)x(t - t_o - \tau)\sin(\omega_o(t - \tau))d\tau \tag{5.12}$$

$$y_2(t) = Q(t - t_o)\sin(\omega_o t) - I(t - t_o)\cos(\omega_o t), \tag{5.13}$$

$$I(t - t_o) = [h(t)\sin(\omega_o t)] * x(t - t_o) \tag{5.14}$$

$$Q(t - t_o) = [h(t)\cos(\omega_o t)] * x(t - t_o) \tag{5.15}$$

Thus, the final demodulated and lowpass filtered output is given by Eq. 5.16. The final output is also time shifted by $t = t_o$. Thus the cascade of up conversion mixer, bandpass filter, down conversion mixer is an LTI system.

$$y_Q(t) = \frac{2}{\pi}\left[h(t)\cos(\omega_o t)\right] * x(t - t_o) \tag{5.16}$$

5.4. System Level Design

Although there are blocks in the delta sigma loop, which are not time invariant, the whole frequency translating delta sigma loop acts like an LTI system. The loop feedback coefficents, a_1, a_2, a_3 should be determined such that the delta-sigma modulator is stable. Let us cut the loop infront of the DAC and go through the loop inorder to determine the loopgain. The NRZ single-bit DAC feedback pulse is modulated up by a sinusoidal wave and is amplified by the bandpass filter. The output of the bandpass filter is downconverted by the local oscillator to the baseband. The transfer function of the bandpass filter is given by Eq. 5.1.

$$H_{bpf} = \frac{0.5\omega_0 s}{s^2 + \omega_0^2}, \tag{5.17}$$

Where ω_0, is the center frequency of the bandpass delta-sigma modulator. The transfer function evaluated at $s = j(\omega_o + \Delta\omega)$, $\frac{\Delta\omega}{\omega_o} << 1$ is given by

$$H_{bpf}(j\Delta\omega) = \frac{\omega_0}{j4\Delta\omega} \tag{5.18}$$

The upconverting mixer, bandpass filter, and the down converting mixer, in Figure 5.3 together act as a lowpass integrator. Since the downconverted signal bandwidth is much smaller than the center frequency of the delta sigma, the sampling frequency of the continuous time delta sigma modulator can be less than the center frequency of the bandpass delta-sigma modulator. Let us assume that the sampling frequency is equal to the center frequency of the delta sigma modulator. The output of the bandpass filter is mixed down by a periodic square wave generated by the local oscillator. The mixer gain is given by Eq. 5.3 [18]. The equivalent integrator transfer function is given by Eq. 5.4, where T is the sampling frequency.

$$G_{mixer} = \frac{2}{\pi} \tag{5.19}$$

$$H_{eq\,\mathrm{int}}(s) = \frac{1}{Ts} \tag{5.20}$$

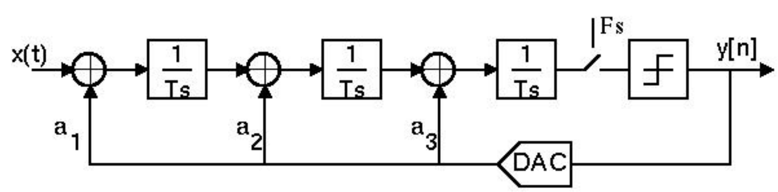

Figure 5.4 Equivalent third order CTLPΔΣM

Thus, the frequency translating delta sigma modulator can be translated in to an equivalent third order continuous time lowpass delta sigma modulator. The equivalent lowpass delta-sigma modulator is shown in Figure 5.3. The feedback coefficients for the equivalent lowpass delta sigma modulator are $a_1 = -0.05$, $a_2 = -0.2$, $a_3 = -0.6416$. The same coefficients can be used for the frequency translating delta-sigma modulator.

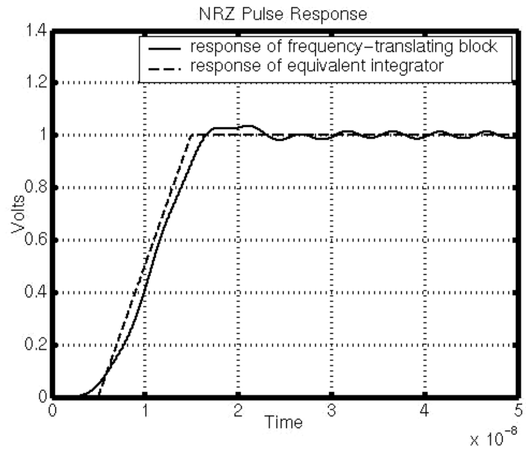

Figure 5.5 Open loop pulse responses of frequency translating block and its equivalent integrator

The response of the frequency translating delta sigma modulator to a modulated NRZ DAC pulse, of 10ns duration is shown in Figure 5.5. The NRZ pulse response of the equivalent lowpass integrator is plotted in the same figure for comparison. Note that a 4^{th} order lowpass Butter Worth filter was used to remove the high frequency signals resulting from mixing down of the output of the bandpass filter. This explains the delay between the two responses. The simulated output spectrum of the continuous time frequency translating bandpass delta-sigma is shown in Figure 5.6. The simulated SNR over 200 KHz bandwidth at an IF frequency of 100 MHz is 95dB.

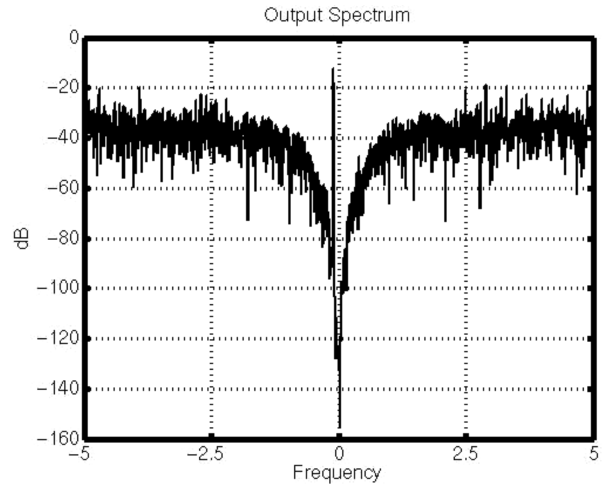

Figure 5.6 Output spectrum of frequency translating modulator

5.5. Jitter Performance of Frequency Translating Delta Sigma Modulator

It was shown in section 5.2 that continuous time frequency translating delta sigma modulators can be mapped to an equivalent lowpass delta sigma modulator. The open loop response of the frequency translating

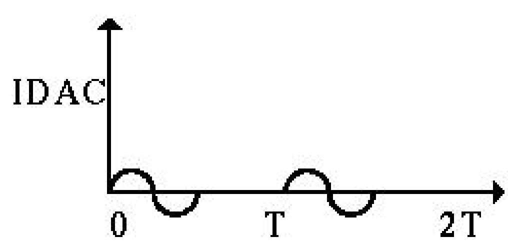

Figure 5.7 Modulated RZ DAC pulse

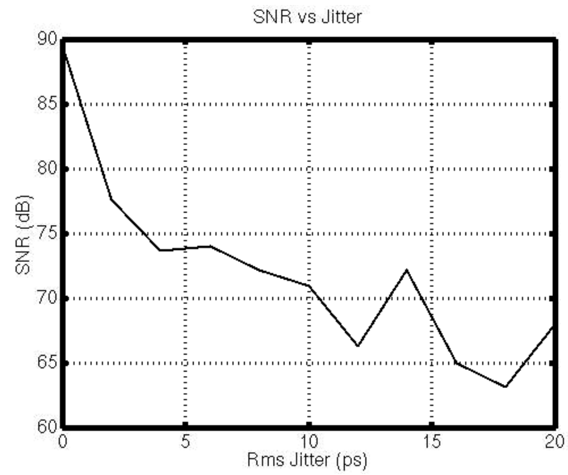

Figure 5.8 SNR vs time delay jitter performance of BPΔΣM

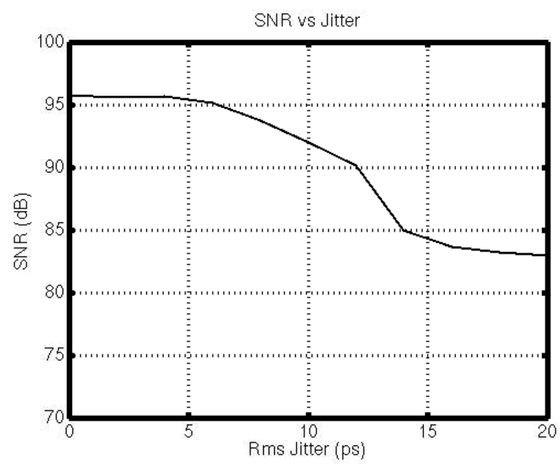

Figure 5.9 SNR vs time delay jitter performance of frequency translating BPΔΣM

modulator to a modulated NRZ pulse is similar to the NRZ pulse response of the equivalent lowpass continuous time modulator. It was shown in chapter 4 that continuous time lowpass delta-sigma modulators are insensitive to time delay jitter in the DAC [11]. Frequency translating delta sigma modulators are also insensitive to time delay jitter in DAC feedback pulse.

Conventional bandpass delta sigma modulators are sensitive to time delay jitter in the DAC feedback pulse. The SNR vs time delay jitter performance of a first order continuous time bandpass delta sigma is shown in Figure 5.8. The center frequency of the modulator is 100 MHz and the sampling frequency is 400 MHz.

The SNR vs time delay jitter plot for a RZ frequency translating bandpass delta-sigma is shown in Figure 5.9. The center frequency of the modulator is 200 MHz and the sampling frequency is 100 MHz. It is evident form Figure 5.9 that frequency translating delta sigma modulator is insensitive to time delay jitter in the DAC feedback pulse.

5.6. Effect of Phase Noise of the Feedback Sine Wave on the Performance of Frequency Translating Delta Sigma Modulator

Frequency translating bandpass delta sigma modulators are sensitive to the non-idealities of the modulating sinusoidal signal in the feedback path. The phase noise in the sine wave is down converted in to the baseband. However it does not modulate high frequency quantization noise in to the baseband. This is because the phase noise is relatively large in the signal band, but the quantization noise is very small in the signal band due to noise shaping. Outside the signal band, the quantization noise dominates, however the phase noise is small. Due to this reason, phase noise in the SDAC feedback pulse is not amplified. The modulator output spectrum with DAC feedback signal corrupted by a single tone is shown in Figure 5.10. The feedback sinusoid is given by Eq. 5.21.

$$V(t) = a_1 \sin(2\pi F_{IF} t + \delta \sin(2\pi F_{tone} t)), \tag{5.21}$$

Where $F_{IF} = 100$ MHz and $F_{tone} = 1$ MHz.

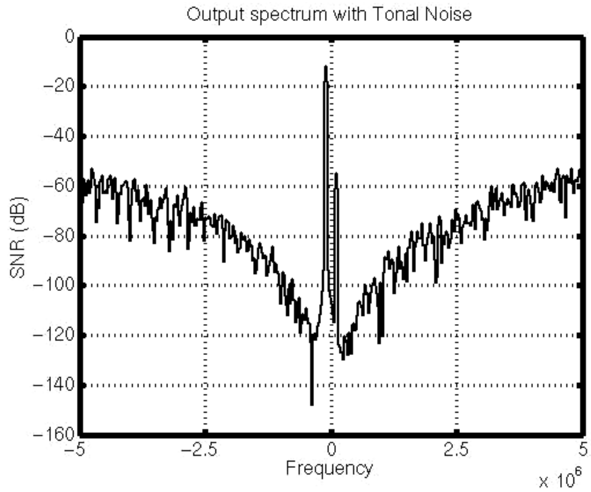

Figure 5.10 Output Spectrum with tonal phase noise in the feedback

6. TRANSISTOR LEVEL DESIGN OF FREQUENCY TRANSLATING DELTA SIGMA MODULATOR

6.1. Architecture

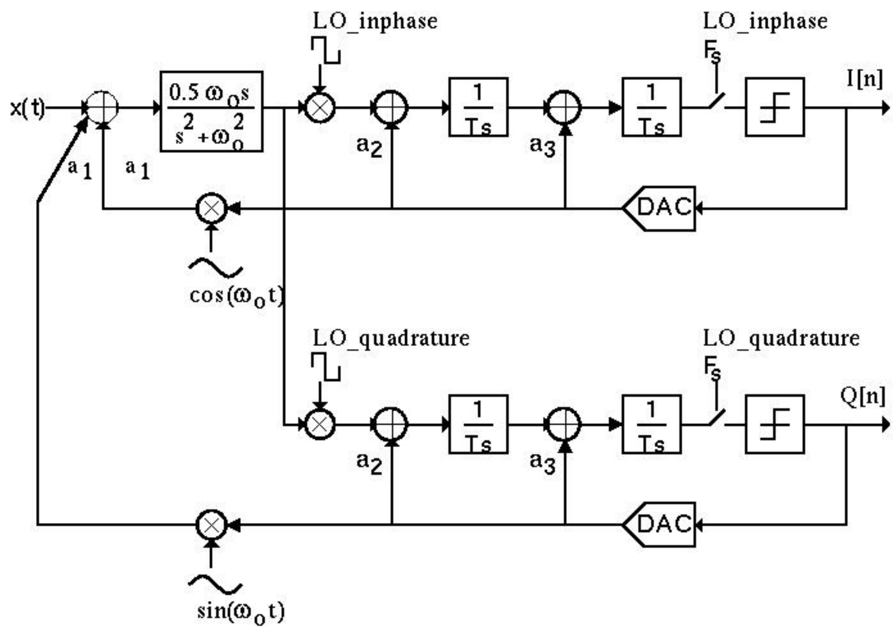

Figure 6.1 Complete delta sigma modulator

As discussed in the pervious chapter, the input IF signal is modulated down to the baseband, inside the delta sigma loop, in a frequency translating delta sigma modulator. Any bandpass signal can be represented in terms of two lowpass signals, given by Eq. 6.1. We need two

$$x_{bp}(t) = I(t)\cos(\omega_o t) + Q(t)\sin(\omega_o t) \tag{6.1}$$

lowpass signals, an inphase component and a quadrature component to represent a bandpass signal. So we need an I-channel delta sigma modulator, which digitize the inphase component and a Q-channel delta sigma, which digitize the quadrature component of the input bandpass signal. The complete delta-sigma modulator architecture is shown in Figure 6.1. The local oscillator signals and the sinusoid signals used for up conversion of quantizer output are shown in Figure 6.2.

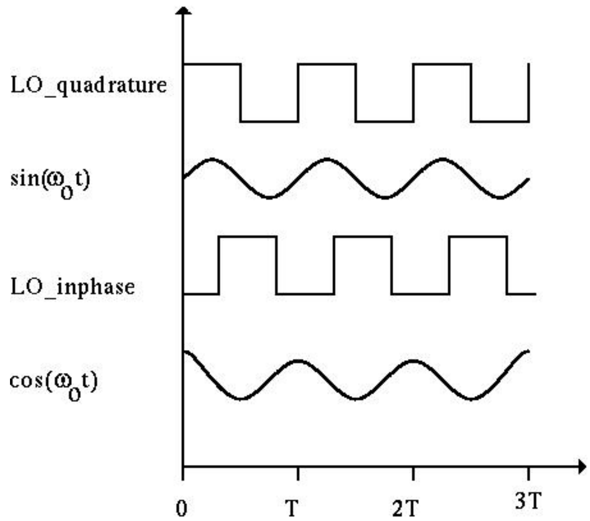

Figure 6.2 Local oscillator and feedback signals

6.2. System Specifications

The design specifications are listed below.

- 100MHz input IF frequency
- 200KHz signal bandwidth
- SNDR should be better than 80dB
- Thermal noise power should be 80dB below the input signal power
- 0.2 Vpp maximum input signal swing
- 3.3V power supply
- TSMC 0.35μm CMOS process

6.3. Bandpass Filter

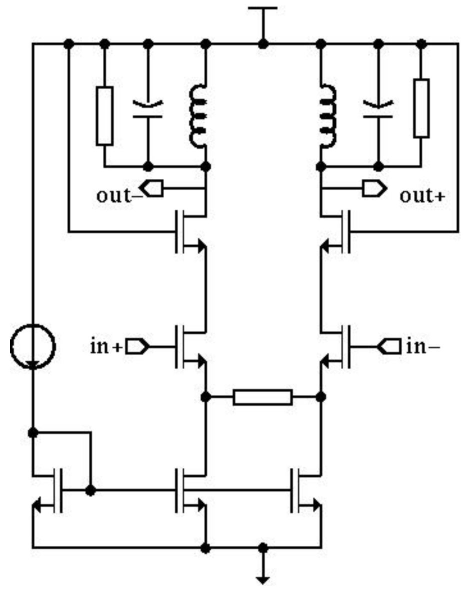

Figure 6.3 Bandpass Resonator

The bandpass resonator is one of the most important blocks in the system. The transistor level implementation of the resonator is shown in Figure 6.3. The resonator is realized as a transconductance stage driving an LC tank tuned to 100 MHz. The transfer function realized by the badndpass resonator is given by Eq. 6.2. The transconductance of the resonator, the inductance and capacitance of the LC tank circuit are given by Eqs. 6.3, 6.4, 6.5. Gm is the transconductance, L is the inductance of the LC tank circuit, C is the capacitance of the LC tank circuit. The inductor in the tank circuit is offchip.

$$H(s) = \frac{0.5\omega_o s}{s^2 + \omega_o^2} \tag{6.2}$$

$$\frac{1}{LC} = \omega_o^2 \qquad (6.3)$$

$$\frac{Gm}{C} = 0.5\omega_o \qquad (6.4)$$

$$Gm = \frac{1}{200}\Omega^{-1},\ \mathrm{L} = 40nH,\ \mathrm{C} = 63.66\mathrm{pF} \qquad (6.5)$$

The bias current and the input transistor sizes are determined by the required intermodulation performance. Assuming square law equation is valid for the input transistors, we can write the Taylor series for the output current of the transconductor with respect to the input voltage. The intermodulation performance can be predicted from Taylor series expansion of the input output characteristics.

Simulations showed that channel length modulation of the input transistors degrade the intermodulation performance considerably and this is not accounted for by the Taylor series expansion of input output characteristics. The input transistors were cascoded to reduce the channel length modulation of input transistors and this improved the intermodulation performance considerably. The expression for intermodulation performance and the values of various design parameters are given by Eqs. 6.7, 6.8, 6.9. The predicted intermodulation from Taylor series expansion is 90dB.

$$IM = \frac{3}{8}\frac{G_m^3 v_{in}^2}{I_b^{2.5}\beta^{0.5}\left[1 + \frac{G_m}{\sqrt{I_b\beta}}\right]^3} \qquad (6.6)$$

$$Gm = \frac{1}{200}\Omega^{-1},\ v_{\mathrm{in}} = 0.2Vpp,\ I_{\mathrm{b}} = 5mA,\ \beta = \frac{\mu \mathrm{C}_{\mathrm{ox}}\frac{w}{l}}{2}, \qquad (6.7)$$

$$\mu C_{ox} = 150 \frac{\mu A}{V^2}, \ \frac{w}{l} = \frac{400}{0.5} \tag{6.8}$$

Figures 6.4, 6.5, 6.6 show the AC transfer characteristics, intermodulation performance and the input referred noise of the bandpass resonator. The main design parameters of the bandpass resonator are summarized in the table below.

Center Frequency	Passband gain	Intermodula-tion	Input referred noise	Power dissipation
100 MHz	15dB	84dB @ 0.2Vpp input signal	$4.6\, nv/\sqrt{Hz}$	35mW

Table 6.1 Design parameters of bandpass filter

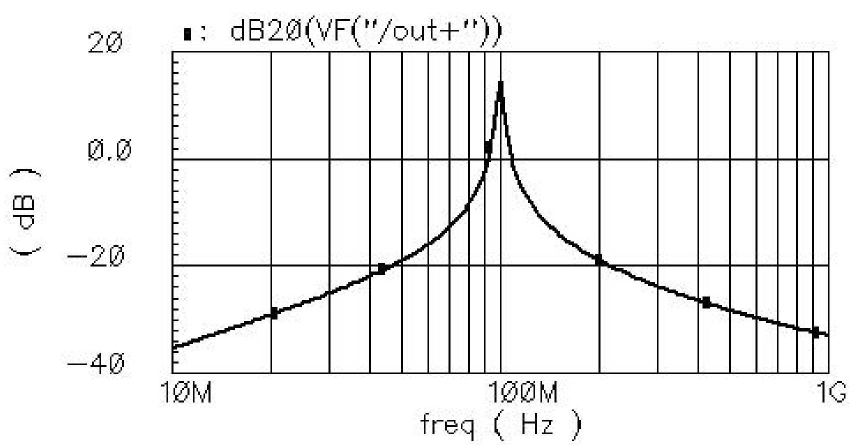

Figure 6.4 AC response of the bandpass resonator

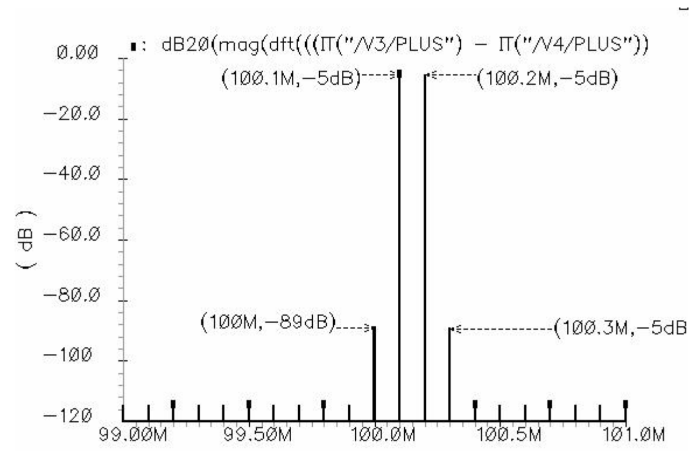

Figure 6.5 Intermodulation performance

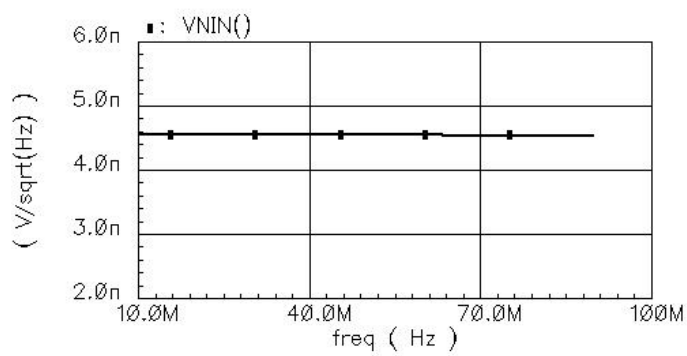

Figure 6.6 Input referred noise of resonator

6.4. Buffer Design

The output filter is down converted to the baseband. The output common mode voltage of the bandpass filter is *Vdd* . Moreover the bandpass filter cannot drive the down conversion mixer. Hence we need a buffer stage which isolated the bandpass filter from the mixer. The buffer stage also should act as a level shifter. A simple common drain amplifier, Figure 6.7 was used as the buffer stage. The intemodulation and the noise performance of the buffer stage are summarized in Table 6.2. Note that the buffer stage is inside the frequency translation loop. Therefore the intermodulation and noise performance of the buffer will be suppressed by the passband gain of the bandpass filter. Thus the closed loop intermodulation and noise performance will be improved by 15dB. The intermodulation and the noise performance are given in Figure 6.8, Figure 6.9 respectively.

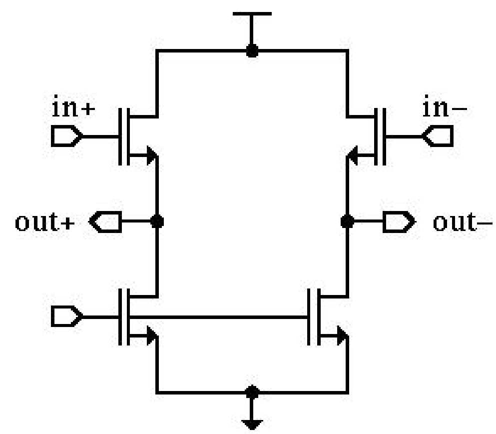

Figure 6.7 Buffer circuit

Intermodulation	Input referred thermal noise	Power dissipation
73dB @ 1vpp input signal	$5nv/\sqrt{Hz}$	6.6 mW

Table 6.2 Design parameters of buffer stage

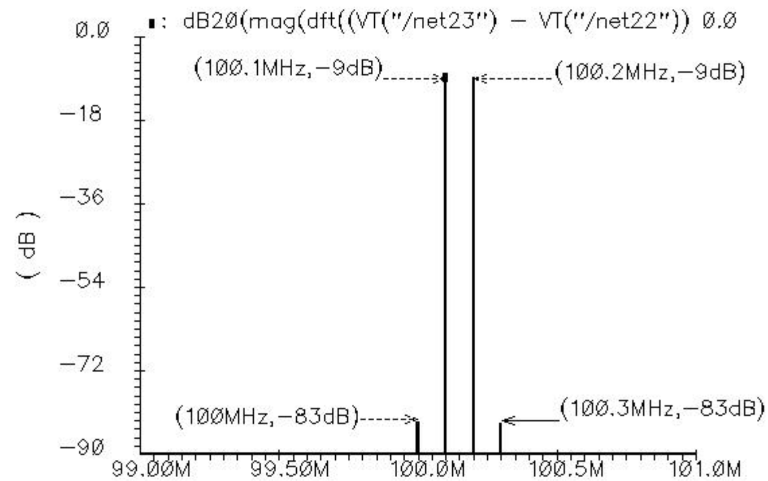

Figure 6.8 Intermodulation performance of Buffer

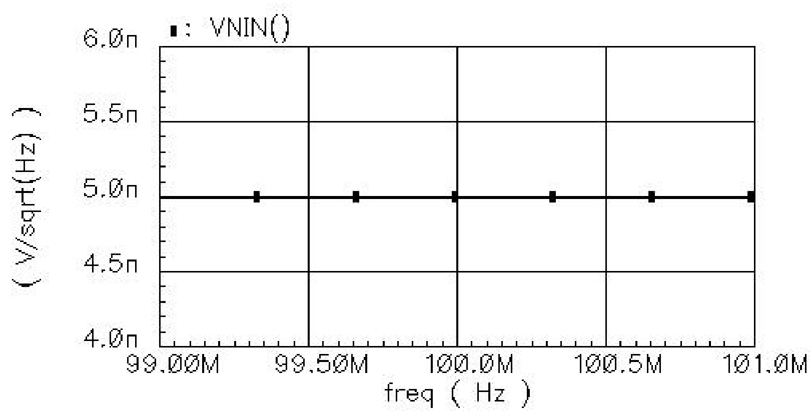

Figure 6.9 Input referred noise of buffer

6.5. Mixer Design

The buffer connected to the output of the bandpass resonator, drives two RC integrators, one for I-channel and the other for Q-channel. The RC integrator form part of the loop filter for the second order continuous time delta sigma modulator within the frequency translating loop. The down

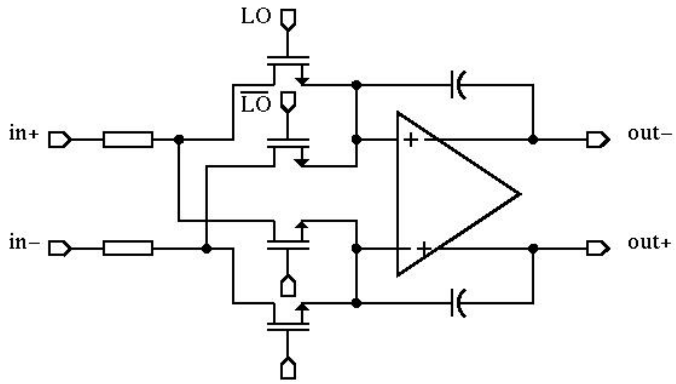

Figure 6.10 Down conversion mixer

conversion mixer, shown in Figure 6.10, is realized using two pairs of nmos switches, connected between the resistors and the virtual ground of the RC integrators [18]. The switches in the mixer are driven by the local oscillator, which is a square wave, with same fundamental frequency as the center frequency of the resonator. The mixer switches couple and cross couples the current in the resistors, depending on the polarity of LO signal.

The conversion gain of the mixer is given by Eq. 6.9 [18]. As mentioned earlier, the input resistors act as linear V/I converters. The mixer switches couples and cross couples the current in the resistors, depending on the polarity of LO signal. The mixer switches are not linear since the on resistance of MOS transistors depends on the drain to source voltage, Vds. Thus the total resistance seen by the buffer stage driving the input resistors will be nonlinear.

The nonlinear dependence of the switch on resistance on Vds is given by Eq. 6.10. Assume that LO is high and $\overline{LO}$ low, then Eq. 6.11 will give the intermodulation performance [18]. The predicted intermodulation is 137dB. It is much less than the simulated intermodulation of 87dB. The intermodulation performance of the integrator with and with out mixer switches, intermodulation performance of actual mixer are summarized in Table 6.3. The intermodulation performance of the mixer corresponding to Table 6.3 are given in Figures 6.11, 6.12, 6.13.

Major sources of thermal noise in the mixer are the input resistors, DAC feedback resistors and the opamp thermal noise. The input referred thermal noise spectral density of the mixer is given by Eq. 6.12. The calculated value of input referred thermal noise is $20nV/\sqrt{Hz}$. However the simulated thermal noise, $38nV/\sqrt{Hz}$ is almost double of the calculated value.

Note that the mixer stage is inside the frequency translation loop. Therefore the intermodulation and noise performance of the mixer will be suppressed by the passband gain of the bandpass filter. Thus the closed loop intermodulation and noise performance will be improved by 15dB.

$$Gain_{mixer} = \frac{2}{\pi} = 0.6366 \tag{6.9}$$

$$r_{on} = \frac{1}{\mu C_{ox}\frac{w}{l}\left(Vgs - Vt - Vds\right)} \tag{6.10}$$

$$IM = \frac{9}{32}\left(\frac{r_{on}}{R_{in}}\right)^3\left(\frac{v_{in}}{Vdd - Vt - Vcm_{in}}\right)^2 \tag{6.11}$$

$$r_{on} = 62\Omega,\ R_{in} = 3k\Omega,\ v_{in} = 1Vpp \tag{6.12}$$

$$Vdd = 3.3,\ Vt = 0.7V,\ Vcm_{in} = 1.4V \tag{6.13}$$

$$P_{th} = 8KTR_{in} + \frac{8KTR_{DAC}}{Gain_{mixer}^2} + \frac{Opamp\ Noise}{Gain_{mixer}^2} \tag{6.14}$$

$$R_{in} = 3k\Omega,\ R_{DAC} = 3k\Omega,\ Opamp\ Noise = 4.84nV / \sqrt{Hz} \qquad (6.15)$$

Intermodulation of integrator with input resistors alone	Intermodulation of integrator with input resistors and mixer switches	Intermodulation of mixer
116dB @1Vpp	87dB @ 1Vpp	70dB @ 1Vpp

Table 6.3 Simulation of intermodulation in mixer

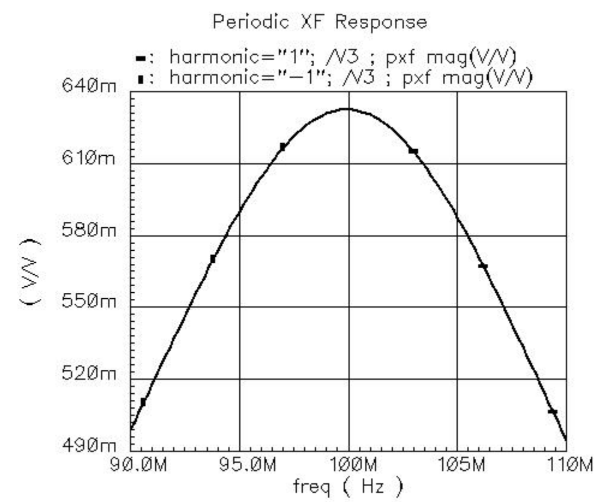

Figure 6.11 Mixer passband gain

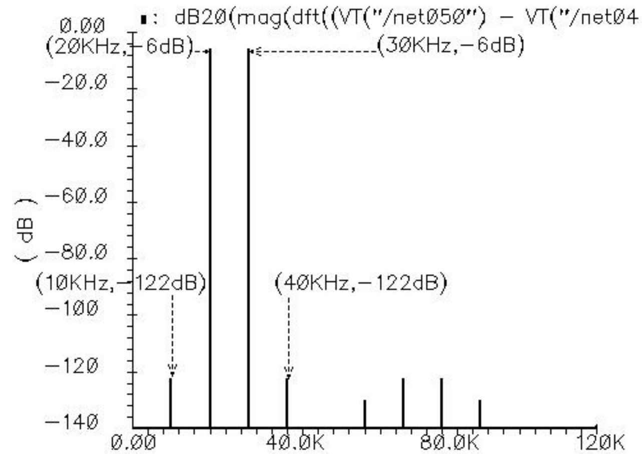

Figure 6.12 Intermodulation of integrator with only input resistors

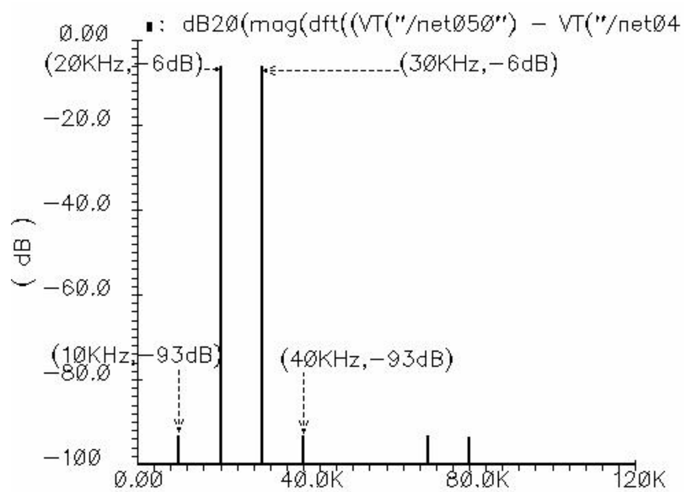

Figure 6.13 Intermodulation of intergrator with input resistors and nonlinear mixer switches

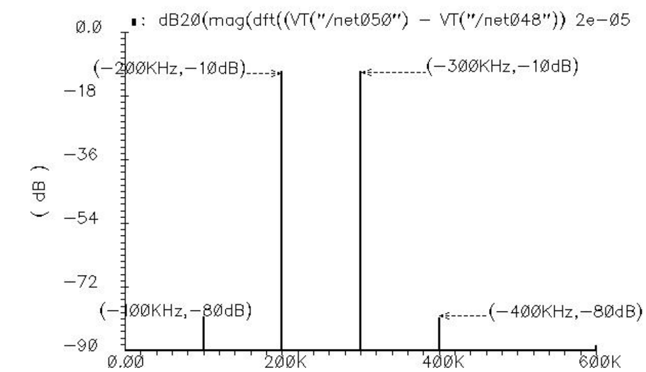

Figure 6.14 Mixer intermodulation Performance

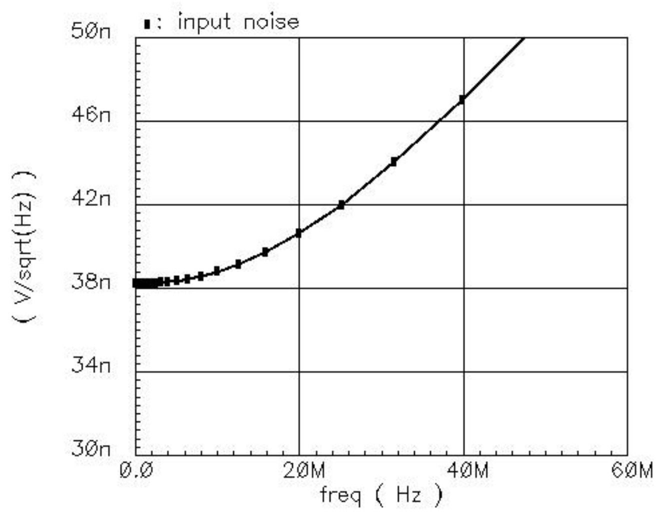

Figure 6.15 Input referred noise of mixer

6.6. Opamps

As discussed earlier, the down converted IF signal is digitized by a second order, continuous time lowpass delta sigma modulator. The opamp of the first integrator of the delta sigma is realized by a simple folded cascode opamp, shown in Figure 6.16. The second stage integrator, Figure 6.17 is realized as a Gm C integrator to avoid resistive loading of the first integrator. The design specification of the folded cascode opamp is given in the table below.

Gain	UGB	Load	Thermal noise
58dB	120 MHz	4pF	$4.84\, nV / \sqrt{Hz}$

Table 6.4 Folded cascode opamp design specifications

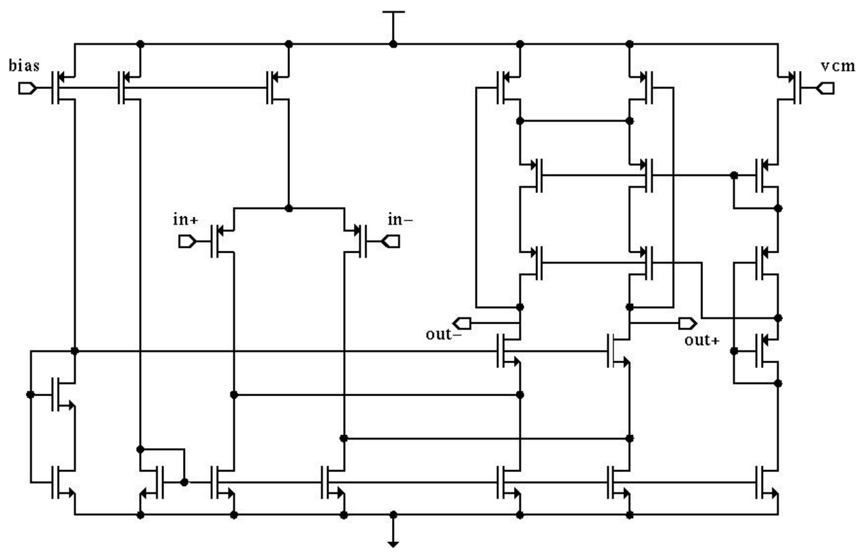

Figure 6.16 Folded cascode opamp

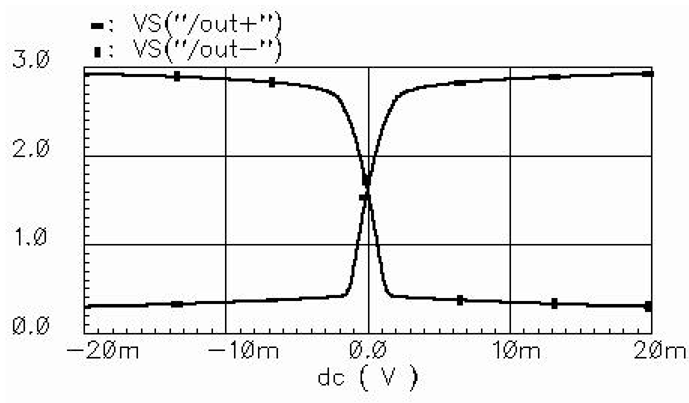

Figure 6.17 DC response of Folded cascode opamp

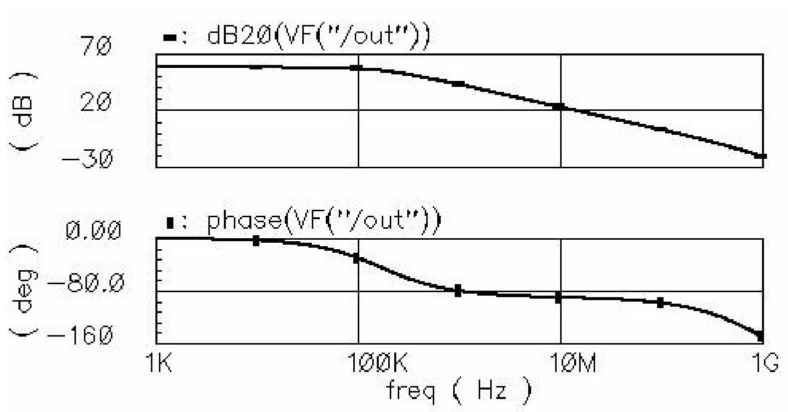

Figure 6.18 AC response of folded cascode opamp

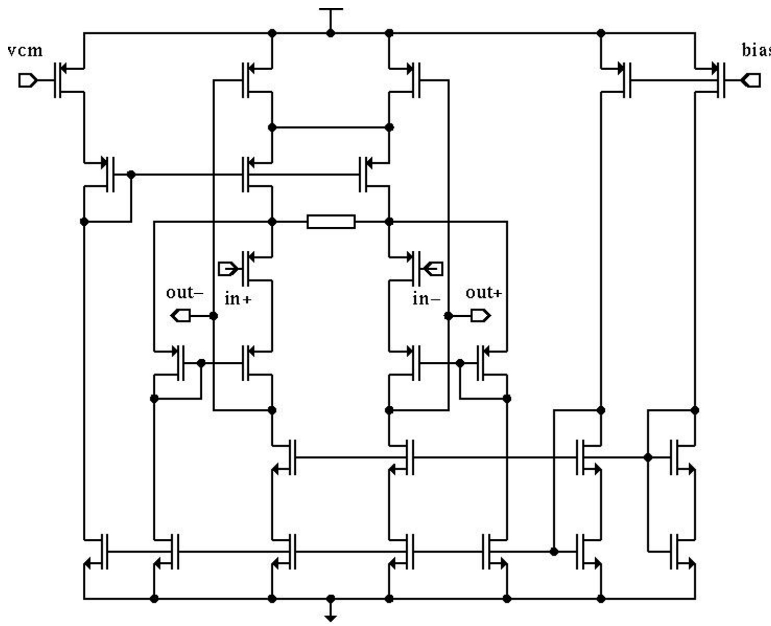

Figure 6.19 Telescopic opamp in GmC integrator

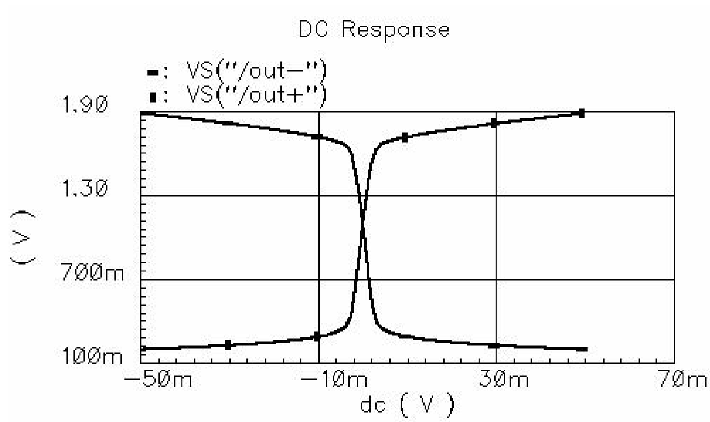

Figure 6.20 DC response telescopic opamp

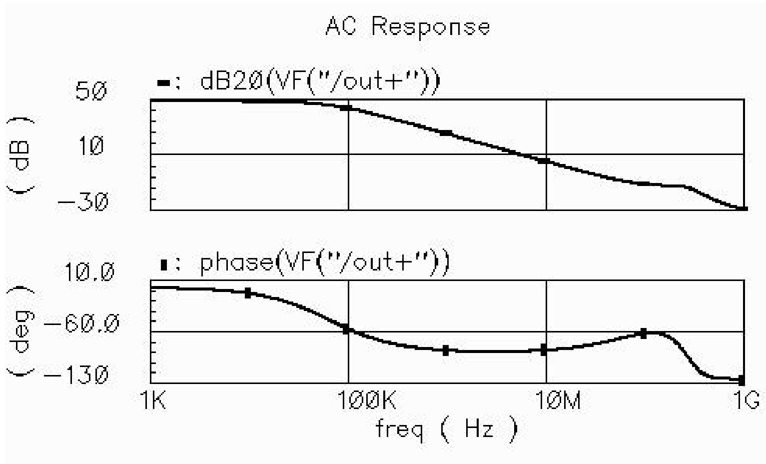

Figure 6.21 AC response of the GmC integrator

6.7. Sinusoidal Feedback DAC

As discussed earlier the digital output of the continuous time delta sigma modulator is upconverted and fedback to the bandpass resonator. The sinusoidal feedback DAC, Figure 6.22, is similar to a Gilbert cell. The input sinusoidal voltage is converted in to current by a V-I converter. The Gilbert cell mixer will switch the polarity of the sinusoidal current depending on the comparator output of the lowpass delta sigma. The feedback current is determined by the feedback coefficient, a_1, and the transconductance of the V/I converter of the input bandpass filter.

$$I_{SDAC} = a_1 Gm = 1mA, \quad (6.16)$$

$$a_1 = 0.2, \; Gm = \frac{1}{200}\Omega^{-1} \quad (6.17)$$

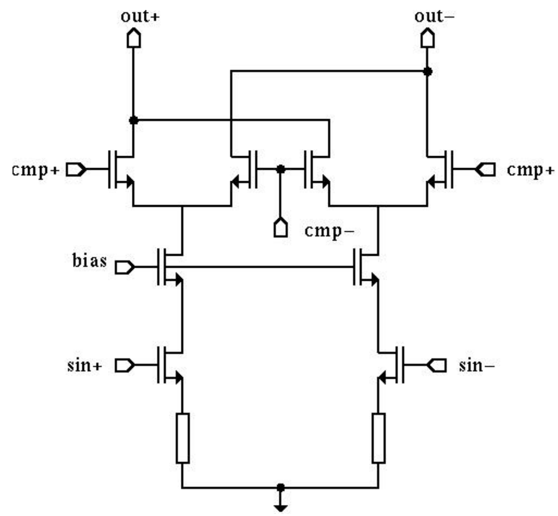

Figure 6.22 SDAC

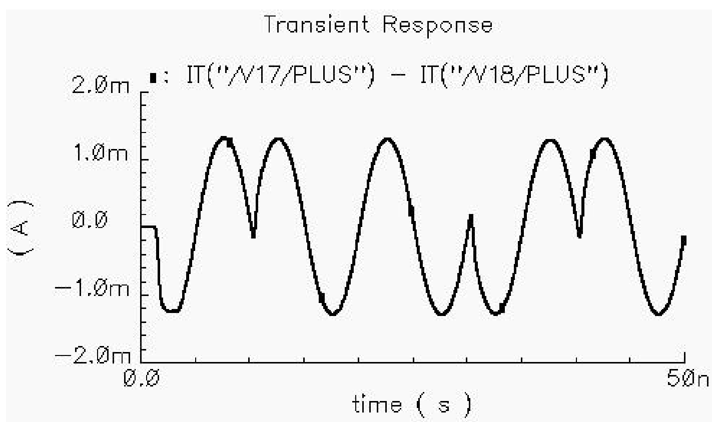

Figure 6.23 SDAC response to comparator

6.8. RDAC and CDAC

The down converted IF signal in a frequency translating delta sigma modulator is digitized using a continuous time second order lowpass delta sigma modulator. The DAC for the first stage integrator of the lowpass delta sigma modulator is shown in Figure 6.24. It realized by switching a pair of resistors to reference voltage, depending on the quantizer output. The DAC for the second integrator is a simple current switching DAC, shown in Figure 6.25.

The DAC feedack current for the RDAC depends on the feedback coefficient, a_2 and the input resistor in the first stage RC integrator. The RDAC feedback current is given by Eq. 6.18. The DAC feedack current for the RDAC depends on the feedback coefficient, a_3 and the transconductance of the first stage GmC integrator. The RDAC feedback current is given by Eq. 6.19.

$$I_{RDAC} = \frac{a_2}{R_{in}} = 100\mu A \quad (6.18)$$

$$a_2 = 0.3,\ R_{in} = 3k\Omega \quad (6.19)$$

$$I_{CDAC} = a_3 Gm = 128\mu A \quad (6.20)$$

$$a_3 = 0.6416,\ Gm = 200\frac{\mu A}{V} \quad (6.21)$$

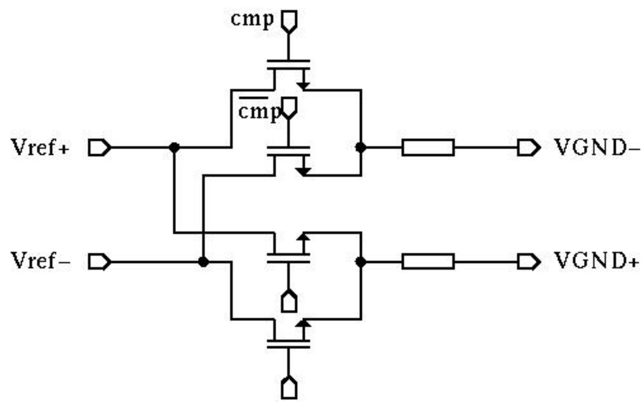

Figure 6.24 RDAC

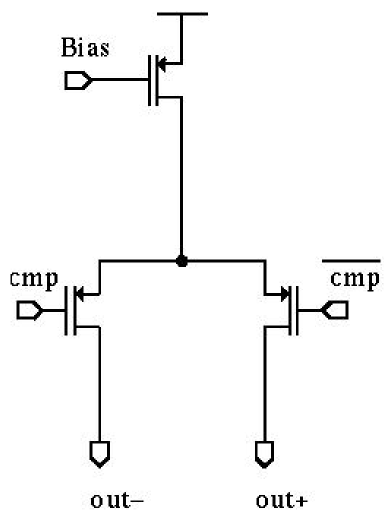

Figure 6.25 CDAC

6.9. Transistor Level Simulation Result

The output spectrum from transistor level simulations for an input signal 1 MHz offset from the center frequency is shown in Figure 6.26.

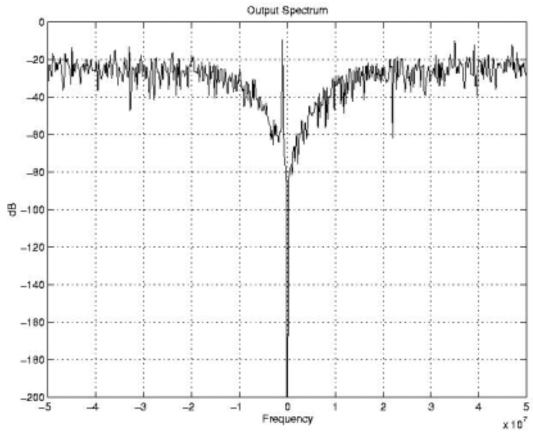

Figure 6.26 Output spectrum from transistor level Simulation

7. CONCLUSIONS

The basic concept of frequency translating continuous time bandpass delta sigma modulation is presented. Frequency translating delta sigma modulators are well suited for digitizing IF signals in radio receivers. It is shown that frequency translating delta sigma modulators can be mapped in to an equivalent, continuous time lowpass delta sigma modulator.

The performance of continuous time delta sigma modulators is investigated in detail and it is shown that continuous time lowpass delta-sigma modulators are less sensitive to time delay jitter in the DAC feedback pulse. The same property holds good for frequency translating delta sigma modulators. A modified DAC feedback scheme to improve DAC jitter performance of continuous time lowpass delta sigma modulators is proposed. A similar technique can be used to improve the jitter performance of frequency translating delta sigma modulators.

A simple design methodology for the system level design of frequency translating modulators is presented. A prototype frequency translating delta sigma modulator is implemented in $0.35\mu m$, CMOS process to prove the concept. All the important blocks in the system are characterized interms of intermodulation performance and input referred thermal noise. Transistor level simulations show that 80dB SNR can be achieved with 100mW of static power dissipation.

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