An Efficient Switched Capacitor Buck-Boost Voltage Regulator

Using Delta-Sigma Control Loop

by

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1. INTRODUCTION

1.1. Background

Small electronic devices are commonly powered by batteries, which allow such devices to be portable. However as the battery use continues, the battery voltage drops depending on the type of battery and type of device. Such variation in the battery voltage may have undesirable effects on the operation of the electronic device powered by the battery. Consequently, DC-DC converters are often used to provide a constant and stable supply voltage from the battery to the electronic device.

For many years the inductive conversion topology has been the standard solution to providing a constant and stable voltage from a battery. This is mainly due to the wide variety of possibilities in current and voltage requirements. With the continued shrinking of the hand held devices as cell phones, PDA's, pagers and laptops, the use of traditional inductive based regulators is becoming less attractive. The bulkier inductive based regulator is being replaced by the compact switched capacitor regulator. The inductive DC/DC conversion uses a magnetic coil, while the switched-capacitor uses capacitors and an array of switches. The switching network is responsible for charging and discharging the capacitors in order to achieve different voltages.

Some of the primary reasons to choose capacitive DC/DC conversion over inductive are reduced electromagnetic induction (EMI) and reduced high frequency noise. These noise sources interfere with systems using radio receivers and transmitters. Filtering is essential to avoid unreliable operation and this adds to board space and cost.

Switched-capacitors, on the other hand, do not produce substantial EMI noise, however the supply voltage may suffer from current spikes during the capacitor recharge depending on the load current. Another issue not addressed in any prior literature is the tones or harmonics on the output of the regulated switched-capacitor converters.

Switched-capacitor regulators also tend to be more efficient for lower input voltages. This can help in improving the lifetime of the battery or smaller batteries are sufficient for the same charge time. Thus switched-capacitor power conversion offers physical volume, radiated EMI, efficiency and cost advantages as peak power requirement fall below 1 Watt.

1.2. Motivation

The existing switched-capacitor regulators suffer from a very tonal frequency response. These tones occur at unpredictable frequencies and hence difficult to filter. In addition these tones might mix with the signal frequencies in higher bandwidths and modulate as noise in the frequency region of operation. In this thesis, an alternate method to control existing switched-capacitor regulators is proposed. It will be shown that this method reduces tones in existing architectures of switched-capacitor regulators.

1.3. Organization Of Thesis.

The thesis is organized as follows. A standard regulator architecture is explained in Section 2. Some common switched-capacitor gain structures are explored and their operation is described briefly in Section 3. The modelling of the switched-capacitor gain structures is described in Section 4. An alternate control loop is proposed for the switched-capacitor regulator in Section 5. We also compare the proposed architecture to the existing control loop. Circuit design and implementation of the regulator are presented in Section 6. Experimental results of the chip are presented in Section 7. Conclusions are provided in Section 8.

2. REGULATOR ARCHITECTURE

There are two basic kinds of DC/DC converters, the *boost* and the *buck*. A *boost* converter will have a gain that is greater than or equal to one, while a *buck* converter will have a gain that is less than one. During the first part of the battery's life, when the battery voltage may be greater than the desired supply voltage, a *buck* converter can be used to provide an output voltage less than the battery voltage. During the second part of the battery's life, when the battery voltage may be less then the desired supply voltage, a *boost* converter can be used to provide an output voltage greater than the battery voltage.

A typical discharge curve for a lithium ion (LiIon) battery for a 100mA constant current discharge, is shown in Fig. 2.1. When freshly charged, a LiIon battery supplies a voltage of about 4V. As time progresses, depending on the load, the voltage can drop to as low as 2.5V.

Thus by changing the gain of a regulator we can compensate for the variation in the battery voltage. In addition to this, we also need to regulate the battery voltage at a constant desired voltage.

2.1. LM3352 Architecture

A conventional method to regulate voltage in a DC-DC converter is to use *pulse frequency modulation* (PFM) or pulse skipping. The basic principle of this scheme is shown in Fig. 2.2. If the output voltage V_{out} is less then the desired voltage $V_{desired}$, the regulator is switched on. This causes charge to be transferred to the output and the output voltage increases. Similarly if V_{out} is more then $V_{desired}$

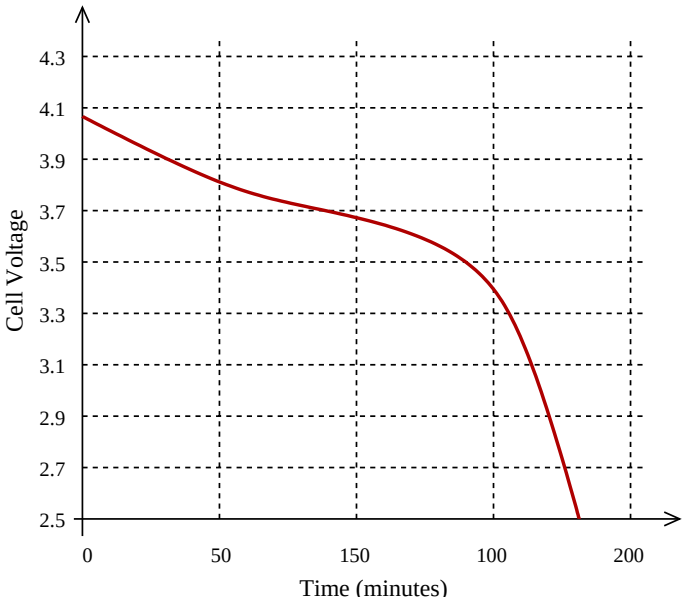

Figure 2.1. LiIon discharge using graphite core.

the regulator is switched off. This switching on and off of the regulator is done by clocking the regulator with the *gated clock*.

One such architecture for such an application was presented in [1]. The block diagram of the architecture is shown in Fig. 2.3. We see that the regulator has two control loops, the *PFM* loop and gain hopping loop.

The purpose of the *PFM* loop is to regulate the output voltage to a desired value. This loop is composed of a reference generator, a comparator and an oscillator. The reference generator generates the desired voltage $V_{desired}$. V_{out} is compared with $V_{desired}$ by the comparator. The output of the comparator is the *skip* signal. If V_{out} is less then $V_{desired}$, *skip* is low and the regulator is idle. If V_{out} is greater then $V_{desired}$, *skip* is high and the regulator is clocked.

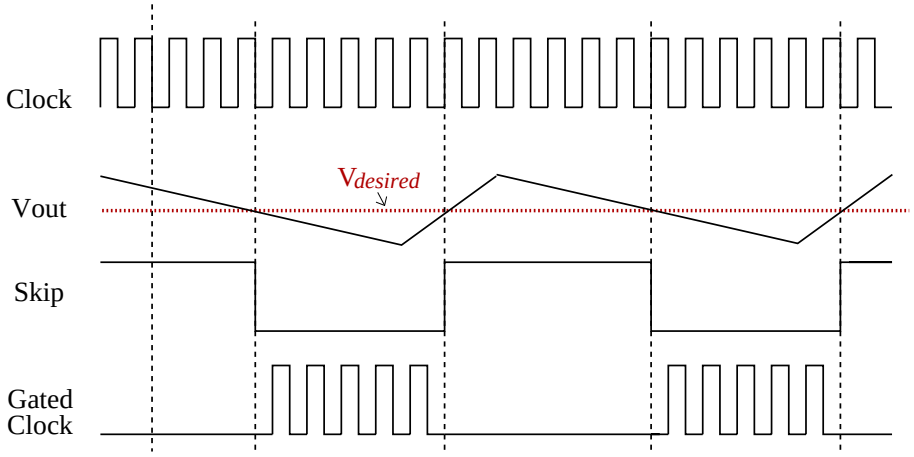

Figure 2.2. PFM control waveforms.

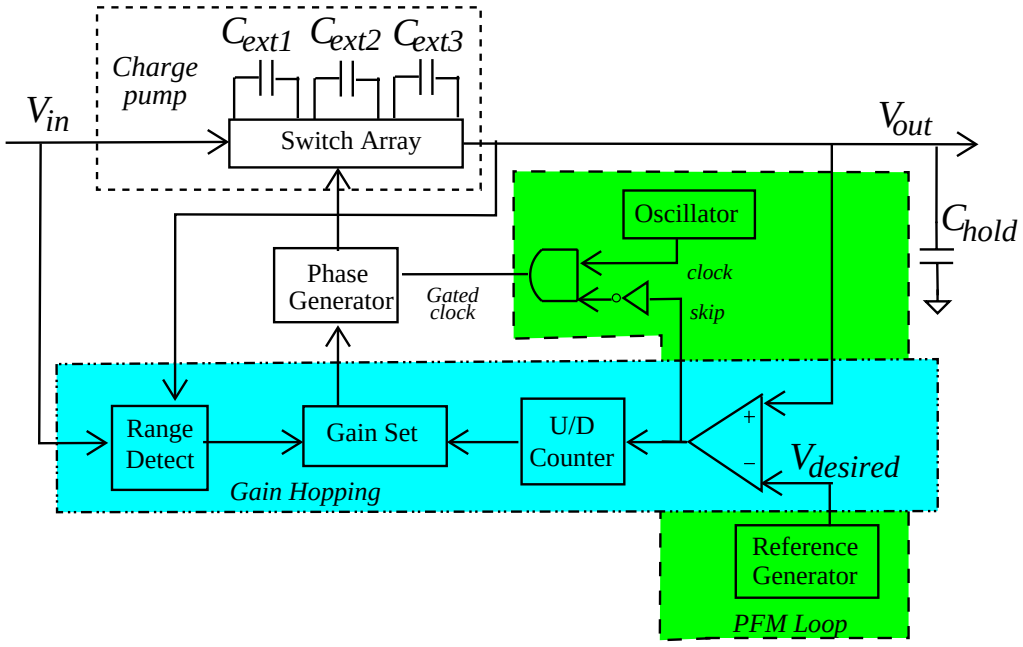

Figure 2.3. Block diagram of LM3352 voltage regulator.

When the regulator is clocked, the external capacitors C_{ext1}, C_{ext2} and C_{ext3} are connected in one of seven gain configurations. This is referred to as the *gain* phase. When the regulator is not clocked, capacitors C_{ext1}, C_{ext2} and C_{ext3} are all connected in parallel between V_{out} and V_{in}. This is referred to as the *common* phase. In the *gain* phase, depending on the gain setting, a certain amount of charge is transferred to or removed from the output, increasing or decreasing the output voltage. Hence the *PFM* loop provides the necessary pulse skipping to regulate the output voltage.

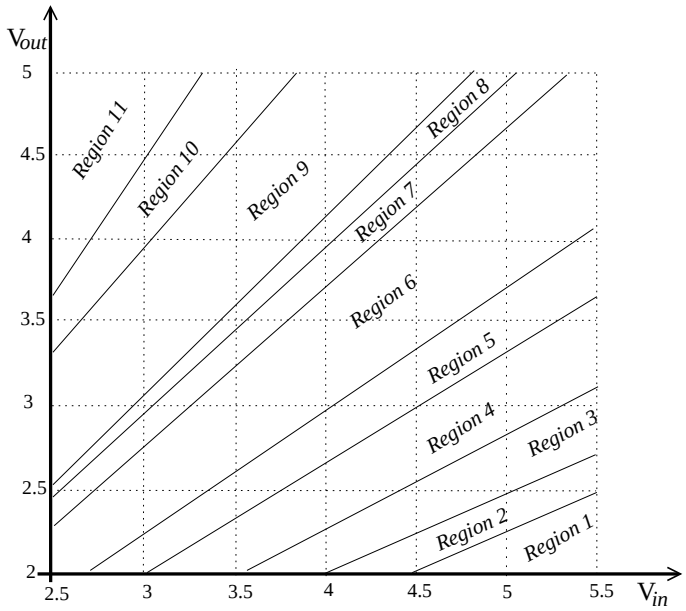

Figure 2.4. Gain map.

The purpose of the *gain hopping* loop is to provide an output voltage greater or less then the battery voltage. As the battery voltage drops, the gain of the regulator has to increase to maintain a constant output voltage. This is accomplished

Region	Max. Gain	Min. Gain
1	2/3	1/2
2	2/3	1/2
3	3/4	2/3
4	1	2/3
5	1	3/4
6	1	1
7	4/3	1
8	3/2	4/3
9	2	4/3
10	2	4/3
11	2	2

Table 2.1. Maximum and minimum gain values for different regions on gain map

by configuring C_{ext1}, C_{ext2} and C_{ext3} into one of seven gain settings with the help of the switch array. The different gains that are possible are 2, 3/2, 4/3, 1, 3/4, 2/3 and 1/2. These will be explained in detail in the following chapter. The three external capacitors are equal in size and they dump charge on the hold capacitor C_{hold} connected to the output in the *gain* phase. The size of $C_{ext1,2,3}$ determines the charge transfer capacity of the configuration. Likewise, the size of C_{hold} determines the amount of ripple. The larger the value of C_{hold}, the smaller the value of the ripple at a given load. A larger C_{hold} of course also means larger size.

There are several constraints to be followed while selecting the *gain* for the regulator. First, we must ensure that $V_{desired} < G_{min} * V_{in}$, where G_{min} is the minimum gain that must be used. This is to make sure that it is possible to obtain the required V_{out} for a given V_{in}. If the above condition is not satisfied, V_{in} can never reach V_{out}. For example, if V_{in} is 2.5V and $V_{desired}$ is 4.5 V, then G_{min} has to be 2. If a gain of 3/2 is used instead, V_{out} will never reach $V_{desired}$.

When the switched capacitor circuit switches from *common* to *gain* phase and vice versa, the voltage at the intermediate nodes can go to values beyond those prescribed by voltage management rules. The voltage management rules ensure that none of the voltages of the circuit are higher or lower by a diode drop of about 0.7 V than the highest or lowest voltage on the chip. If this is not met, parasitic diodes might be forward biased causing large substrate currents. This problem can be solved using three techniques described below:

1. Make the switch size large. This causes the switch to have a very small on resistance (R_{on}) and reduces the voltage drop across it.

2. Use phase shifted clocks. This means rather than switching all the switches at once, switching them in sequence. This is accomplished by the *phase generator* block.

3. Limit the gain of the regulator such that in a particular gain no node voltage goes above or below the supply or ground by more then 0.7 V. Thus there is a maximum gain, G_{max}, depending on the input and output voltages. The G_{max} is set so that the above stated rules are met for all gain configurations. This was determined by extensive simulations and ensured by the *range detect* block.

The *range detect*, essentially an analog to digital converter, sets the above mentioned G_{max} and G_{min} levels. The output of the *range detect* are two 3-bit codes specifying the G_{max} and G_{min} levels for a given V_{out} and V_{in}. The entire range of V_{out} and V_{in} can be divided into *gain regions*, each having a G_{max} and G_{min} associated to it.

The plot of various possible gain regions, depending on the input and output voltage, are shown in Fig. 2.4. The minimum and the maximum gains, G_{min} and G_{max}, for each region are given in Table 2.1. For example consider the case in which V_{out} is 2.5V and V_{in} is 4.5V. The Fig. 2.4 shows that the regulator will be in *Region3*. This means that, from Table 2.1 , G_{min} will be 2/3 and G_{max} is 3/4.

The *gain hopping* loop consists of a counter, range detect and a gain set block. The counter counts the number of *skip*, K and $\overline{skip}$ (*pumps*), M. If $pumps = 1$ for 4 consecutive clock cycles (M=4), the gain is increased. If $skip = 1$ for 3 consecutive cycles (K=3), the gain is decreased. The counter resets after every gain change. In general, M should be greater than K for greater efficiency. By making it harder to increase the gain, a lower gain setting is maintained for a longer period of time, thereby increasing the efficiency. The gain set block chooses the gain of the regulator.

The gain selected by the *counter* goes to a digital comparator in the gain set block. Here it is compared to the maximum and minimum gains (G_{max} and G_{min}) provided by the *range detect* block. If the selected gain is higher then G_{max} or if it is lower then G_{min}, the maximum or minimum gains are selected respectively.

Thus the correct gain to be used is provided by the *gain hopping* loop and the *pump* or *skip* signal during each of these gain settings is provided by the *PFM* loop.

2.2. Drawbacks

The gain selection in the regulator is done by the gain hopping loop explained above. If I_{load}, V_{in} and $V_{desired}$ do not change, the gain hopping loop will select the same pattern of gain and *skip* over a period of time and the duty cycle of the output voltage remains fixed. This corresponds to a tonal spectrum. Figure 2.5 shows the time domain and spectrum of the LM3352 with I_{load} of 100mA, V_{in} of 2.4V and $V_{desired}$ of 3.3V. The tones in the frequency spectrum are difficult to filter and can degrade the performance of the overall system.

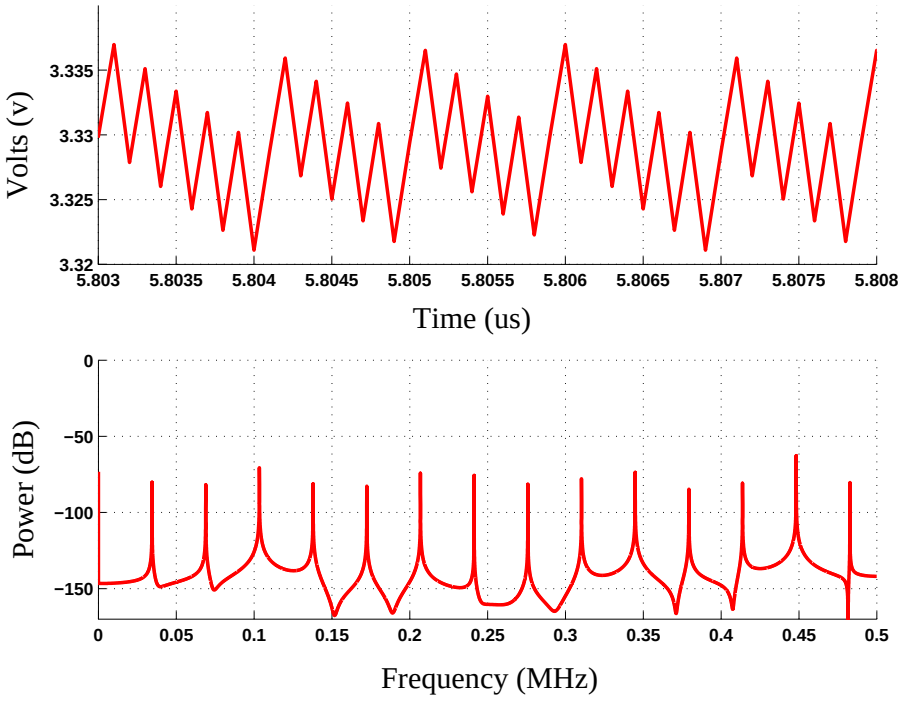

Figure 2.5. Typical time and spectrum plots for LM3352.

3. BUCK AND BOOST SWITCHED CAPACITOR STRUCTURES

As explained in the previous chapter, if $V_{out} < V_{desired}$, the regulator is clocked. If $V_{out} > V_{desired}$ the regulator is not clocked. As shown in Fig. 3.1, when the regulator is clocked, the *gain* and *common* phase alternate. If the regulator is not clocked it remains in the *common* phase.

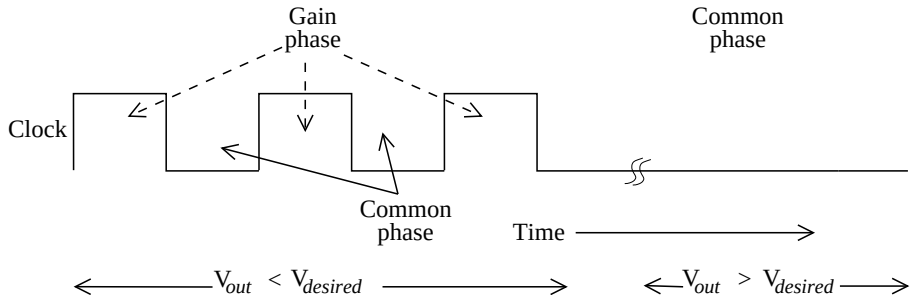

Figure 3.1. State of Regulator under different output conditions.

As mentioned before, during the *gain* phase the external capacitors are connected in one of seven configurations, while in the *common* phase all the three external capacitors are connected in parallel between V_{in} and V_{out}. It is this alternation between the *gain* and *common* phases that provides the specified gain. The different *buck* and *boost* structures are introduced in [1].

3.1. Boost Structures

A *boost* stage has a gain greater than 1. We have 3 different *boost* configurations. They provide the gains of 2, 3/2 and 4/3. The gain of 2 is shown in Fig. 3.2. In the *gain* phase, the voltage across C_{ext2} and C_{ext3} is given by Eq. 3.1. In the

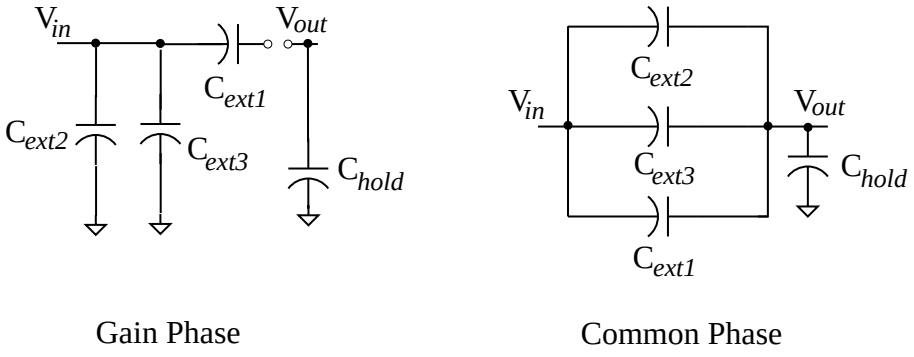

Figure 3.2. Configuration for gain = 2.

common phase the three capacitors are connected in parallel between V_{in} and V_{out}. Equation 3.2 shows the final output voltage at the end of the *common* phase.

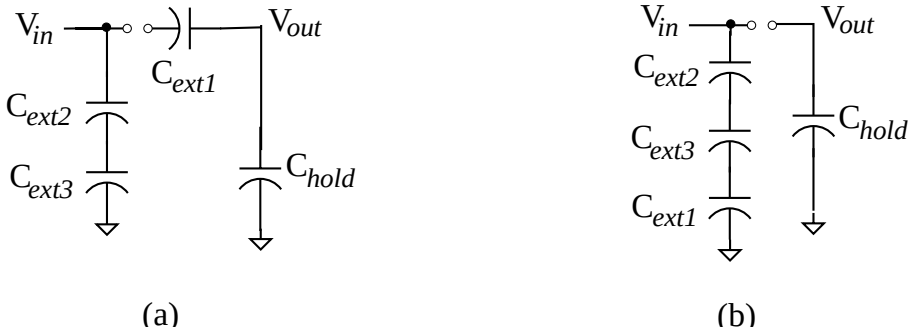

Figure 3.3. Configuration for (a) gain = 3/2 and (b) gain = 4/3.

Thus, by alternating between the two phases we achieve a gain of 2. It should be mentioned that in the gain of 2 configuration, we can have all the three

capacitors charged to V_{in}. This would increase the charge delivering capability of the configuration.

Therefore in the *gain* phase,

$$V_{Cext2} = V_{Cext3} = V_{in} \tag{3.1}$$

where V_{Cext2} is the voltage across C_{ext2}.

While in the *common* phase,

$$\begin{aligned} V_{out} &= V_{Cext3,2} + V_{in} \\ &= V_{in} + V_{in} \\ &= 2 * V_{in} \\ \Rightarrow \frac{V_{out}}{V_{in}} &= Gain = \frac{2}{1} \end{aligned} \tag{3.2}$$

The same can be explained for the gains of 3/2 and 4/3 shown in Fig. 3.3. For the gain of 3/2, C_{ext3} and C_{ext2} are each charged to $V_{in}/2$. In the *common* phase the capacitors are connected in series with V_{in} to get a gain of 3/2. Similarly, in the *gain* phase for the gain of 4/3, C_{ext3}, C_{ext2} and C_{ext1} are each charged to $V_{in}/3$. In the common phase the are connected in series with V_{in} to provide a gain of 4/3.

3.2. Buck Structures

The buck stages have a gain that is equal to or less than 1. There are 4 buck stages that are used in the implementation. They provide the gains of 1/2, 2/3, 3/4 and 1. The gain of 1/2 is shown in Fig. 3.4. In the *gain* phase one of the external capacitors, C_{ext2}, is charged to $-V_{out}$ as shown in Eq. 3.3. In the *common* phase C_{ext2} is connected in series with V_{in}. This provides a gain of 1/2 as shown by Eq. 3.4.

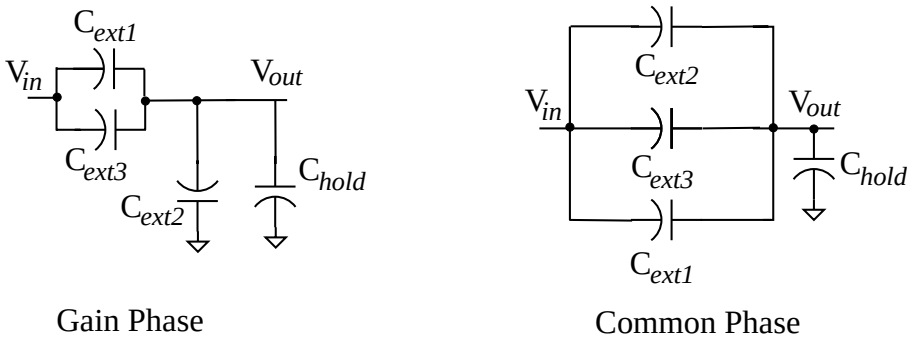

Figure 3.4. Configuration for gain = 1/2.

In the *gain* phase,

$$V_{Cext2} = -V_{out} \tag{3.3}$$

In the *common* phase,

$$\begin{aligned} V_{out} &= V_{Cext2} + V_{in} \\ &= -V_{out} + V_{in} \\ &= \frac{1}{2} * V_{in} \\ \Rightarrow \frac{V_{out}}{V_{in}} &= Gain = \frac{1}{2} \end{aligned} \tag{3.4}$$

Gains of 1, 2/3, 3/4 are shown in Fig. 3.5. In the gain of 1, the external capacitors are charged between V_{in} and V_{out} in the *gain* phase. In the *common* phase they are flipped and again connected between V_{in} and V_{out}. We can see that all the three external capacitors can be used to increase the charge delivery capacity of the stage.

In the *gain* phase of gain 2/3, the external capacitors are charged to $-V_{out}/2$ (by charging two of them in series) before being connected in series with V_{in} in the

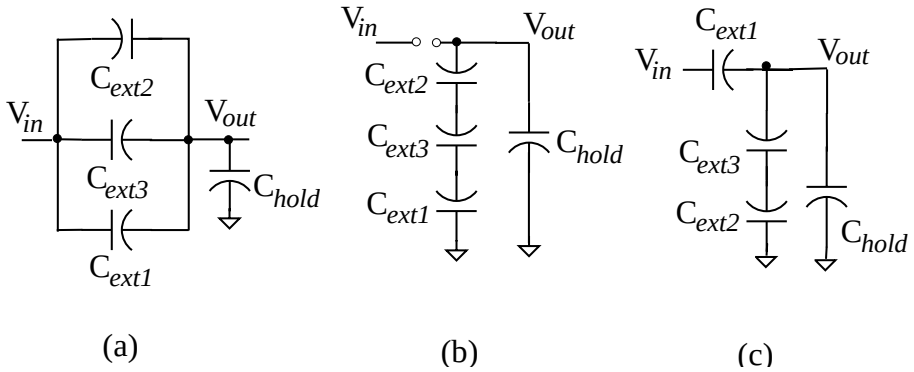

Figure 3.5. Configuration for (a) gain = 1, (b) gain = 3/4 and (c) gain = 2/3.

common phase. In the gain of 3/4 the external capacitors are charged to $-V_{out}/3$. This is accomplished by charging all the three external capacitors in series to V_{out}. Since they are equally sized, each has a charge of $V_{out}/3$. The negative sign comes as the capacitors are flipped over in the *common* phase. Using the above configurations in a feedback loop we can generate a regulated voltage from an unregulated battery.

4. SWITCHED CAPACITOR REGULATOR MODELLING

In order to simulate the regulator at the system level, we need to compute closed loop expressions of each of the gain configurations. That helps us predict the time domain behavior of the regulator without using any real circuit components to a first order approximation. The expressions that we have derived are all based on the assumption that the switches are ideal and have zero on resistance, R_{on}. Another assumption that has been made is that there is a constant load on the regulator.

4.1. Modelling the Gain Configurations

A typical time domain output of any given gain configuration is shown in Fig. 4.2. The *gain* phase is referred to as ϕ_1 and the *common* phase is called ϕ_2. There are four voltages that are of importance to us. V_h and V_m are the output voltage at the beginning and end of ϕ_1. Similarly, V_{m1} and V_l are the values of the output voltage at the beginning and end of ϕ_2 respectively.

Since a constant load, I_{load} was assumed the values of V_h, V_m, V_{m1} and V_l repeat after every cycle in steady state. The transition from $\phi 1$ to $\phi 2$ and viceversa have abrupt changes due to the change from the *gain* phase to *common* phase. In reality these will not be abrupt due to the nonzero switch resistance.

We can express V_h in terms of V_l as shown in Eq. 4.1. Similarly we can express V_{m1} in terms of V_m as shown in Eq. 4.2. The output voltage V_m is sampled at the end of $\phi 2$.

$$V_h = \frac{V_l(C_{hold} + C) + V_{in}C}{3 * C + C_{hold}} \tag{4.1}$$

where $C = C_{ext1,2,3}$, as all the three capacitors are equal in size.

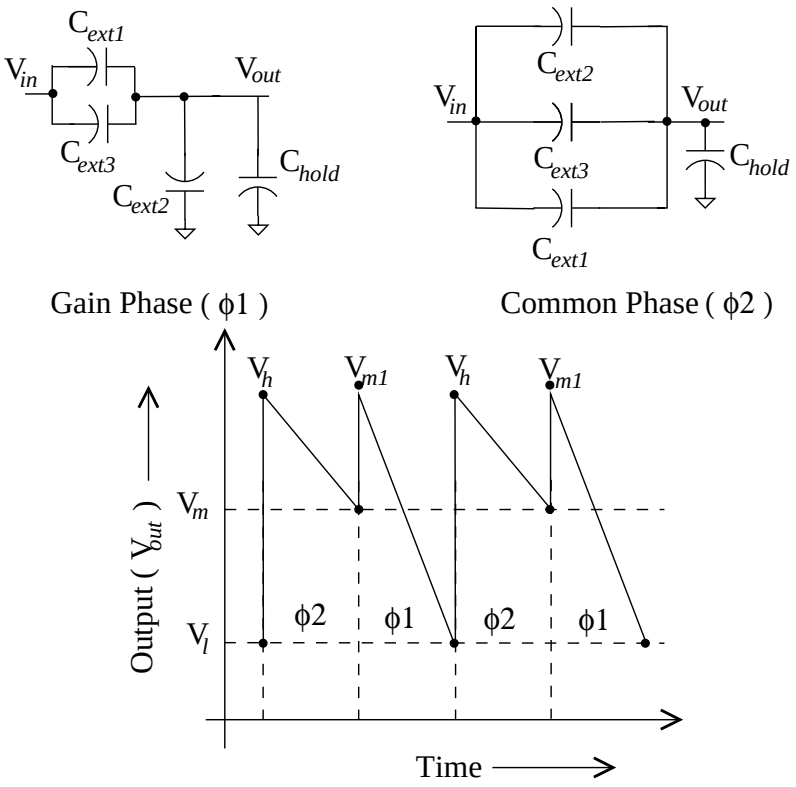

Figure 4.1. Theoretical time domain response of a gain configuration.

Since I_{load} is constant and is present during both phases we can write Eqs. 4.3 and 4.4

$$V_{m1} = \frac{V_m(C_{hold} + C) + V_{in}C}{3 * C + C_{hold}} \tag{4.2}$$

$$V_{m1} - V_l = \frac{I_{load}}{2f(3C + C_{hold})} \tag{4.3}$$

$$V_h - V_m = \frac{I_{load}}{2f(3C + C_{hold})} \tag{4.4}$$

where f is the frequency of operation.

From the above equations we can find the output voltage, V_h, in terms of the input voltage and is given in Eq. 4.5. We see that given V_{in} and all the circuit parameters we can calculate V_h. This can now be substituted in Eqs. 4.2-4.4 to calculate the value of V_m, V_{m1} and V_l. These four points are sufficient to describe the state of the system at any given time. We see from in Eq. 4.5 that if I_{load} is zero (ideal condition), the output voltage is $V_{in}/2$ as expected.

$$V_h = \frac{V_i}{2} - \frac{I_{load}(C_{hold} + C)}{8fC(2C + C_{hold})}\left[1 + \frac{C_{hold} + C}{3C + C_{hold}}\right] \tag{4.5}$$

The time domain behavior of the gain configurations 1/2 and 2 is shown in Fig. 4.2. These were plotted using the closed form equations given above. The input voltage was 1.5V, C was 0.33μF and C_{hold} was 10μF. The load was assumed to be 100mA. The frequency of operation is 1MHz.

Using the above equations, each of the gain configurations was simulated in MATLAB and compared with simulations in SPICE. They were found to be in close agreement. The expressions for different gain configurations are listed in Table 4.1.

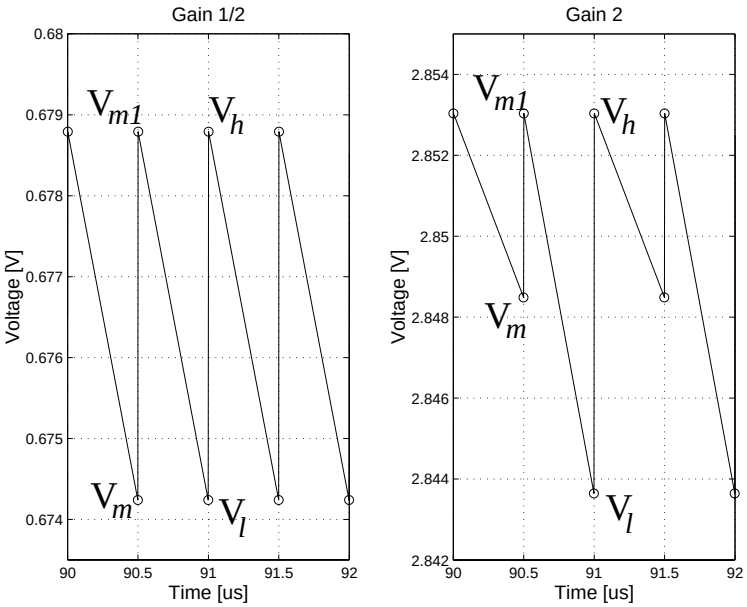

Figure 4.2. Simulated time domain response of gain configurations 1/2 and 2.

Gain configuration	Output Voltage (Vh)
1/2	$\frac{V_i}{2} - \frac{I_{load}(C_{hold}+C)}{8fC(2C+C_{hold})}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right]$
2/3	$\frac{2V_i}{3} - \frac{I_{load}C_{hold}}{9fC(C+C_{hold})}\left[1+\frac{C_{hold}}{3C+C_{hold}}\right]$
3/4	$\frac{3V_i}{4} - \frac{3I_{load}(C_{hold}-C)}{32fCC_{hold}}\left[1+\frac{C_{hold}-C}{3C+C_{hold}}\right]$
1	$\frac{V_i}{1} - \frac{I_{load}(C_{hold}+C)}{4fC(3C+C_{hold})}$
4/3	$\frac{4V_i}{3} - \frac{I_{load}}{6fC}\left[1+\frac{C_{hold}}{3C+C_{hold}}\right]$
3/2	$\frac{3V_i}{2} - \frac{I_{load}}{4fC}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right]$
2	$\frac{2V_i}{1} - \frac{I_{load}}{4fC}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right]$

Table 4.1. Expressions of Output Voltage for different gain configurations.

4.2. Modelling Efficiency of the Gain Configurations

The efficiency of the charge pump can be computed by Eq. 4.6. The power dissipated at the output, P_{out}, can be easily computed as we know V_{out} and I_{load}. To calculate the power supplied by the input, P_{in}, we need to compute the average current that is delivered by the input in each of the gain configurations.

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{in}} \\ &= \frac{V_{out} \cdot I_{load}}{V_{in} \cdot I_{in}} \end{aligned} \tag{4.6}$$

To compute the average current supplied by the input, I_{in}, we find the amount of charge transferred from V_{in} to C_{ext1}, C_{ext2} and C_{ext3} in every cycle. This can be used to calculate the current provided by the input in every cycle. The average current is calculated by averaging the current per cycle for a large number of clock cycles. Since we know the value of V_{out} at the beginning and end of every clock phase (Eqs. 4.12-4.15) we can compute the amount of charge transferred by Eq. 4.7.

$$\delta q = C_{eff} * \delta V_{in} \tag{4.7}$$

The output voltage makes four transitions in a given clock period ($\phi 1$ and $\phi 2$) as seen in Fig. 4.2. The amount of charge transferred from the input when the output makes a transition from V_h to V_m is given by q_{h-m} and is given by Eq. 4.8. Similarly the charge transfer when V_{out} transitions from V_m to V_{m1} is q_{m-m1} and is given by Eq. 4.9.

$$q_{h-m} = 3C(V_h - V_m) \tag{4.8}$$

$$q_{m-m1} = 2C(V_m - V_{m1}) \tag{4.9}$$

The C_{eff} for Eq. 4.8 is 3C because the input sees three capacitors in parallel and in Eq. 4.9 the effective capacitance is 2C because the input sees two capacitors in parallel. The charge delivered for the other two transitions are given in Eqs. 4.10 and 4.11. The effective capacitance is 2C and C_{hold} respectively.

$$q_{m1-l} = 2C(V_{m1} - V_l) \tag{4.10}$$

$$q_{l-h} = C_{hold}(V_h - V_l) \tag{4.11}$$

By adding Eqs. 4.8-4.11 we get the total charge transferred per clock cycle and hence the average current. These computations do not take into account the non-zero switch resistance and power dissipation in the other regulator circuits.

4.3. Modelling the Charge Pump

We can rewrite Eqs. 4.1-4.4 for a gain of 1/2 as shown in Eqs. 4.12-4.15,

$$V_m(n) = V_h(n) - \frac{I_{load}}{2f(3C + C_{hold})} \tag{4.12}$$

$$V_h(n) = \frac{V_l(n)(C_{hold} + C) + V_{in}(n)C}{3 * C + C_{hold}} \tag{4.13}$$

$$V_l(n) = V_{m1}(n) - \frac{I_{load}}{2f(3C + C_{hold})} \tag{4.14}$$

$$V_{m1}(n) = \frac{V_m(n-1)(C_{hold} + C) + V_{in}(n)C}{3 * C + C_{hold}} \tag{4.15}$$

where V_m(n) corresponds to the n-th sample.

Solving these equations we can compute V_m(n) in terms of V_m(n − 1) as shown in Eq. 4.16

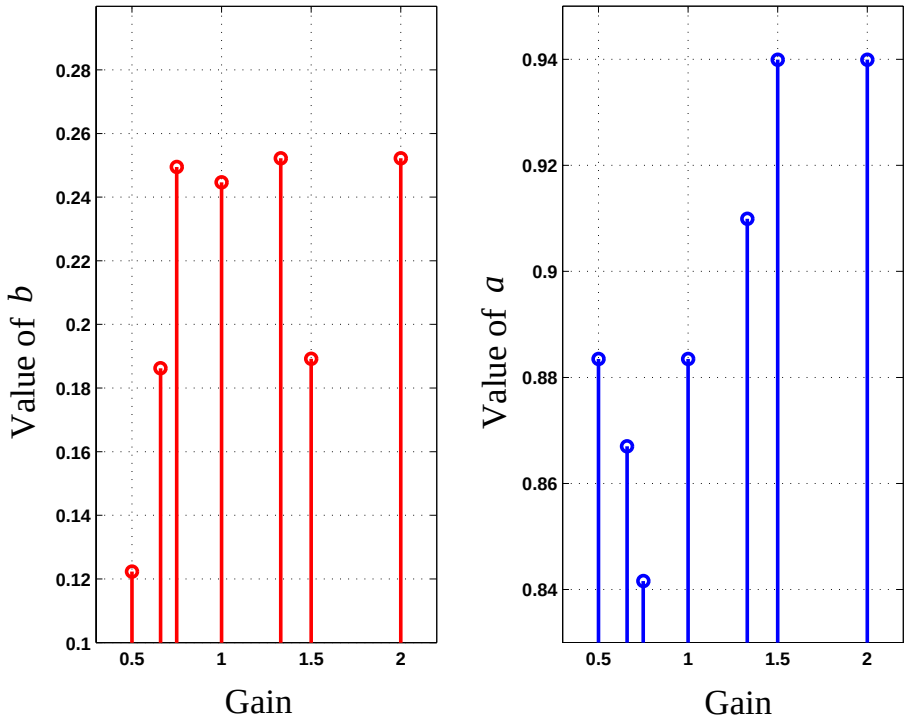

Figure 4.3. Variation of a and b with gain for zero load condition.

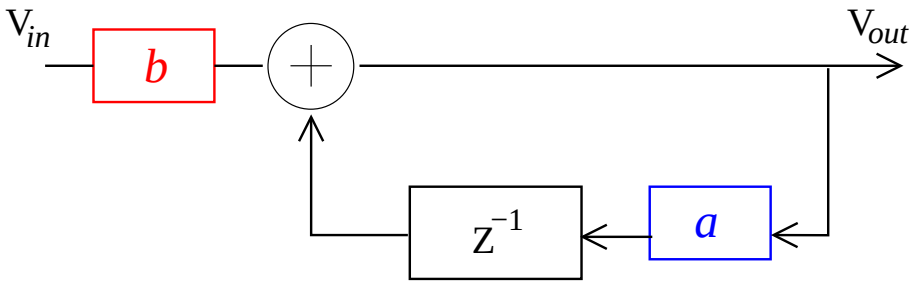

Figure 4.4. Charge pump modelled as a lossy integrator.

Gain configuration	a	b
1/2	$\frac{(C_{hold}+C)^2}{(C_{hold}+3C)^2}$	$\frac{C}{(C_{hold}+3C)}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right]$
2/3	$\frac{2C_{hold}^2}{(C_{hold}+3C)(2C_{hold}+3C)}$	$\frac{2C}{(C_{hold}+3C)}\left[1+\frac{C_{hold}}{3C+2C_{hold}}\right]$
3/4	$\frac{3(C_{hold}-C)^2}{(C_{hold}+3C)(3C_{hold}+C)}$	$\frac{3C}{(C_{hold}+3C)}\left[1+\frac{C_{hold}-C}{C+3C_{hold}}\right]$
1	$\frac{(C_{hold}+C)^2}{(C_{hold}+3C)^2}$	$\frac{2C}{(C_{hold}+3C)}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right]$
4/3	$\frac{C_{hold}}{3C+C_{hold}}$	$\frac{4C}{3C+C_{hold}}$
3/2	$\frac{C_{hold}+C}{3C+C_{hold}}$	$\frac{3C}{3C+C_{hold}}$
2	$\frac{C_{hold}+C}{3C+C_{hold}}$	$\frac{4C}{3C+C_{hold}}$

Table 4.2. Expressions of a and b for different gain configurations.

$$V_m(n) = \frac{V_m(n-1)(C+C_{hold})^2}{(3C+C_{hold})^2} + \frac{V_{in}(n)C}{(3C+C_{hold})}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right] \tag{4.16}$$

This can also be written as:

$$V_m(n) = aV_m(n-1) + bV_{in}(n) \tag{4.17}$$

where a= $\frac{(C+C_{hold})^2}{(3C+C_{hold})^2}$ and b = $\frac{C}{(3C+C_{hold})}\left[1+\frac{C_{hold}+C}{3C+C_{hold}}\right]$ for a given input voltage.

This suggests that the charge pump can be modelled as a lossy integrator with a loss factor a and constant gain b as shown in Fig. 4.4. The values of a and b change for different gain settings and are listed in Table 4.2.

The variation of a and b with gain is plotted in Fig. 4.3. The output given by this proposed model has been verified against spice simulations of the individual gain configurations. It should be mentioned that this model represents the charge pump in a single gain setting and does not model the dynamic variation between the different gain settings.

The key idea of the model is to be able to simulate the regulator on a system level to a first order approximation and compute the time domain response, frequency response and efficiency without any circuit level simulations.

5. DELTA-SIGMA CONTROL LOOP

5.1. The Delta-Sigma Concept

The class of analog to digital converters that use oversampling of the input signal and noise shaping of the quantization error to achieve higher resolution are called delta-sigma ($\Delta\Sigma$) converters. Oversampling implies that the input signal is captured at a higher rate then the nyquist rate. A common parameter used for $\Delta\Sigma$ converters is the oversampling ratio (OSR), defined as:

$$OSR = \frac{f_s}{f_{nyq}} \tag{5.1}$$

where f_s is the sampling frequency and f_{nyq} is the nyquist frequency, defined as a frequency twice the highest frequency component of the input. By oversampling the input signal, the quantization error which is an artifact of the conversion from analog to digital, is spread over a larger range of frequencies.

The other property which is common to $\Delta\Sigma$ converters is noise-shaping. Fig. 5.1 illustrates a linearized z-domain model of a first order $\Delta\Sigma$ modulator. The model assumes that the quantization error can be modelled as additive white noise, with properties that it is independent of the input, uniformly distributed in $[-\Delta/2, \Delta/2]$ where Δ is the step size of the quantizer, and has a white power spectral density. Thus, this quantization error, $e[n]$ can be represented as an additional input to the system. The digital output from the A/D is then fed to a digital to analog converter (D/A) and subtracted from the input.

The output of the modulator $Y(z)$ can be expressed as

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{5.2}$$

where STF(z) is the signal transfer function and NTF(z) is the noise transfer function. Solving Eq. 5.2 for STF(z) and NTF(z), and expressing them in terms of H(z) yields

$$STF(z) = \frac{Y(z)}{U(z)}\bigg|_{E(z)\equiv 0} = \frac{H(z)}{1+H(z)} \tag{5.3}$$

$$NTF(z) = \frac{Y(z)}{E(z)}\bigg|_{E(z)\equiv 0} = \frac{1}{1+H(z)} \tag{5.4}$$

Equation 5.4 illustrates that if H(z) is a lowpass function, the quantization noise is shaped by a high-pass type function. This indicates that most of the quantization noise can be pushed to higher frequencies.

This property of the delta sigma loop is utilized to solve the drawbacks of the LM3352 shown in chapter 2.

5.2. Proposed Delta-Sigma Control Loop

The block diagram of the regulator with the proposed $\Delta\Sigma$ control loop is shown in Fig. 5.2. Comparing this to Fig. 2.3 we see the $\Delta\Sigma$ control loop is a part of the *gain hopping* and *PWM* loop and it replaces the comparator and the *U/D counter* from the LM3352. The $\Delta\Sigma$ block provides a 3-bit word and the *skip* signal required for the gain hopping and *PWM* operation.

As shown in Fig. 5.3, the $\Delta\Sigma$ loop comprises of an integrator, an A/D and a D/A. The error between the desired voltage and the output voltage is integrated and is fed into the 4-bit A/D. As V_{out} approaches $V_{desired}$, the error signal decreases, reducing the input to the A/D. This causes a smaller gain to be chosen until we are forced to use the minimum gain. The 3 most significant bits (MSB's) are used to define the gain of the regulator. Since there are 7 possible gain settings 3 bits are

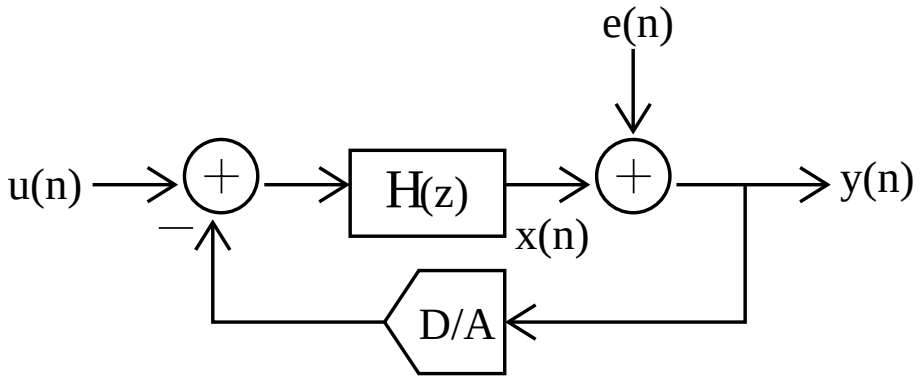

Figure 5.1. Linear model of a ΔΣ modulator.

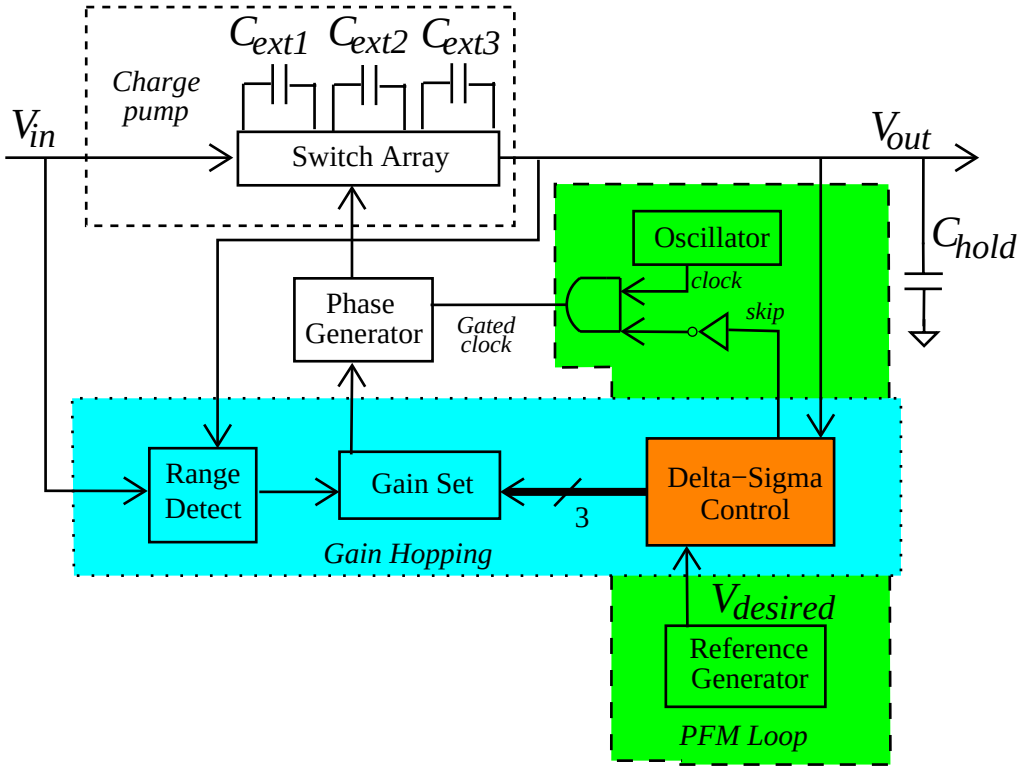

Figure 5.2. Block diagram of LM3352 with the ΔΣ control loop.

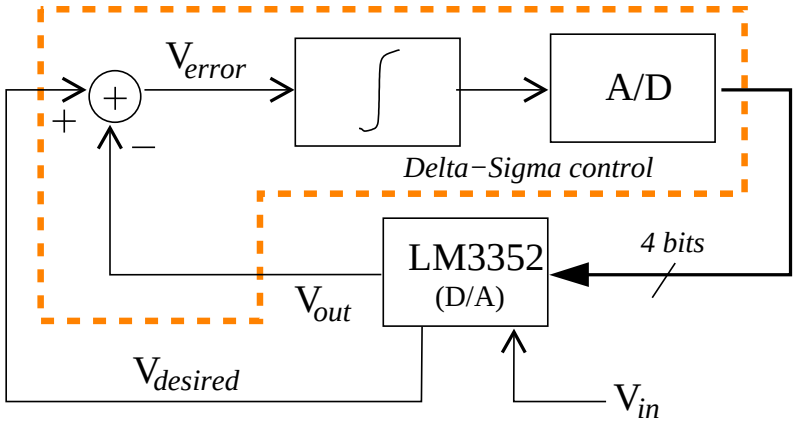

Figure 5.3. Components of the $\Delta\Sigma$ control loop.

sufficient to cover all possible gain settings. The least significant bit (LSB) is used as the *skip* signal to switch the *charge pump* ON and OFF. The LM3352 is used as the D/A in the $\Delta\Sigma$ control loop. The output from the LM3352 is the regulated voltage.

5.3. Discrete-Time Model of Delta-Sigma Control Loop

Figure 5.4 depicts the discrete-time model of the $\Delta\Sigma$ control loop with the regulator. The equivalent model of the charge pump derived in the previous chapter is used. The A/D is represented as a additive white noise source with a quantization noise of q. The hold capacitor on the output of the regulator introduces a pole in the system and there is also additional analog delay through the loop. These factors make the loop less stable. So in order to stabilize the loop a feed-forward path was added around the integrator. The gain of this feed-forward path is K.

The NTF for the system shown in Fig. 5.4 is given in Eq. 5.5 . This however is for a specific value of input, output and load voltage and assumes that the system is settled. This does not represent the dynamic nature of the system but gives us a good estimate of how the system behaves. This is because the values of a and b depend on the state of the system and change dynamically.

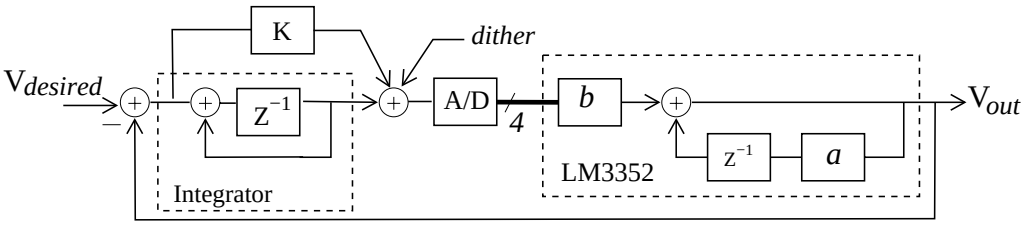

Figure 5.4. Discrete-time model of the regulator with the delta-sigma control loop.

$$NTF = \frac{V_{out}}{q} = \frac{b(1-z^{-1})}{1 - z^{-1}[1 + a - (K+1)b] + z^{-2}(a - Kb)} \tag{5.5}$$

Since the $\Delta\Sigma$ is a first-order loop it is prone to idle tones [2] . This is overcome by using a dither signal. The dither signal is a additive pseudo-random white noise with a value lower then 1/2LSB. Here LSB signifies the least significant bit of the quantizer in the $\Delta\Sigma$ loop. The quantizer is 4-bit, so the LSB is $V_{in}/2^4$. The dither signal is not shown in Fig. 5.4 but it is added along with q.

The NTF has been plotted in Figure 5.5. Also shown is the variation in the NTF with the increase in the feedforward gain K. We see that as the feedforward increases the pole Q reduces and this in turn makes the system more stable. In the time domain this would correspond to a lower ripple. This can intuitively be explained as the feedforward path actually lowers the effect of the delay through the

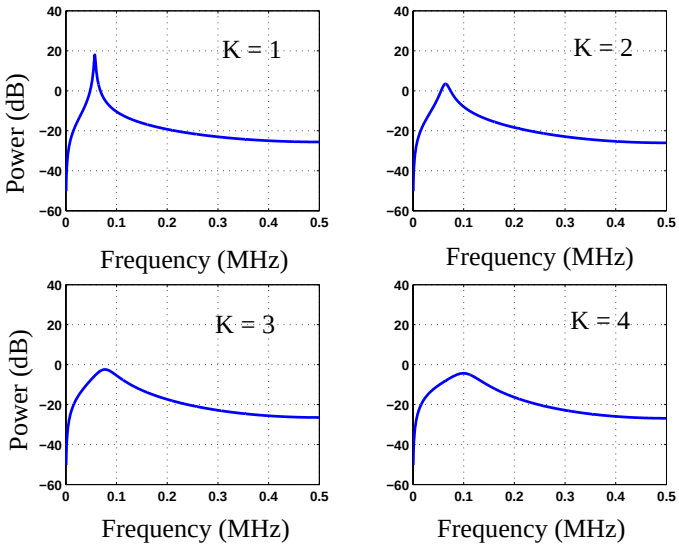

Figure 5.5. Variation of the NTF with feed-forward factor K.

integrator. It was seen from simulations that a value of K greater than 4 does not benefit stability. This is because the increase in the feed-forward reduces the effect of the integrator in the loop. From Figure 5.5 we see that the system has a zero at 500kHz which is $F_s/2$.

The time domain output and spectrum of the regulator with and without the $\Delta\Sigma$ loop are compared in Figure 5.6. Both the regulators were simulated using the closed-form equations derived in chapter 5. For the simulation V_{in} was 5.2V, $V_{desired}$ was 3.6V, I_{load} was 150mA, C_{hold} was 30uF and $C_{ext1,2,3}$ was 0.33uF. We see the the ripple in the case of the $\Delta\Sigma$ implementation is higher then that of the LM3352. This can be attributed to increased delay through the control loop. The $\Delta\Sigma$ control loop spreads the tones and thus has a smoother spectrum. We also see that the $\Delta\Sigma$ loop makes the duty-cycle of the output voltage more random thus spreading the tones.

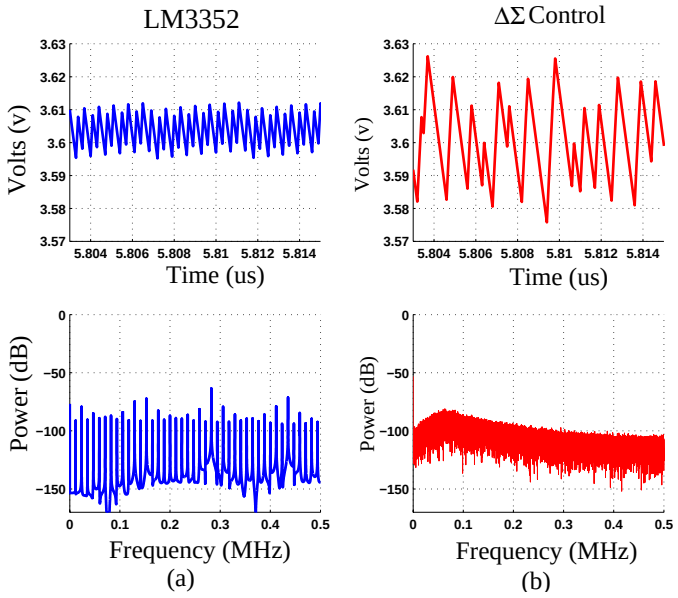

Figure 5.6. Time-domain and spectrum plots of LM3352 and ΔΣ control loop for $V_{desired} = 3.6$V.

Figure 5.7 shows the two regulators for $V_{desired} = 4.9$V all other factors remaining constant.

The efficiency plots for both the architectures are shown in Figure 5.8. These have been computed using Eq. 4.6. We see that both the architectures have similar efficiencies. The dotted line is the efficiency of the LM3352 and the solid line is the plot of efficiency with the ΔΣ control. The conditions for the particular simulation are similar to those mentioned above. The input voltage is swept from 2.5V to 5V.

Thus by the use of a ΔΣ control loop the drawbacks of LM3352 can be circumvented. This however comes at the cost of increased ripple.

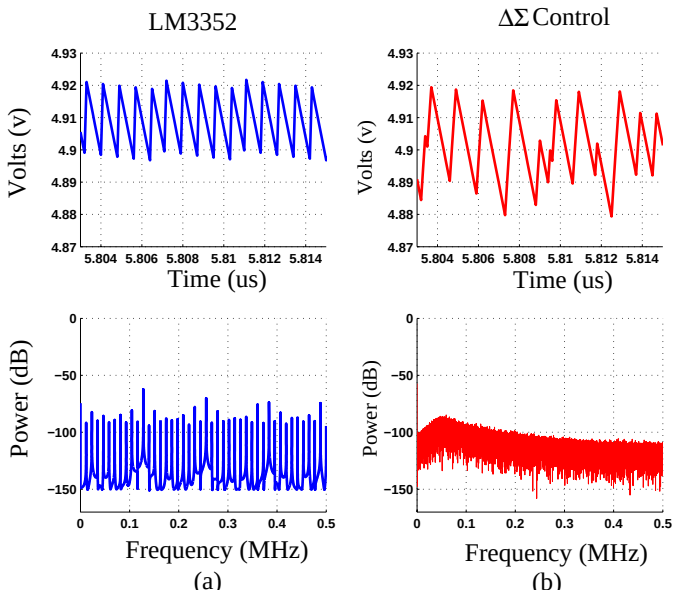

Figure 5.7. Time-domain and spectrum plots of LM3352 and ΔΣ control loop for $V_{desired} = 4.9$V.

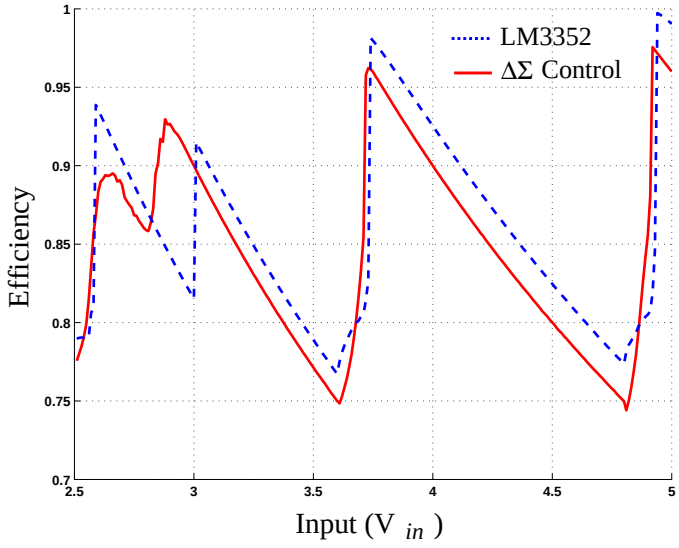

Figure 5.8. Efficiency plots of LM3352 and ΔΣ control loop.

6. IMPLEMENTATION AND CIRCUIT DESIGN

To realize the $\Delta\Sigma$ proposed in the previous chapter and shown in Figure 5.3, five basic building blocks are needed (as illustrated in Figure 6.1):

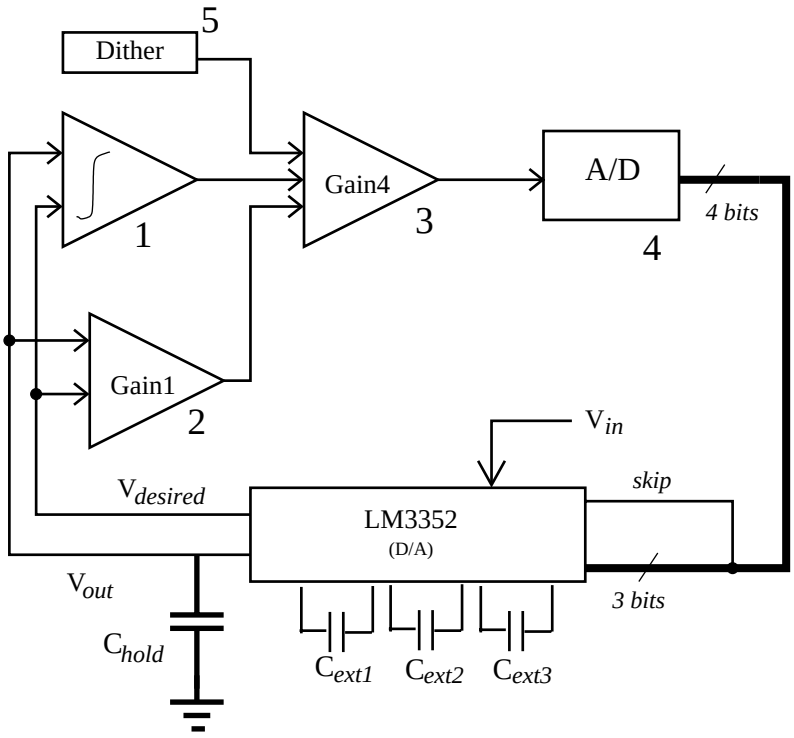

Figure 6.1. Generic circuit schematic of $\Delta\Sigma$ control loop with LM3352 indicating the 5 basic building blocks.

- **Integrator**

  To compute the difference between $V_{desired}$ and V_{out} and integrate this error voltage.

- **Gain 1**

  To provide the required feed-forward path for V_{error}.

- **Gain4**

  To add the output of the integrator, gain1 and the dither cell.

- **Analog to digital converter (A/D)**

  To provide the 4-bit word to the LM3352.

- **Dither**

  To generate a pseudo-random white noise of amplitude less them $\pm 1/2V_{LSB}$.

The $\Delta\Sigma$ loop provides gain control and does not come directly in the signal path. This allows us to use single ended circuitry and keep the circuits simple. Since the battery voltage is the positive supply for all the analog blocks, they should be designed to operate at a voltage as low as 2.5V.

6.1. Integrator

The purpose of the integrator is to integrate the difference between V_{in} and $V_{desired}$. The integrator is realized using the classical parasitic-insensitive switched-capacitor integrator [3] shown in Figure 6.2. Capacitors C_1 and C_2 dump charge equivalent to the difference between $V_{desired}$ and V_{in} into C_f. The common-mode voltage of V_{in} and $V_{desired}$ is different from that of the operational amplifier (opamp). This requires that we implement a level shift in the integrator to ensure that the output of the integrator is referred to the common mode voltage V_{cm}, of the opamp. This is accomplished by charging C_1 with respect to ground but discharging it with respect to V_{cm}. The same can be done for C_2.

In addition to the level shift we need to provide a gain of 2 to $V_{desired}$. This is because $V_{desired}$ is provided by a bandgap and is actually half the required value. In other words the regulator can be programmed to give a output in the range of 1.8V to 5.5V but the actual range of $V_{desired}$ is only 0.9V to 2.75V. Hence C_1 is twice the size of C_2 and C_f. Advanced cut off is used to minimize charge injection. The transfer function of the integrator, considering an ideal opamp and zero input offset voltage, is given by Eq. 6.1. This assumes that both $V_{desired}$ and V_{in} change at the beginning of $\phi 2$.

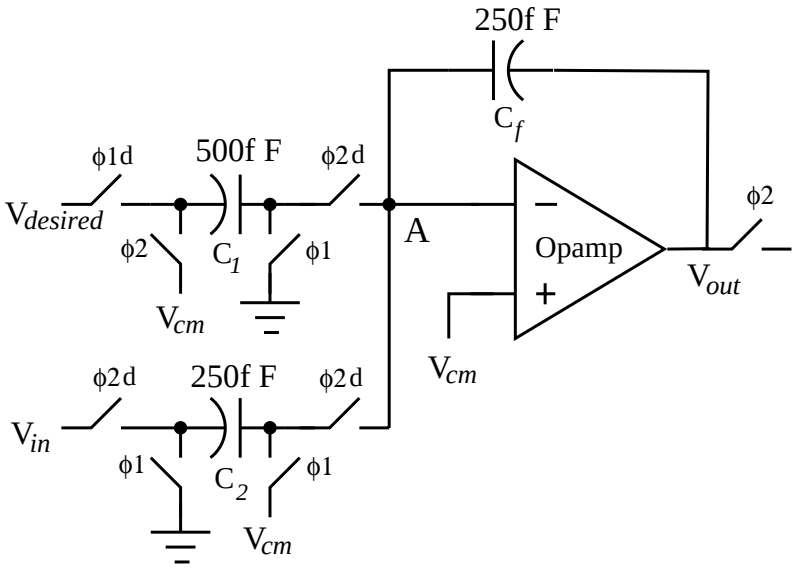

Figure 6.2. Schematic of the integrator.

$$V_{out}(z) = \frac{C_1}{C_f}\frac{z^{-\frac{1}{2}}}{1-z^{-1}}V_{desired}(z) - \frac{C_2}{C_f}\frac{1}{1-z^{-1}}V_{in}(z) \tag{6.1}$$

6.1.1. Operational Amplifier

A standard two stage miller compensated opamp was implemented. The schematic is shown in Figure 6.3. The characteristic of the opamp are listed in Table 6.1. The input transistors have long channel lengths to reduce mismatch. The total power dissipation in the opamp is 400μW at a supply voltage of 5.5V.

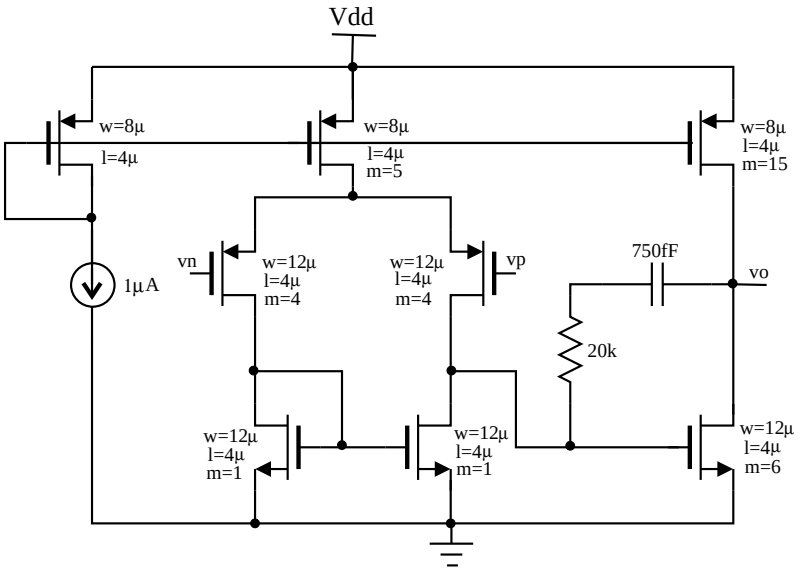

Figure 6.3. Schematic of the opamp.

6.1.2. Common-Mode Voltage Generator

Since the switched-capacitor circuits used are single ended the opamp needs a common-mode voltage. This is generated using the circuit shown in Figure 6.4.

	Typical.	*Slow*	*Fast*
DC Gain	77	76	76
Unity Gain Frequency	12.2	15	9
Phase Margin	66	62	65

Table 6.1. Opamp specifications over process corners.

The output from the bandgap (V_{bg}) is passed through a PMOS and a NMOS soure follower to provide the common-mode voltage (V_{cm}). The total power dissipation in this cell is 880μW at a supply voltage of 5.5V.

6.2. Gain1 Block

This block provides the required feedforward path in the $\Delta\Sigma$ loop. The schematic of the block is shown in Figure 6.5. The capacitors C_1 and C_2 dump charge corresponding to the difference of $V_{desired}$ and V_{out} into C_f. Capacitor C_f, however, is discharged every alternate clock cycle. The opamp used is the same as shown in Figure 6.3. The transfer function for the block is given by Eq. 6.2 if the opamp is considered ideal and the offset voltage is considered to be zero. We have assumed that both V_{in} and $V_{desired}$ change at beginning of $\phi 2$.

$$V_{out}(z) = \frac{C_1}{C_f} z^{-\frac{1}{2}} V_{desired}(z) - \frac{C_2}{C_f} V_{in}(z) \tag{6.2}$$

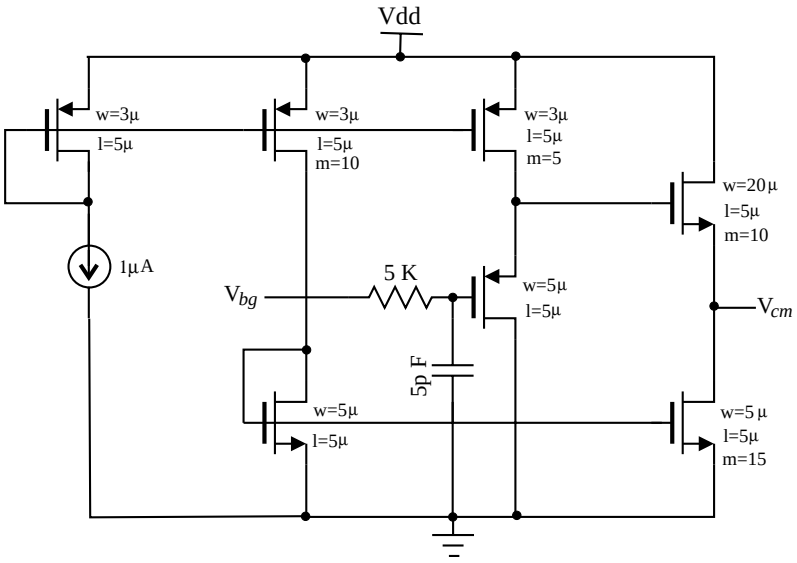

Figure 6.4. Schematic to generate common-mode voltage (V_{cm}) for switched-capacitor blocks.

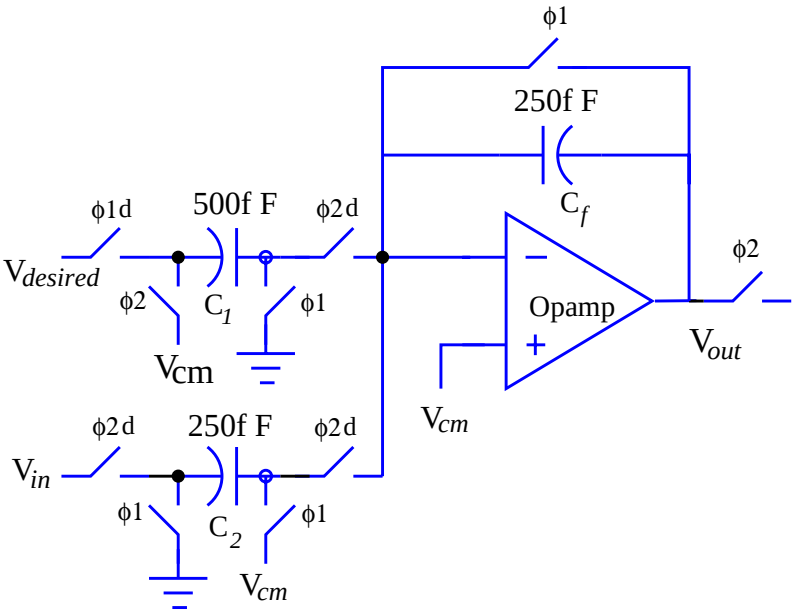

Figure 6.5. Schematic of gain1 block.

6.3. Gain4 Block

This block acts as a summing node for the signal from the integrator, gain1 and the dither generation block. In addition this provides a gain of 4 for V_{gain1} (the output of gain1 block) and an attenuation of 32 for V_{dither} (the output of the dither generator block). This is accomplished by appropriately sizing the capacitors C_1 and C_3 with respect to C_f as shown in Figure 6.6. The ideal transfer function of this block is given by Eq. 6.3. The opamp used in the schematic below is shown in Figure 6.3.

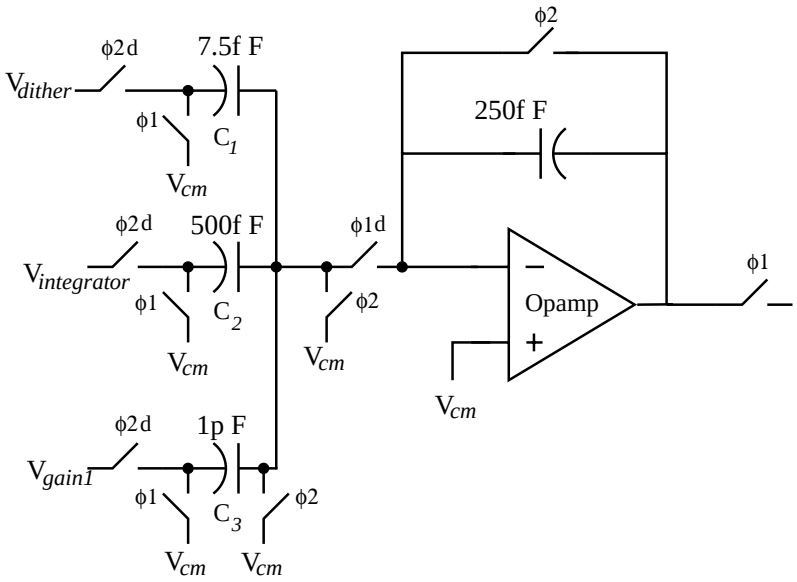

Figure 6.6. Schematic of the gain4 block.

$$V_{out}(z) = \frac{C_1}{C_f} z^{-\frac{1}{2}} V_{dither}(z) + \frac{C_2}{C_f} z^{-\frac{1}{2}} V_{integrator}(z) + \frac{C_3}{C_f} z^{-\frac{1}{2}} V_{gain1}(z) \qquad (6.3)$$

6.4. Analog-Digital Converter

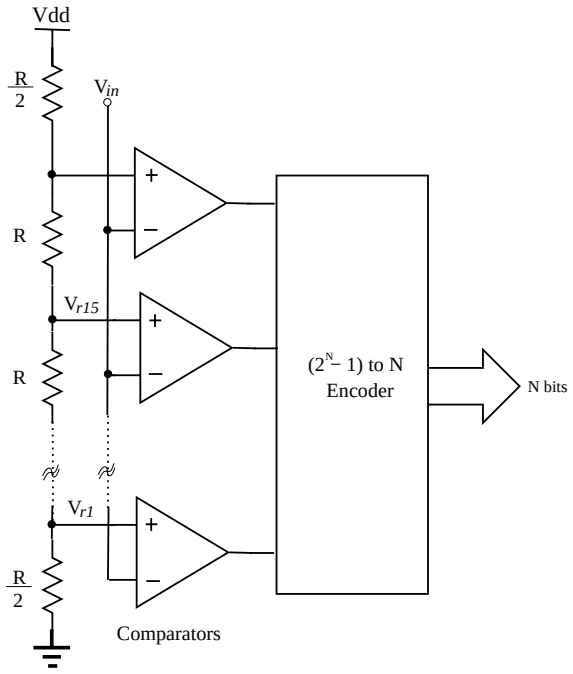

Figure 6.7. Block diagram of the a/d converter used.

The A/D converter is required to generate a 4 bit word every clock cycle. This can be accomplished by using either an flash or an interpolative type architecture. For the present implementation a 4-bit flash [4] was considered. The block diagram of the architecture is shown in Figure 6.7. Since we need 4 bits there are 15 comparators and 15 reference levels. The resistive ladder generates the required reference levels. The total resistance of the resistive ladder is 400KΩ. This means a static current of 12μA will flow through it at a supply voltage of 5.5V. Any comparator connected to a resistor string node where V_{ri} is larger than V_{in} will have a 1 output while those connected to nodes with V_{ri} less than V_{in} will have 0 output. Such an output code is

referred to as the thermometer code. The thermometer code is encoded to provide a 4 bit word.

6.4.1. Comparator

Since we need 15 comparators, a simple clocked comparator [4] shown in Figure 6.8 was used. This uses a clocked inverter as a comparator. When $\phi 1$ is high, the inverter is set to its bistable operating point, where its input voltage equals its output voltage. The inverter is biased with a constant current source, to limit the amount of current through it during the reset phase. The inverter operates as a single stage opamp with only one pole so the stability is guaranteed. In the same phase the bottom plate of capacitor C is charged to V_{ri}. In $\phi 2$ the inverter is free to fall either low or high depending on its input voltage. At the same time, the bottom plate of C is pulled to the input voltage, V_{in}. Since the top plate of the capacitor is floating, C must keep its charge, and therefore the inverter's input will change by the voltage difference between V_{ri} and V_{in}. Since the inverter's input was at its bistable point, the difference between V_{ri} and V_{in} will determine which direction the inverter's output will fall.

6.4.2. Encoder and Dither Generation

As mentioned earlier the thermometer code from the comparators has to be encoded into a 4 bit code. The thermometer code should have a single transition. However, sometimes a lone 1 will occur within the string of 0s (or 0 within a string

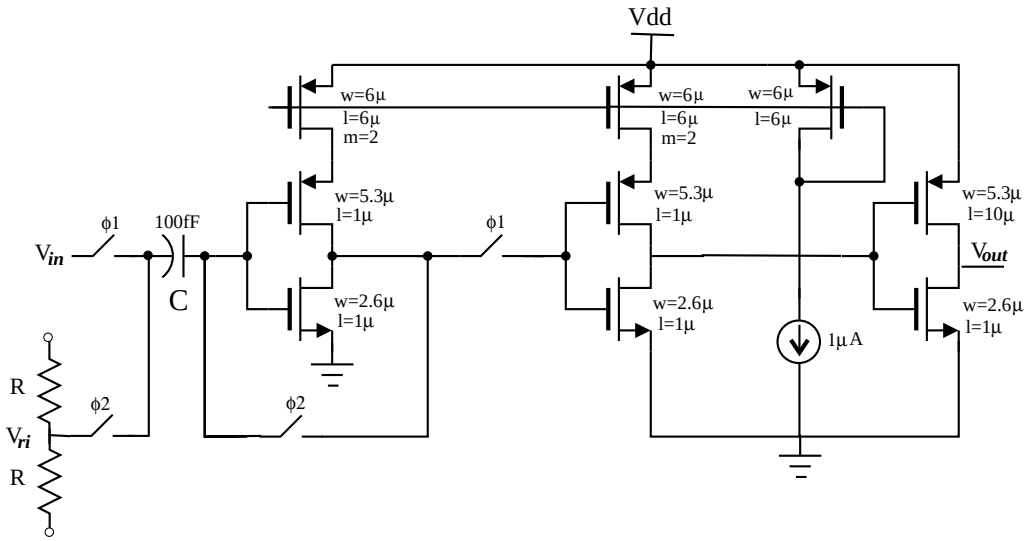

Figure 6.8. Schematic of the clocked comparator.

of 1s) due to comparator metastability, noise and cross talk. These bubbles occur near the transition points of the thermometer code and can be removed by using three input NAND gates [5]. There must now be two 1s immediately above a 0 in determining the transition point in the thermometer code. However, this circuit will not eliminate the problem of a stray 0 being two places away from the transition point. Once the bubble error has been removed the code is encoded using a standard 15 bit to 4 bit encoder.

A maximal-length feedback shift register is used to generate the pesudo-random dither signal. This comprises of a series of 7 flip-flops with XOR gates in the feedback [6].

7. EXPERIMENTAL RESULTS

A test chip was fabricated in a $0.72\mu m$ CMOS process through National semiconductor corporation. The die photograph of the test chip is shown in Fig. 7.2. The different regions are marked on the figure. The chip was tested through the input range of 3V to 5V for several loads and output voltages. A typical measured output ripple and spectrum for a load of 50mA and 150mA, output voltage of 3.2V and input voltage of 3.7V is shown in figures 7.1 and 7.3.

The ripple of LM3352 is periodic, while the delta-sigma control causes a more random ripple and hence a smoother spectrum. The tones in LM3352 reduce as the load increases. The efficiencies of the LM3352 and the $\Delta\Sigma$ control for an output voltage of 3.2V and load of 50mA and 150mA have been plotted in Fig. 7.4. We see that they are comparably efficient.

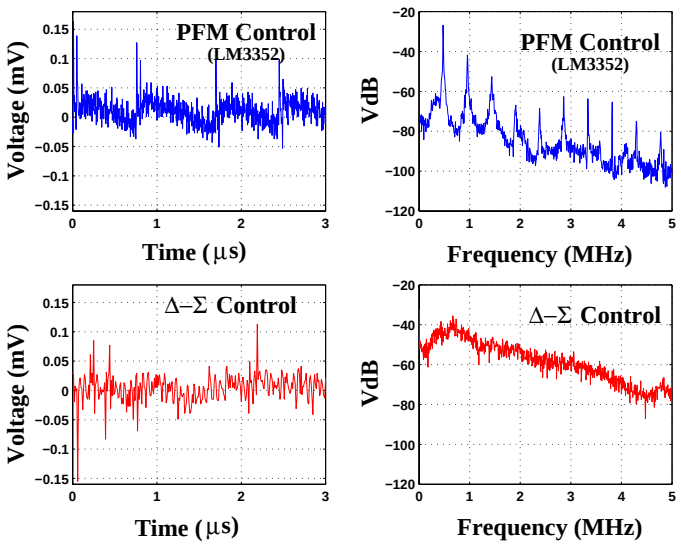

Figure 7.1. Measured output ripple and frequency spectrum of LM3352 and $\Delta\Sigma$ control loop for I_{load}=50mA, V_{out}=3.2V and V_{in}=3.7V.

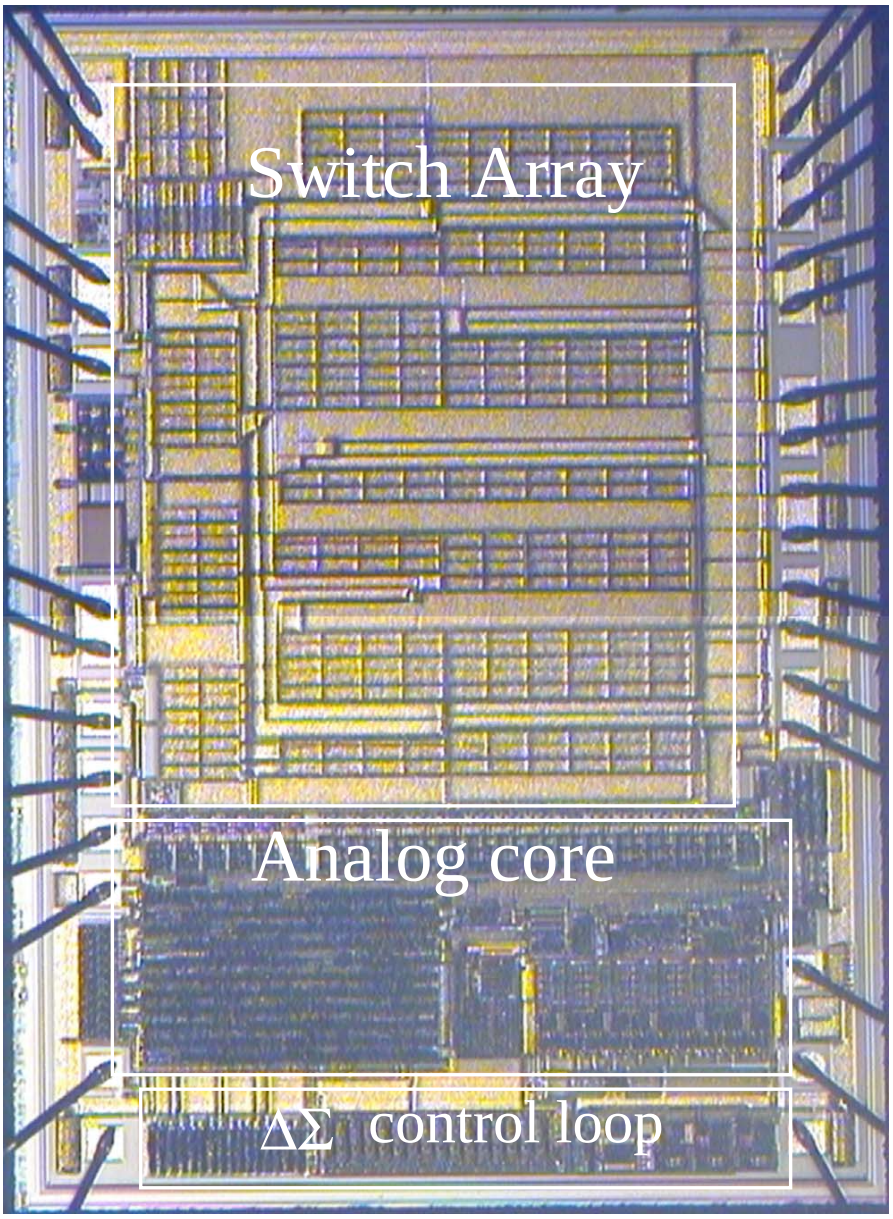

Figure 7.2. Die photograph of regulator with $\Delta\Sigma$ control loop.

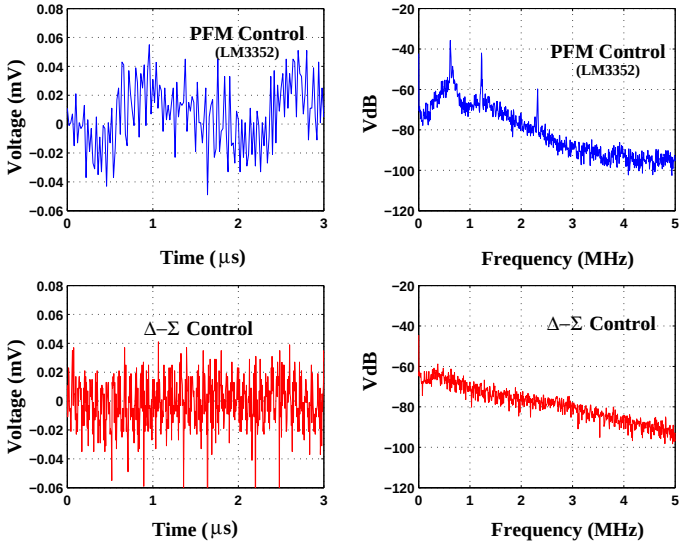

Figure 7.3. Measured output ripple and frequency spectrum of LM3352 and ΔΣ control loop for I_{load}=150mA, V_{out}=3.2V and V_{in}=3.7V.

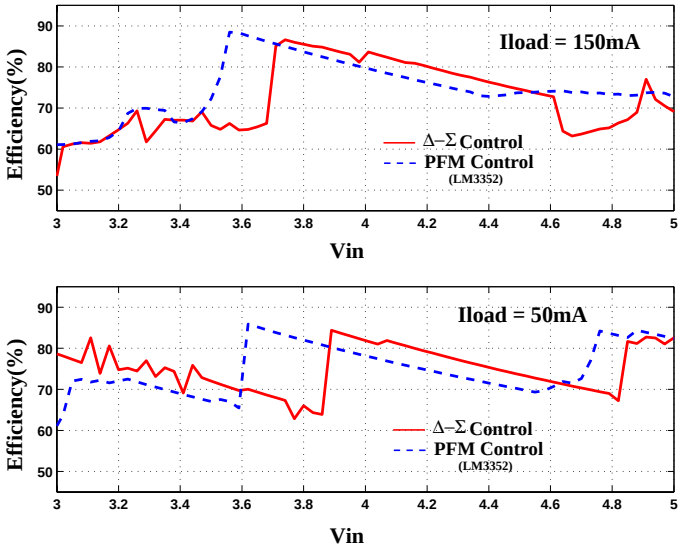

Figure 7.4. Efficiency plots of LM3352 and ΔΣ control loop for I_{load}=50mA and I_{load}=150mA and V_{out}=3.2V.

8. CONCLUSION

This thesis presents a $\Delta\Sigma$ control loop for PFM controlled voltage regulators. The test results indicate that the suppressions of tones in existing PFM architectures is possible using the $\Delta\Sigma$ control loop. A suppression of up to 50dB was measured in the 0-500kHz range. The additional delay through the loop however increases the ripple and causes slightly poorer regulation.

The thesis also presents an alternate method to model and compute the efficiency of switched capacitor buck and boost configurations.

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