20-Stage Pipelined ADC with Radix-Based Calibration

by
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1. INTRODUCTION

The continuous effort to improve the performance of analog-to-digital converters (ADC) has led the development of several precision techniques for ADC's. The primary objective of those precision techniques is to alleviate the accuracy constraints such as capacitor mismatch, charge injection, finite op amp DC gain and comparator offset. In the early years, the error correcting techniques like the ratio-independent [1], reference refreshing [2], capacitor error-averaging [3], on-chip capacitor trimming [4] and analog calibration [5] were applied in the analog domain. The main drawback of these analog precision techniques is the complexity of circuit implementation. The digitally controlled self-calibration [6] and digital-domain calibration [7] techniques were introduced to eliminate the disadvantage of the analog precision techniques but developed for successive approximation and flash type ADC's, respectively.

Due to the simplicity and relative easiness to achieve high resolution and high speed, the 1-bit/stage pipelined architecture has been used and calibration techniques [8]-[12] and [14] have been developed for it recently. The digital self-calibration technique proposed in [8] compensates for errors mentioned above but the overall transfer characteristics of the ADC are dependent upon the actual residue gains of each stage. The technique presented in [9] resolves the dependability of inter-stages but the finite op amp DC gain is not compensated. While the technique introduced in [11] has an advantage of continuous calibration, it requires an extra stage. The calibration algorithm presented in [12] overcomes these limitations addressed above but applies only to a single-stage algorithmic ADC.

The radix-based calibration proposed in [14] extends the technique [12] to a multi-stage algorithmic or pipelined architecture. To show the concept of radix-based calibration, a two-stage algorithmic ADC is used in [14]. Because the two-stage algorithmic ADC has only two different radices, which are repeatedly used for calibration, this does not show the effect of a true multi-stage ADC in which the radix

for each stage differs from each other. The primary objective is to verify the capability of the radix-based calibration in a multi-stage ADC as which a 1-bit/stage pipelined ADC is used.

The thesis organization is as follows. Chapter 2 describes the general pipelined architecture and specifies in the 1-bit/stage pipelined ADC. The sources of errors in a 1-bit/stage pipelined ADC is also addressed in the chapter. Some of the calibration techniques mentioned above are revisited with details in Chapter 3. Chapter 4 presents the radix-calibration techniques as well as the necessity of sub-radix-2 system. Chapter 5 is devoted to the circuit implementation of the 20-stage pipelined ADC with radix-based calibration. The simulation results are given in Chapter 6. Finally, Chapter 7 provides conclusion for this thesis.

2. PIPELINED ARCHITECTURE

A brief description of a general pipelined ADC architecture is first presented in this chapter. A single-bit-per-stage pipelined ADC, for which the radix-based calibration is used, is next described in details. The error sources and their effects in a pipelined ADC conclude this chapter.

2.1. General Pipelined ADC

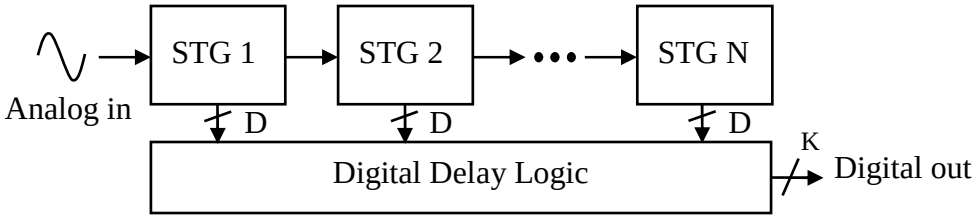


Figure 2.1. Block diagram of a typical pipelined ADC

Figure 2.1 shows a block diagram of a general N-stage pipelined ADC. Each stage consists of a multiplying digital-to-analog converter (MDAC) and a sub-ADC. An illustration on one stage is given in Figure 2.2. An external analog signal is sampled in the first stage. The sampled signal is then quantized by the sub-ADC yielding a D-bit digital output. The quantized signal is converted back to an analog signal in MDAC and subtracted from the original input signal, V_{IN}. The resulting quantity is multiplied by the amplifier gain 2^D to produce the residue voltage, $V_{RES,1}$, in full reference range for the next stage. $V_{RES,1}$ is sampled and processed in the similar manner on the next clock phase. Due to the concurrent stage residue processes and the successive sampling of the stage inputs, the corresponding digital outputs of each stage for a sampled input at a specific time are not aligned. In order to align the digital outputs in phase, an appropriate delay-logic is necessary. The digital delay logic exists to resolve the issue. The total number of bits is $K = N \cdot D$. The digital output of the pipelined ADC is

$$D_{OUT} = D_1 \cdot 2^{N-1} + D_2 \cdot 2^{N-2} + \cdots + D_{N-1} \cdot 2^1 + D_N . \qquad (2.1)$$

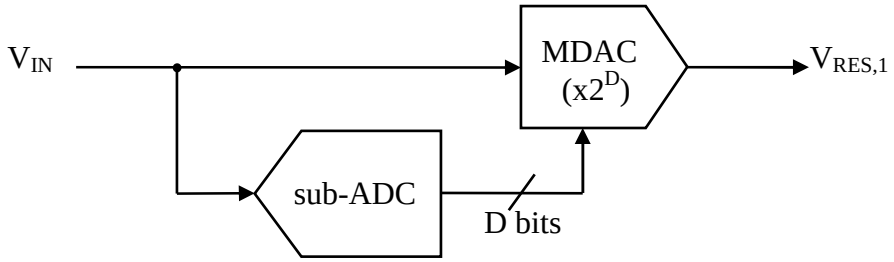


Figure 2.2. Block diagram of the first stage

2.2. 1-bit/stage Pipelined ADC

The prototype architecture is a single-bit-per-stage pipelined ADC. The advantage of it is simplicity and speed. The low resolution per stage reduces the requirements for the sub-ADC comparator from those of the higher resolution per stage architecture. The fewer bits per stage realized, the smaller gain for MDAC required. As the gain decreases, the bandwidth of the MDAC amplifiers increases granting higher speed for each stage to resolve their digital outputs. The only limitation for the sampling rate is the time to generate the bits for one stage. Hence, higher speed is allowed for an architecture with a fewer number of bits per stage.

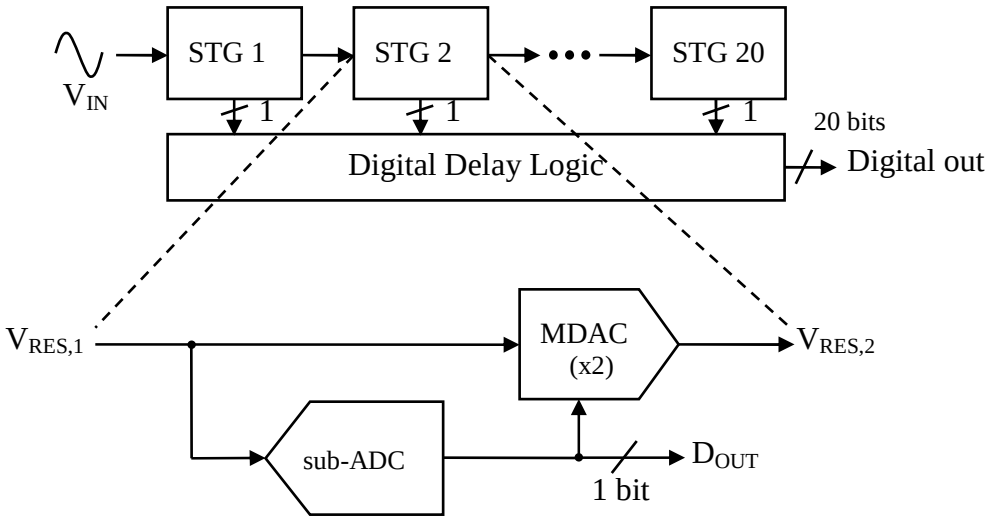


Figure 2.3. 1-bit/stage pipelined ADC

A 1-bit/stage pipelined ADC with 20 stages is illustrated in Figure 2.3. The input range is from $-V_{REF}$ to $+V_{REF}$. With the sampled input at the first stage, each stage produces a corresponding single bit at their proper clock cycle. The sub-ADC threshold is the midpoint between $-V_{REF}$ and $+V_{REF}$. The prototype uses the common-mode voltage for the comparator threshold because the system is unipolar. For the purpose of simple explanation, a bipolar system is considered. In a bipolar system, the sub-ADC threshold is zero. The operation of the ADC is shown in Figure 2.4. Only the first three stages are shown for simplicity. If the input of a stage is greater than zero, the digital output is one and the input is subtracted by $+V_{REF}$ and amplified by the gain of two. If the input of a stage is less than zero, the digital output is zero and the input is subtracted by $-V_{REF}$ and amplified by two. Then, the residue transfer function is as follows:

$$V_{RES} = \begin{cases} 2 \cdot \left(V_{IN} - \dfrac{V_{REF}}{2} \right) & if\ V_{IN} \geq 0,\ D = 1 \\ 2 \cdot \left(V_{IN} + \dfrac{V_{REF}}{2} \right) & if\ V_{IN} < 0,\ D = 0 \end{cases} \tag{2.2}$$

A graphical representation of the residue transfer function is shown in Figure 2.5.

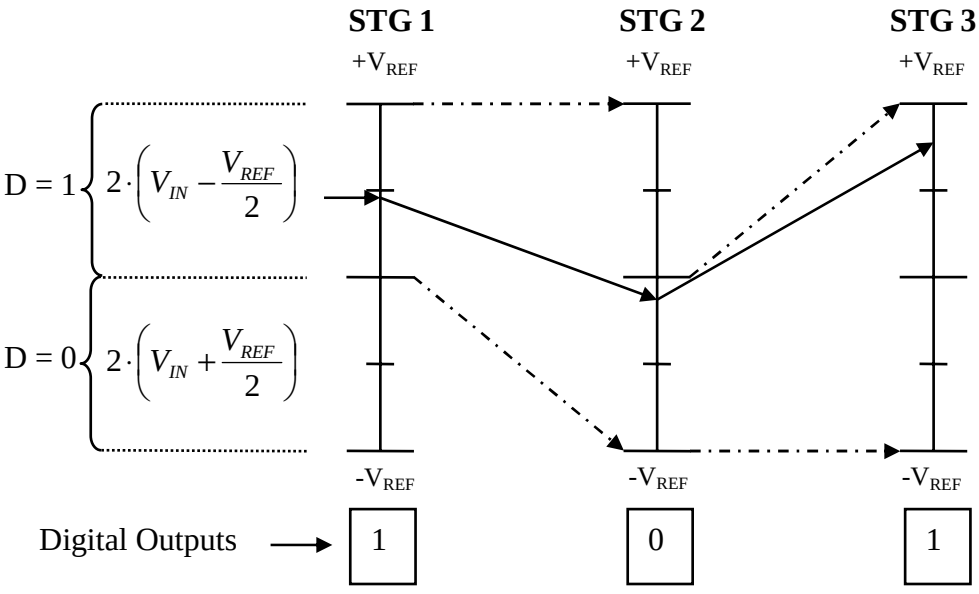


Figure 2.4. Operation of pipelined ADC stages

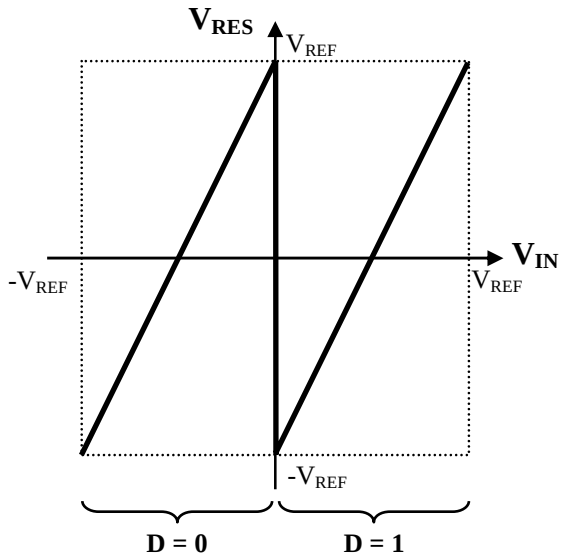


Figure 2.5. Ideal residue transfer characteristics of a pipeline stage

The digital output of the pipelined ADC can be expressed with Eq. 2.1. Substituting 20 for N, the digital output is the following:

$$D_{OUT} = D_1 \cdot 2^{19} + D_2 \cdot 2^{18} + \cdots + D_{20} \tag{2.3}$$

The radix used to resolve D_{OUT} is two, which is directly multiplied to the stage output bits with proper exponents.

A detailed structure of an ideal MDAC used in a pipeline stage is illustrated in Figure 2.6. In the sampling phase ϕ_1, V_{IN} is sampled in C_S and the op amp is reset as the charge in C_F is discharged to ground. In the amplifying phase ϕ_2, $+V_{REF}/2$ is sampled if the digital output of the stage is high. $-V_{REF}/2$ is sampled otherwise. The sampled reference voltage is subtracted from V_{IN} and multiplied by radix 2. This operation can be expressed by solving the charge equation. The result is shown in Eq. 2.4.

$$V_{RES} = \frac{C_S}{C_F} \cdot \left(V_{IN} \pm \frac{V_{REF}}{2} \right) \tag{2.4}$$

Since $C_S = 2C_F$, Eq. 2.5 shows the resulting expression of the residue voltage of each pipeline stage.

$$V_{RES} = 2 \cdot \left(V_{IN} \pm \frac{V_{REF}}{2} \right) \tag{2.5}$$

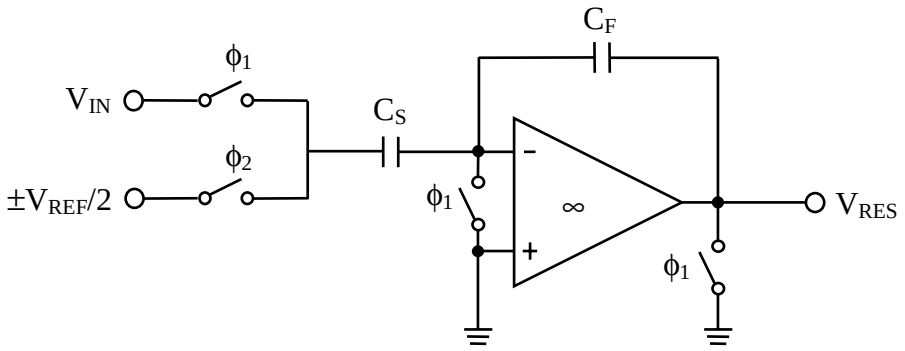


Figure 2.6. Ideal MDAC used in a pipelined stage

2.3. Error Sources in 1-bit/stage Pipelined ADC

Generally, the primary sources of error in a 1-bit/stage pipelined ADC are capacitor mismatch, finite op amp DC gain, charge injection by the sampling switches in MDAC, and comparator offset. These errors cause missing codes and missing decision levels, and hence require precision techniques like calibration. The effects of the errors are addressed in this section.

Some error affected residue transfer curves are shown in Figure 2.7. The first diagram demonstrates the error effect of capacitor mismatch. The effect of offset error is shown secondly. Capacitor mismatch causes the amplifier gain of 2 to be inexact as well as finite op amp DC gain. The bit change position shifts vertically in result. Consequently, the residue voltage exceeds the reference level causing some decision levels to be missed. The gap in the reference range causes missing codes. Offset errors are primarily caused by comparator offset and charge injection offset. The horizontal shift of the bit transition position is caused by comparator offset and

the vertical shift of the entire transfer curve is caused by charge injection offset. The exceeding residue voltage in the bit transition point and the lower reference boundary result in missing decision levels. The deficiency of the residue in the lower reference range near the bit transition point and the upper right reference boundary result in missing codes.

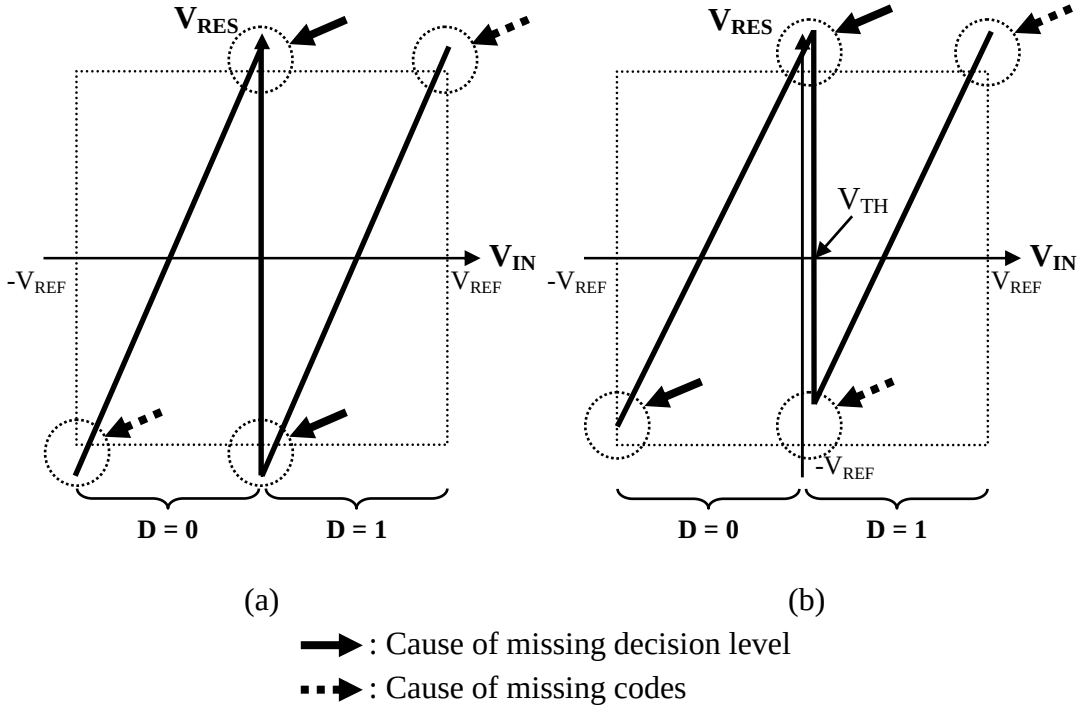


Figure 2.7. Residue transfer characteristics: (a) with capacitor mismatch; (b) with offset errors

3. REVIEW OF CALIBRATION TECHNIQUES

There are many precision techniques for various ADC architectures. Discussions of those techniques for architectures other than the pipelined structure are beyond the scope of this work. The calibration techniques for pipelined ADC presented in [8], [9], [11], and [12] are described in this chapter.

3.1. A 15-b 1-Msample/s Digitally Self-Calibrated Pipelined ADC [8]

The digital calibration technique presented in [8] employs a 1-bit/stage pipelined ADC. The primary goal of this calibration is to remove the errors discussed in the previous chapter. Figure 3.1 shows implementation of the technique.

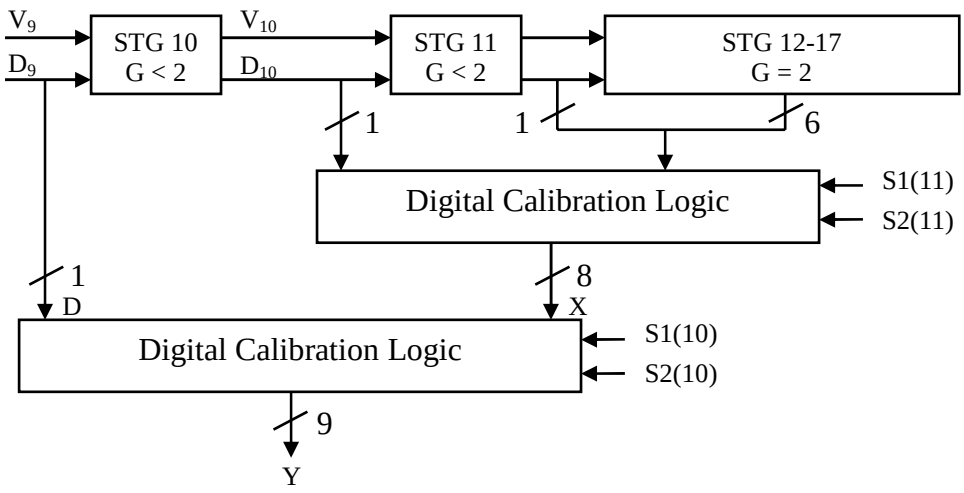


Figure 3.1. Digital calibration presented in [8]

A nominal gain less than 2 is used up to the eleventh stage to eliminate missing decision levels. The gain of stages 12 through 17 is 2. The calibration is performed from the eleventh stage back up to the first stage. S1(i) and S2(i) are the quantities of X, when $V_{i-1} = 0$ and D = 0 and D = 1, respectively, where i is the stage index. The calibration algorithm is given in Eq. 3.1.

$$Y = \begin{cases} X, \; if \;\; D = 0 \\ X + S1 - S2, \; if \;\; D = 1 \end{cases}, \tag{3.1}$$

where X is the raw data bits of the current stage plus the following stages, D is the output bit from the previous stage. Y is the calibrated output of the current stage. The calibrated output codes are used successively up to the first stage.

This technique measures the residue jumps for each stage for calibration. The errors caused by capacitor mismatch and finite DC gain are compensated. It is hard to control fluctuations of the actual residue gains. The measurements of residue jumps for the later stages are less accurate since they use fewer bits to measure the residues. The calibration depends on each stage.

3.2. A Digitally Self-Calibrated Pipelined Algorithmic ADC [9]

The calibration technique described in this paper is similar to the technique shown in [8] but incorporates a 1.5-bit/stage pipelined structure. A 1.5-bit/stage pipeline stage uses two comparators. Therefore, each stage generates three possible digital outputs, +1, 0, or -1, whereas a 1-bit/stage pipeline stage generates two possible outputs, just 1 or 0.

A 1.5-bit/stage pipeline stage is illustrated in Figure 3.2. The technique calibrates the error caused by capacitor mismatch, the only source of linearity error in 1.5-bit/stage converter is the capacitor. The capacitor mismatch can be expressed as the following:

$$C_2 = (1+\alpha)\cdot C_1, \tag{3.2}$$

where α denotes the mismatch error. Under this condition, the residue voltage is

$$V_{RES} = 2\cdot\left(1+\frac{\alpha}{2}\right)\cdot V_{IN} - D\cdot(1+\alpha)\cdot V_{REF}, \tag{3.3}$$

where D = +1, 0, or -1. In order to make the residue voltage identical to the ideal residue voltage,

$$V_{RES,ideal} = 2\cdot V_{IN} - D\cdot V_{REF}, \tag{3.4}$$

a digital correction value of $D[-\alpha V_{IN}+D(1+\alpha)V_{REF}]$ is added to V_{RES}. The rewritten digital correction value is the following:

$$D\left[-\alpha_i \cdot V_{IN}(i) + D(i) \cdot \alpha_i \cdot V_{REF}\right] = \frac{\alpha_i}{2^i}\left[\frac{D(i)}{2} - \frac{D(i+1)}{2^2} - \frac{D(i+2)}{2^3} - \cdots\right], \quad (3.5)$$

where i is the stage index. To perform the calibration, α for each stage needs to be measured.

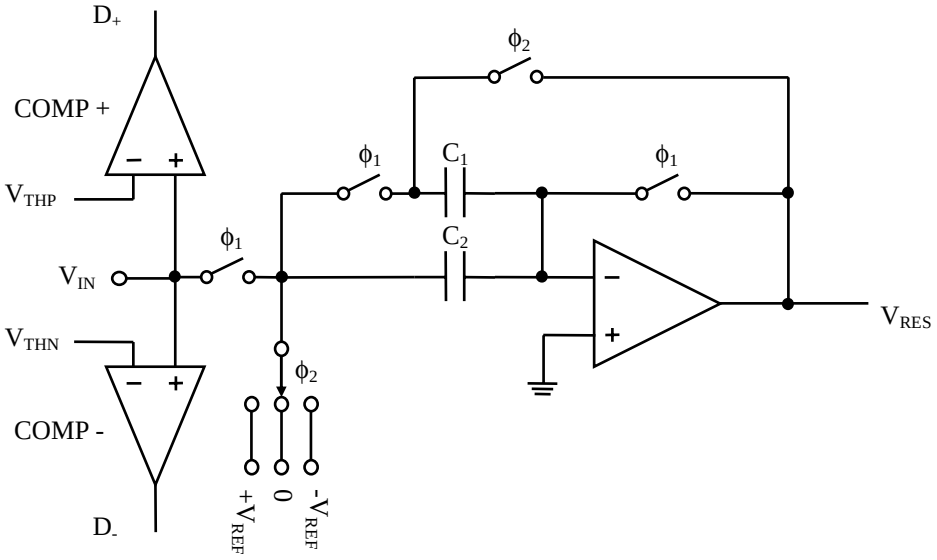


Figure 3.2. 1.5 bit/stage pipelined stage used in [9]

For this calibration technique, the quantity of capacitor mismatch is measured for each stage. A stage calibration is independent of other stages. The digital redundancy for correcting the offset errors is inherent from the 1.5-bit/stage structure. The finite DC gain, however, is not calibrated.

3.3. A Continuously Calibrated 12-b 10-MS/s, 3.3-V A/D Converter [11]

The calibration scheme employs a 1-bit/stage pipelined ADC. Adjusted comparator thresholds and reference voltages are used to perform calibration. For better understanding, transfer characteristics of a stage are depicted in Figure 3.3. The maximum analog output changes by β from the ideal positive reference V_{REFP} and the minimum analog output changes by γ from the ideal negative reference V_{REFN}. $V(n-1)_{MAX}$ and $V(n-1)_{MIN}$ denotes the maximum and minimum values of the residue

voltage when the radix is less than 2. To obtain adjusted values of threshold and reference for stage N, the stage input voltage $V_{IN,TH}$, which yields output $(1+\beta)V_{REFP}$, and V_{THA}, where the digital output of the stage transitions between 0 and 1 when compared to $V_{IN,TH}$, need to be measured. It takes two steps per stage to measure these values. Figure 3.4 and Figure 3.5 shows how these values for the N^{th} stage are measured. For the $V_{IN,TH}$ measurement, the digital output of the stage is forced to zero and the threshold voltage of the calibration comparator is set to $(1+\beta)V_{REFP}+V_{OS}$, where V_{OS} is the comparator offset. With these conditions kept unchanged, the analog input voltage to the stage is increased from 0V until the output of the calibration

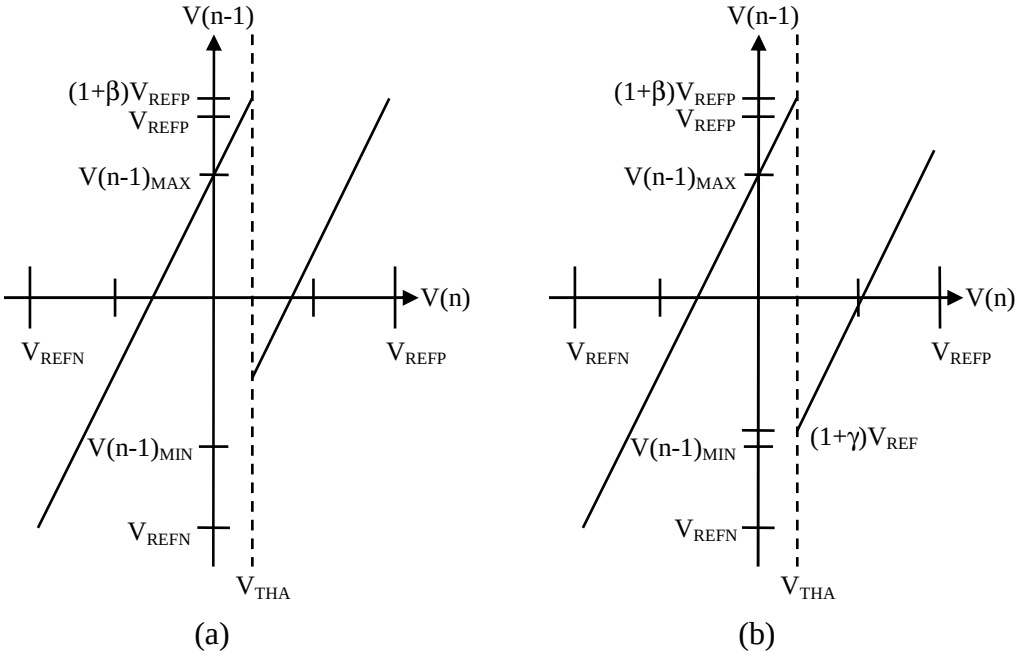


Figure 3.3. Transfer characteristics of a pipeline stage: (a) with adjusted V_{TH} and (b) after calibration [11]

comparator changes from 0 to 1. The input voltage at the output transition point is $V_{IN,TH}$. To determine V_{THA}, $V_{IN,TH}$ is fed to the comparator of the stage and compared to the varying V_{THA} until D(N) changes between 0 and 1. V_{THA} at the D(N) transition point is the desirable value. An additional calibration stage is necessary to perform this measurement process.

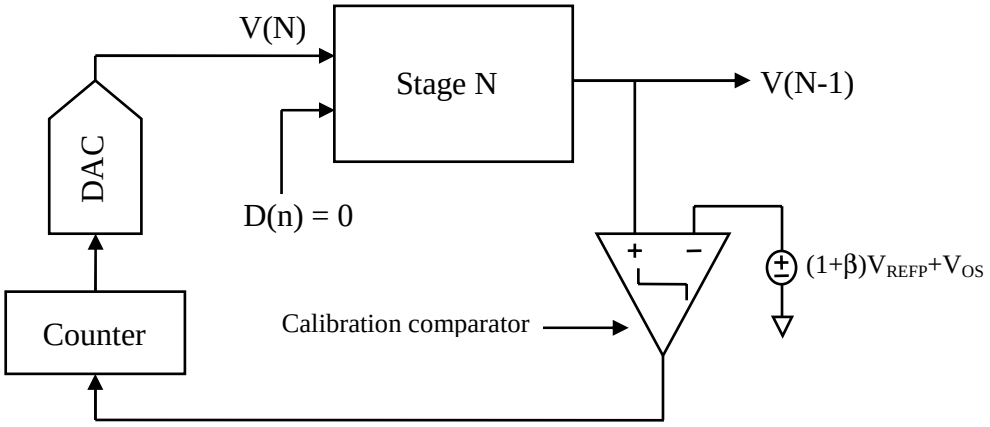


Figure 3.4. Determination of V(n) which produces output $(1+\beta)V_{REFP}$ [11]

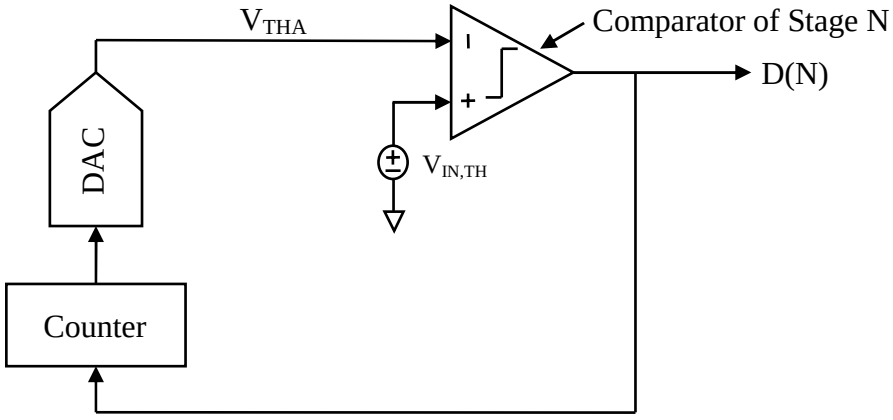


Figure 3.5. Determination of V_{THA} [11]

Both capacitor mismatch and finite DC op amp gain are compensated. The drawback is the use of an additional stage only for the calibration purpose.

3.4. A 12-b Digital-Background-Calibrated Algorithmic ADC [12]

The calibration technique proposed in this paper uses the algorithmic ADC shown in Figure 3.6. In a sense this calibration algorithm is also a radix-based calibration since the radix is measured and used for calibration. Because it is

designed only for a single stage algorithmic ADC, the linearity of the ADC solely depend upon the accuracy of the radix measurement.

To avoid missing decision levels, the residue gain is less than 2. The residue voltage for the N^{th} conversion cycle is expressed as follows:

$$V_{RES,N} = V_{IN} \cdot G^{N} - D_1 \cdot G^{N-1} \cdot V_{REF} - \cdots - D_N \cdot V_{REF}, \tag{3.6}$$

where $V_{RES,N}$ is the residue voltage of the N^{th} conversion cycle, G is the residue gain, D_N is the raw data bit of the N^{th} stage and V_{REF} is the reference voltage. The corresponding overall binary-weighted digital output is the following:

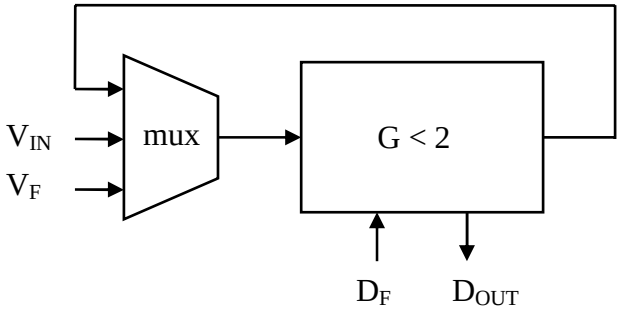


Figure 3.6. An algorithmic ADC used in [12]

$$D_{OUT} = D_1 \cdot G^{N-1} + D_2 \cdot G^{N-2} + \cdots + D_{N-1} \cdot G + D_N \tag{3.7}$$

Eq. 3.7 will produce an accurate result if the value of G is accurate. However, the actual value of G is not known initially due to its dependability on variation of capacitor mismatch and op amp gain. Therefore, the calibration algorithm focuses on the accurate measurement of G.

The inaccurate G causes the transfer characteristics to be nonlinear and it is the only cause of nonlinearity. Thus, it is necessary to obtain an accurate value of G. In order to measure the actual G, an estimate value of G is initially used in Eq. 3.7 with the analog input voltage forced to zero. With the forced input, two possible digital outputs are acquirable: the one with the MSB forced to 1 and the other with the MSB forced to 0. The difference of the two results should be 1 LSB under ideal condition.

It will not be, however, equal to 1 LSB initially because the estimate and actual values of G are different. When the difference of the digital outputs are not equal to 1 LSB, the following least mean square algorithm:

$$\hat{G}[j+1] = \hat{G}[j] + \mu \cdot (\Delta D - 1LSB), \tag{3.8}$$

where $\hat{G}$ represents the estimated value of G, μ is the update step size, ΔD is the difference between the two digital outputs, and j is an iteration index. Eq. 3.8 is processed until ΔD is 1 LSB.

Errors caused by capacitor mismatch and finite DC gain are compensated. The calibration scheme is simple, but it is only applicable for a single-stage algorithmic ADC.

4. RADIX-BASED CALIBRATION TECHNIQUE

The radix-based calibration technique described in this chapter is based on [14]. In order to perform this peculiar calibration technique in a pipelined ADC, a sub-radix-2, defined as a radix less than 2, structure needs to be used. The first section explains the necessity of a sub-radix 2 system. Discussions on the general concept of calibration technique itself and incorporation of the technique in a pipelined ADC follow.

4.1. Necessity of a Sub-Radix-2 System

An ideal operation of a radix-2 pipeline architecture was described in Chapter 2. The transfer characteristics shown in Figure 2.5 holds only if no errors are present. In reality, errors described in Section 2.3 appear usually. When the errors are taken into account, the MDAC of each pipeline stage looks like Figure 4.1.

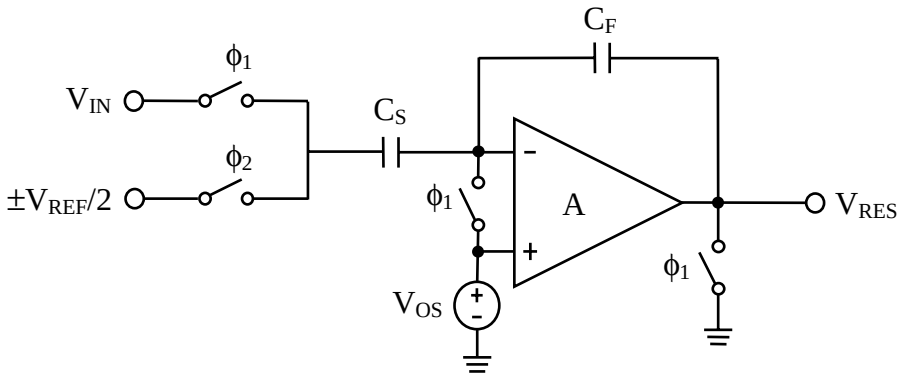


Figure 4.1 MDAC with errors

The solution to the charge equation with errors is as follows:

$$V_{RES} = \frac{(2+\varepsilon)\cdot A}{3+\varepsilon+A}\cdot\left(V_{IN} \pm \frac{V_{REF}}{2}\right) + \left(\frac{A}{3+\varepsilon+A}\right)\cdot V_{OS}\,, \qquad (4.1)$$

where ε is a capacitor mismatch error, A is a finite op amp DC gain, and V_{OS} is the op amp input offset voltage. The radix is no longer an exact 2 and the undesirable V_{OS} term is included in V_{RES}. The effect of these errors in the pipeline stage operation is shown in Figure 4.2. V_{TH} represents the threshold voltage with a comparator offset. Each stage has V_{TH} at different levels. The residue voltage of the first stage saturates in the next stage resulting in a code error. The outcome is now 011 for the example in Figure 4.2, where the expected output is 100. Due to the distinctive errors in capacitor mismatch for each stage, the reference range for each stage might be different from each other. Depending upon the quantity of capacitor mismatch in one stage, the residue voltage of the very stage can saturate in the following stage. The offset errors are generally consistent with their values. Therefore, the offset errors do not affect the linearity. Thus, the use of a sub-radix 2 will eliminate the saturation of residue voltages.

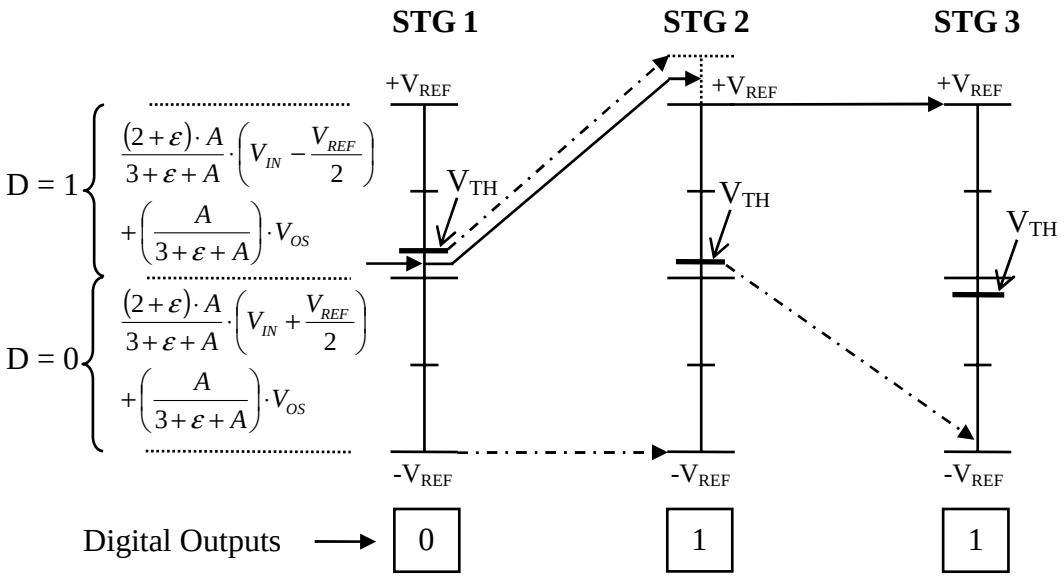


Figure 4.2. A radix-2 pipeline stage operation with errors

For a sub-radix 2 pipeline stage, the nominal capacitor ratio C_S/C_F should be less than 2. Figure 4.3 shows an MDAC used in a sub-radix 2 pipelined ADC. The

difference from a radix-2 structure is the feedback capacitance C_F contains a nominal radix selection factor ρ.

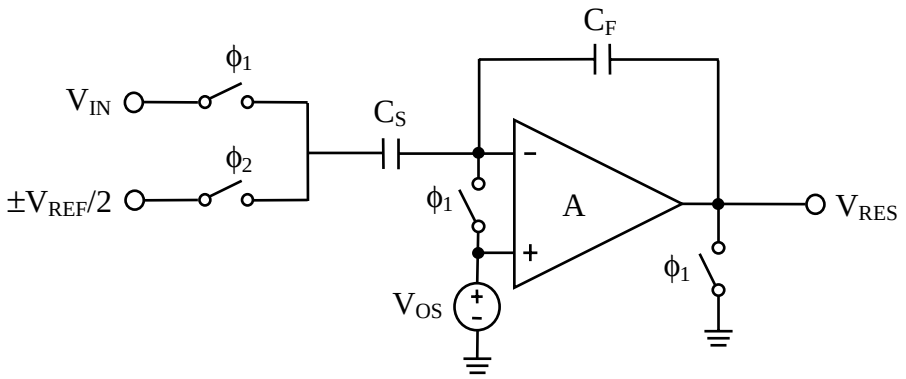


Figure 4.3. A sub-radix 2 MDAC

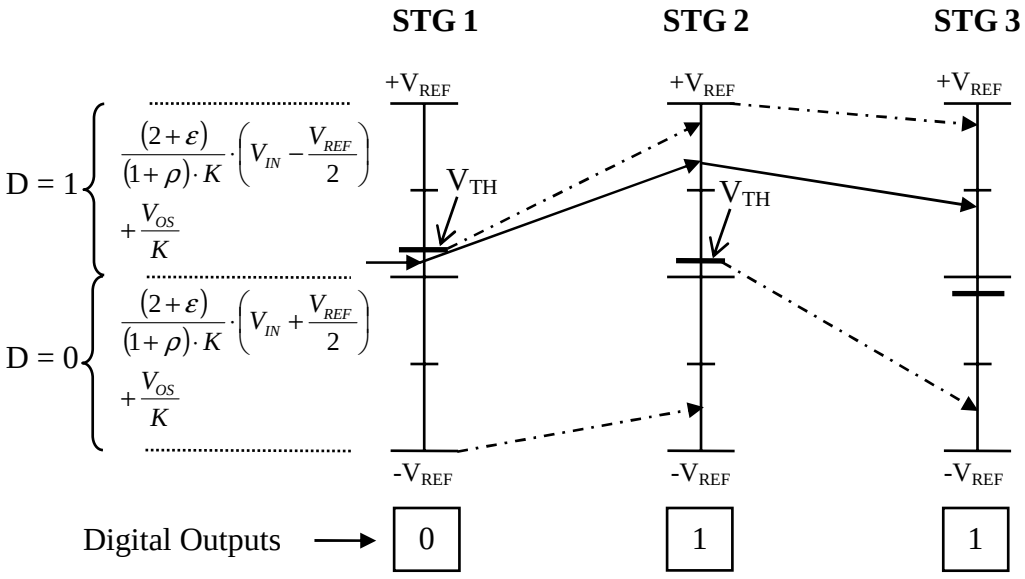


Figure 4.4. Operation of a sub-radix 2 pipeline stages

The equation for the residue voltage of a sub-radix 2 stage is the following:

$$V_{RES} = \frac{(2+\varepsilon)/(1+\rho)}{K} \cdot \left(V_{IN} \pm \frac{V_{REF}}{2} \right) + \frac{V_{OS}}{K} \tag{4.2}$$

$$\text{, where } K = \frac{(2+\varepsilon)}{(1+\rho)\cdot A} + 1 + \frac{1}{A} \tag{4.3}$$

The operation of pipeline stages based on the sub-radix 2 structure is shown in Figure 4.4. It is apparent in the illustration that the residue voltages no longer saturate in the following stages. The use of sub-radix 2 is essentially digital redundancy. Each stage produces 1-bit outputs but the resolution is less than a bit since the radix is less than 2. An expression for a radix can be expressed like the following:

$$ra = \frac{(2+\varepsilon)/(1+\rho)}{\dfrac{(2+\varepsilon)}{(1+\rho)\cdot A} + 1 + \dfrac{1}{A}} \tag{4.4}$$

4.2. Radix-Based Calibration

4.2.1. Fundamental Concept

Ideal and nonlinear ADC transfer curves are shown in Figure 4.5. For an ideal ADC each digital transition step is equal to one least significant bit (LSB). However, the nonlinear transfer curve indicates step sizes other than 1 LSB. In order to correct the nonlinearity, the use of correct radices for each stage is needed. The digital out using radices is given in Eq. 4.5.

$$\begin{aligned} D_{OUT} = {} & D_1 \cdot ra_1 \cdot ra_2 \cdots\cdots ra_{N-1} + D_2 \cdot ra_2 \cdot ra_3 \cdots\cdots ra_{N-1} + \cdots \\ & + D_{N-2} \cdot ra_{N-2} \cdot ra_{N-1} + D_{N-1} \cdot ra_{N-1} + D_N \end{aligned} , \tag{4.5}$$

where ra_i, i = 1, 2, … , N-1, is the radix for the i^{th} stage and D_i, i = 1, 2, … , N, is the output bits from the i^{th} stage. The more accurate radices are, the better the ADC transfer curve is. However, immediate recognition of accurate radices is impossible due to capacitor mismatch and other miscellaneous errors. Therefore, an accurate measurement of radices is necessary for calibration.

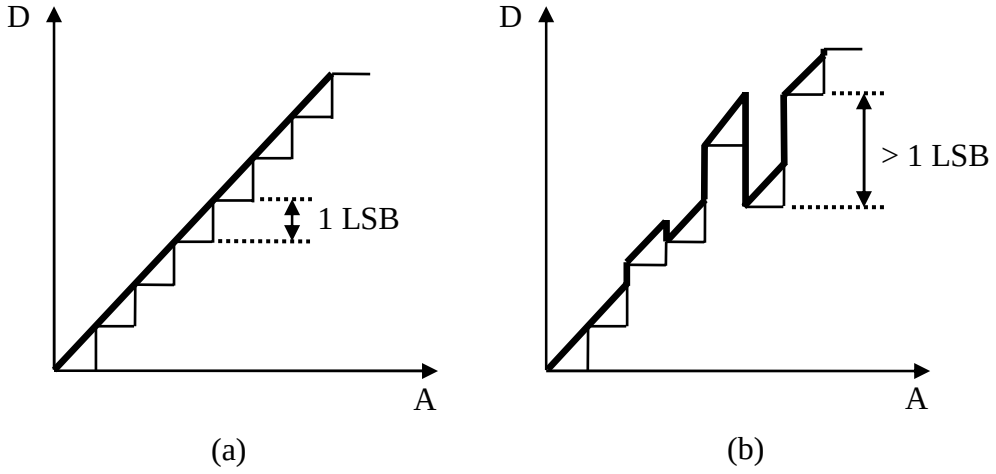


Figure 4.5. ADC transfer curves: (a) Ideal; (b) Nonlinear

4.2.2. Radix Measurement

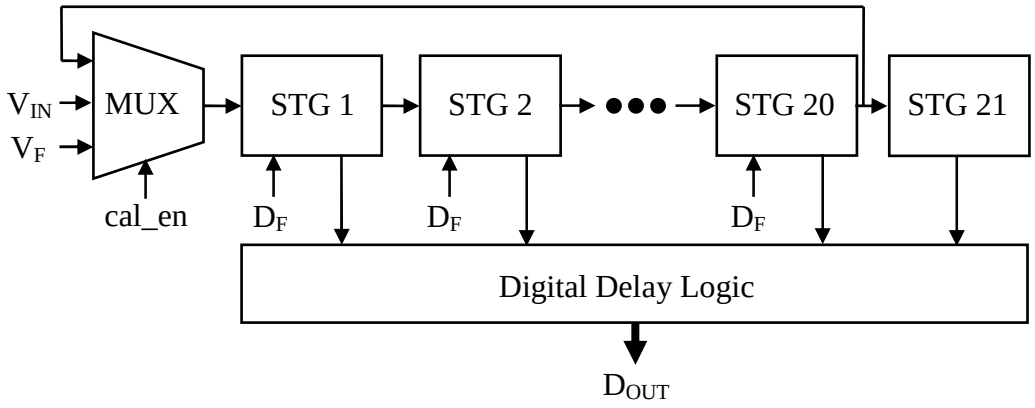


Figure 4.6. Radix measurements in a 20-stage pipelined ADC

Figure 4.6 shows radix measurements in a 20-stage pipelined ADC. V_{IN} is the input signal, V_F is the forced input signal, and D_F is the forced bit. For each radix determination two sets of D_{OUT} is required, i.e., D_{OUT} for which the MSB is forced to one and D_{OUT} for which the MSB is forced to zero while V_{IN} is set to V_{CM}. The MSB of the i^{th} data set is D(i). For example, the raw sequence of D_{OUT} for the ra_1 measurement is D(1)D(2)…D(19)D(20)D(21), that of D_{OUT} for the ra_2 measurement is

$D(2)D(3)\ldots D(20)D(1)D(2)_{unforced}$, and so forth. $D(2)_{unforced}$ denotes the unforced digital output from the second stage. For a precise bit match the unforced bit of the forced stage is needed.

Eq. 4.5 is used to calculate D_{OUT} with the raw data for each radix measurement. The difference between the zero-forced D_{OUT} and the one-forced D_{OUT} is compared to 1 LSB and corrected until it is equal to 1 LSB. The iterative equation used for each radix measurement is as follows:

$$ra[n] = ra[n-1] - \delta \cdot \left(D(1) - D(0) - 1LSB\right), \tag{4.6}$$

where n is the iteration index, δ is the correction increment, D(i), i = 0 and 1, is the digital output of the ADC when the MSB is forced to i with zero input. Note that δ should be much smaller than 2^N for an N-bit ADC. In each iterative correction process, the most recently updated radices are used.

5. CIRCUIT IMPLEMENTATION OF A PIPELINED ADC WITH RADIX-BASED CALIBRATION

The circuit-level component blocks of the 20-stage pipelined ADC are discussed individually in this chapter. The circuits are designed so that the calibration mode reflects in the same circuitry. The TSMC 0.35μm CMOS technology is used to design circuits.

5.1. Timing of the Pipelined ADC

Phase	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2
Stage 1 *Sub-ADC 1* preamp comp. latch *MDAC 1*		S(CM)	A T S (Input)	L(D1) A (Res1)						
Stage 2 *Sub-ADC 2* preamp comp. latch *MDAC 2*			S(CM)	A T S (Res1)	L (D2) A (Res2)					
Stage 3 *Sub-ADC 3* preamp comp. latch *MDAC 3*				S(CM)	A T S (Res2)	L (D3) A (Res3)				
LATCH1,1 LATCH1,2 LATCH1,3				T	L (D1) T	L (D1) T	L (D1)			
LATCH1,19 LATCH1,20									L (D1) T	L (D1)
LATCH2,1 LATCH2,2 LATCH2,3					T	L (D2) T	L (D2) T	L (D2)		
LATCH2,18 LATCH2,19									L (D2) T	L (D2)
LATCH19,1 LATCH19,2									L(D19) T	L(D19)
LATCH20,1									T	L(D20)

Figure 5.1. Timing diagram of ADC operation

The pipelined ADC operates by the timing scheme shown in Figure 5.1. Only the first three stages are described for simplicity. The rest of the stages operate in the same manner. Note that S represents sampling, A amplifying, T tracking, and L latching in Figure 5.1. The clock phases for even and odd stages are interleaved. In other words, the even stages amplify when the odd stages sample their inputs and vice versa. The number of latches decreases toward the end of pipeline to align data bits from each stage at the same clock phase.

The schematic of a pipeline stage is shown in Figure 5.2. Both MDAC and sub-ADC are fully differential. MDAC for the first stage has an additional switch circuitry for the calibration loop. The rest of the stages are identical. Signals V_F, D_F, and F_EN are used only in the calibration mode. The following sections detail MDAC and sub-ADC.

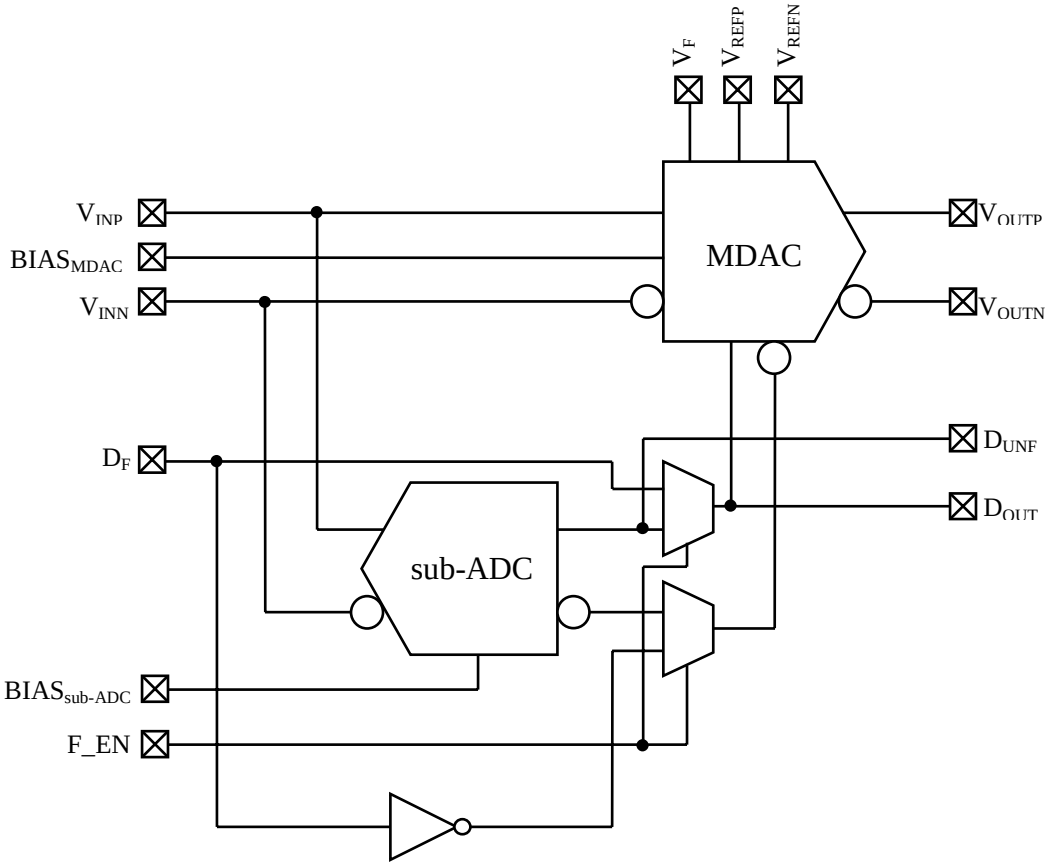


Figure 5.2. Schematic of a pipeline stage

5.2. Multiplying Digital-to-Analog Converter

A fully differential MDAC is shown in Figure 5.3. The power supply voltage is 3.3V and the input and output signal range is 2Vpp. The common-mode voltage V_{CM} is set to 1.65V, the midpoint of the supply voltage range, to allow sufficient headroom for the signal range. The reference voltage range is identical to the signal range. Thus, the maximum and minimum reference voltages are 2.65V and 0.65V, respectively. REFP and REFN are the half point of the positive and negative reference range, respectively.

Switches on the signal path should be realized with transmission gates to avoid malfunction due to the varying nature of the signal. Correspondingly, the transistors M1 through M4 compose the transmission gate input switches. The switch control signals, V_{IN}_en, V_{IN}_enB, and V_F_en are based on the sampling clock phase. In the normal ADC operation mode, M1-M4 are turned on to sample the input during the sampling phase, while M5 and M6 are turned on in the calibration mode.

The digital logic circuitry shown in Figure 5.3 determines which reference voltage should be connected in the amplifying phase. The control voltage A and C connect REFP and B and D connect REFN to the bottom plate of the sampling capacitor.

The thermal noise should be considered when deciding the size of the sampling capacitors in MDAC. It has been designed for 16-bit resolution for which 1 LSB is about 30.5μV with 2V reference range. To suppress the noise level below the LSB level, an adequate capacitor size can be determined by the equation following:

$$1LSB > \sqrt{\frac{kT}{C}}, \tag{5.1}$$

where k is Boltzmann's constant, T is the absolute temperature, and C is the capacitance of the sampling capacitor. From Eq. 5.1, it can be shown that the noise level is about 22μV if C = 8pF, which is well below the LSB level.

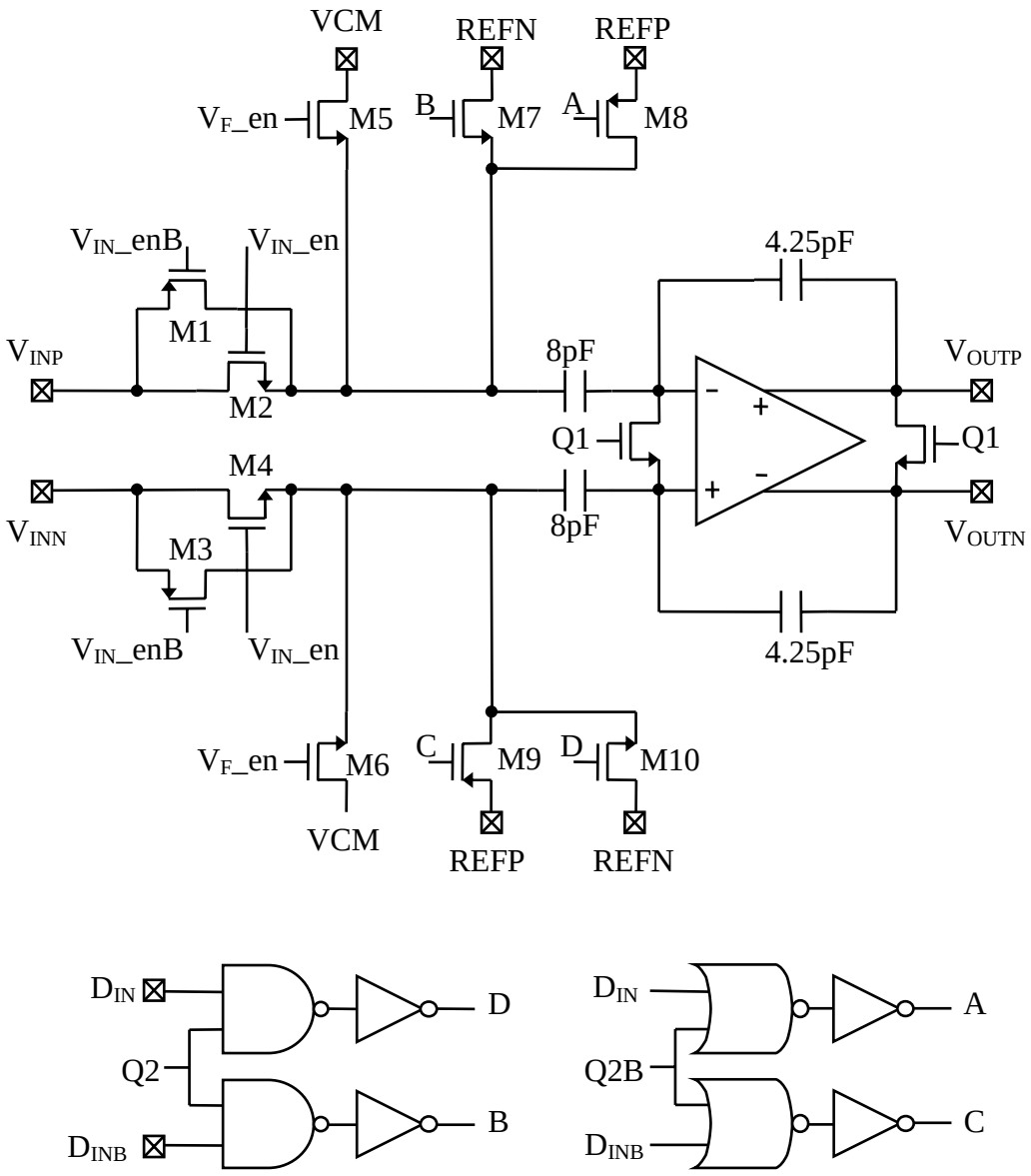


Figure 5.3. Circuit diagram of MDAC

5.2.1. Operational Amplifier

A simple one-stage op amp fits the purpose to realize the pipelined ADC. The commonly used fully differential folded cascode op amp [17] shown in Figure 5.4 is implemented in the MDAC. For the pipelined ADC, the op amp is designed to meet the following specifications: the op amp DC gain greater than 60dB, the minimum unity-gain bandwidth of 25MHz, settling to ±1/2 LSB within a half clock phase, and the output swing of at least 2Vpp with a supply voltage of 3.3V. The input sampling frequency is 5MHz. A design procedure of the op amp is explained next.

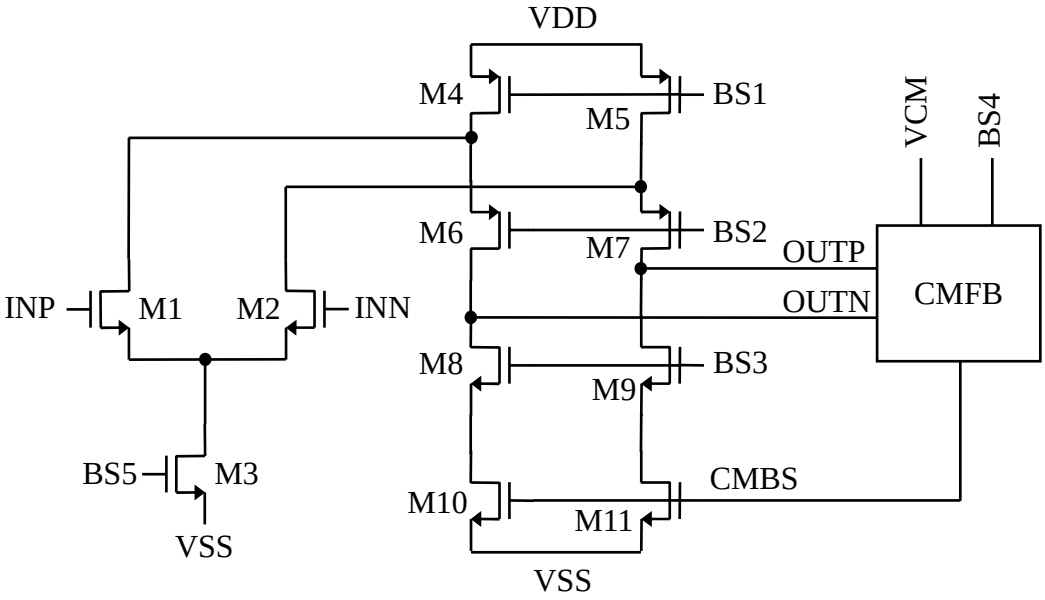


Figure 5.4. Schematic of the Op Amp

The feedback factor β needs to be determined to begin. The sampling capacitor and feedback capacitor are the main components to calculate β. Such a relationship is found to be:

$$\beta = \frac{C_F}{C_S + C_F + C_P}, \tag{5.2}$$

where C_S is the sampling capacitance, C_F is the feedback capacitance, and C_P is the parasitic capacitance seen at the input of the op amp. From the equation, β is about 1/3. Then, the settling time can be calculated from the following equation:

$$V_{OUT}(t) = V_{STEP} \cdot \left(1 - e^{-\frac{t}{\tau}}\right), \tag{5.3}$$

where $V_{OUT}(t)$ is the output voltage with respect to time, V_{STEP} is the maximum output voltage level, and

$$\tau = \frac{1}{\beta \cdot \omega_{UNITY}}, \tag{5.4}$$

where ω_{UNITY} is the unity-gain frequency. Since the accuracy objective is 16 bits, a margin of 1 bit should be allowed to achieve the ±1/2 LSB settling. From Eq. 5.3, the settling time, t, is 12τ. Denoting a clock period to be T_S, the settling time must be less than a half of it. For safety, t is set to $3T_S/8$ for this application. Once the approximate settling time is determined, the transistor transconductance g_m can be calculated from the following equations:

$$\omega_{UNITY} = \frac{g_m}{C_L} = \frac{1}{\beta} \cdot \omega_{-3dB} \tag{5.5}$$

$$g_m = \frac{1}{\beta} \cdot \omega_{-3dB} \cdot C_L \tag{5.6}$$

With the calculated g_m and selected I_D, the drain current, the size of the input devices can be determined from the following:

$$g_m = \sqrt{2 \cdot \mu \cdot C_{OX} \cdot \left(\frac{W}{L}\right) \cdot I_D} \;\rightarrow\; \frac{W}{L} = \frac{{g_m}^2}{2 \cdot \mu \cdot C_{OX} \cdot I_D}, \tag{5.7}$$

where μ_n is the mobility of electrons, C_{OX} is the gate capacitance per unit area, and W/L is the width-to-length ratio of the transistor device. For the TSMC 0.35μm technology, $\mu_n C_{OX}$ is 188.8μA/V^2 and $\mu_p C_{OX}$ is -63.2μA/V^2. The size of the rest of the transistors are determined using Eq. 5.7.

I_D can be selected considering an appropriate slew rate. The slew rate is the following:

$$SR = \frac{I_{D,IN}}{C_L} = \frac{dV_{OUT}}{dt}, \tag{5.8}$$

where $I_{D,IN}$ is the drain current of the input device and C_L is the load capacitance.

One condition needed to be considered is the device resistance for determination of the transistor sizes since the DC gain directly depends on them. The gain equation is as follows:

$$A = g_{m1} \cdot \left(g_{m6} \cdot r_{O4} \| g_{m8} \cdot r_{O10}\right), \tag{5.9}$$

where g_{m1} is the transconductance of M1, g_{m6} is that of M6, g_{m8} is that of M8, r_{O4} is the resistance of M4 and r_{O10} is that of M10.

5.2.2. Common-Mode Feedback

Due to the fully differential nature, the common-mode voltage at the output of the op amp is not stable without a common-mode feedback (CMFB) circuitry. The CMFB circuit used for this application is specified in Figure 5.5. A voltage divider is formed by capacitors C2 and C3 to sense the common-mode output voltage. The common-mode output voltage is adjusted to the desirable common-mode voltage VCM by C1 and C4 with switches operated by the two different clock phases. In the amplifying phase Q2, VCM is sampled on both C1 and C4. Then, the adjustment of the common-mode voltage is done in the sampling phase Q1. The desirable common-mode voltage is reached over time.

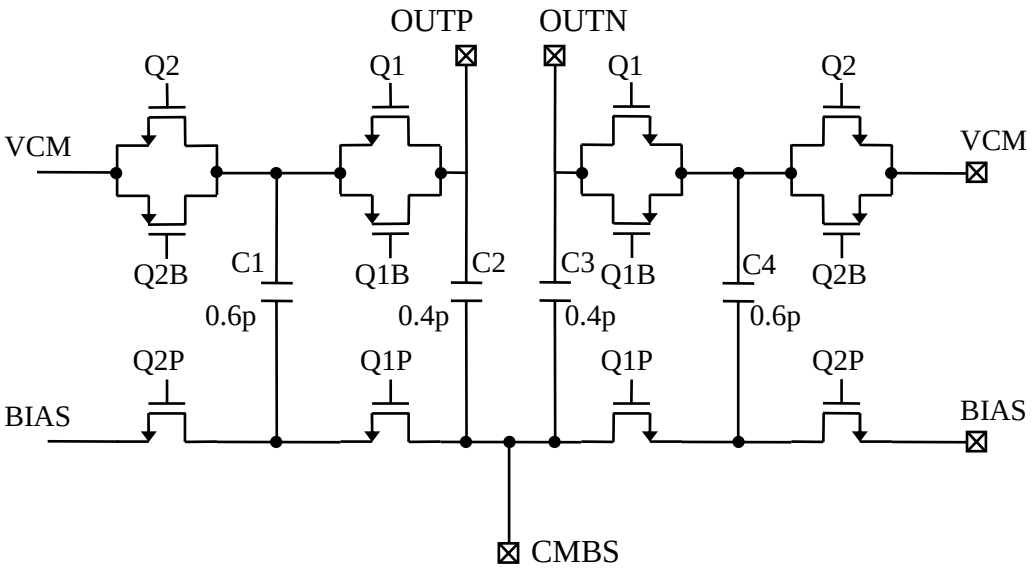


Figure 5.5. Common-mode feedback circuit

5.2.3. Biasing

The op amp bias voltages are generated by the circuitry shown in Figure 5.6. To minimize dependability between bias voltages, each branch generates a single bias voltage. The bias current of 50μA flows into IBIAS. This circuit sets the DC levels for each bias voltage generated such that the output swing of the op amp satisfies the 2Vpp range. The effective gate-source voltage, Δ is defined as follows:

$$\Delta = V_{GS} - V_{TH}\,, \tag{5.10}$$

where V_{GS} is the gate-source voltage and V_{TH} is the threshold voltage. For the technology used, V_{TH} of the N-channel transistor is 0.54V and that of the P-channel transistor is 0.75V. The bias voltages B1 through B5 are 2.252V, 2.096V, 1.12V, 0.867V, and 0.867V, respectively. Δ_4 is then 0.298V, Δ_6 0.154V, Δ_8 0.253V, and Δ_{10} 0.327V. The maximum output voltage is 2.846V and the minimum is 0.58V in order for all the transistors to operate in the saturation region. This limit suits the desirable output voltage range from 0.65V to 2.65V.

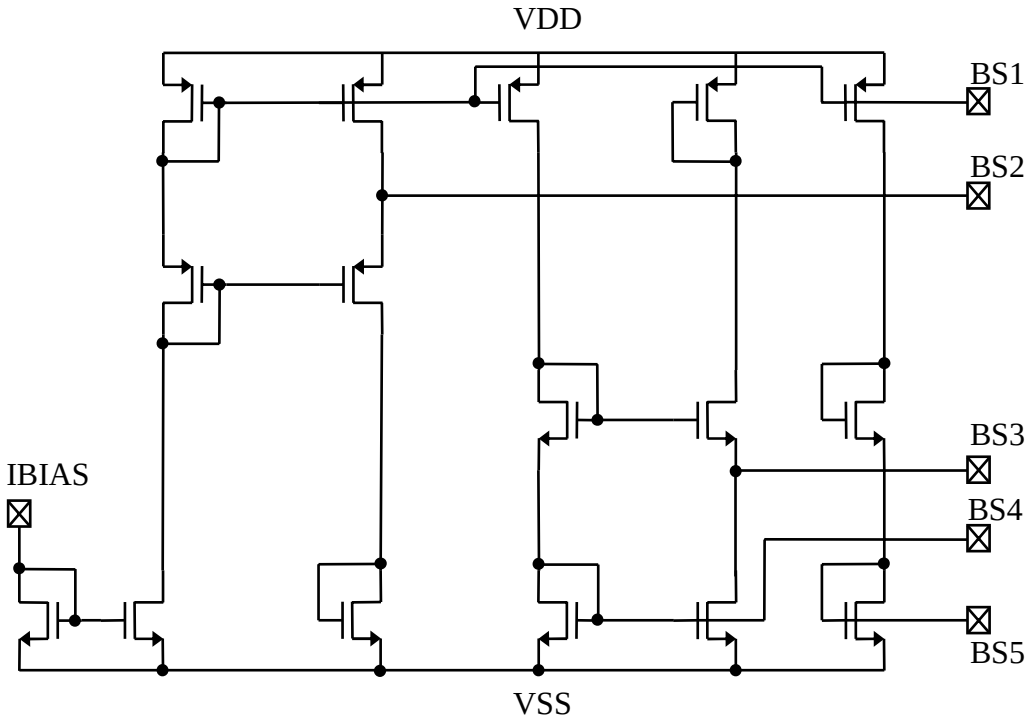


Figure 5.6. Op Amp Bias Circuit

5.2.4. Simulation Results

The results of AC analysis and transient analysis are shown in Figures 5.7 and 5.8, respectively. The AC analysis results show that the loop gain is 54dB and phase margin is about 86 degrees. A differential DC signal is injected into the input of MDAC for the transient analysis. The result shown in Figure 5.8 is the differential output of MDAC. The transient analysis results show that the settling time is about 50ns.

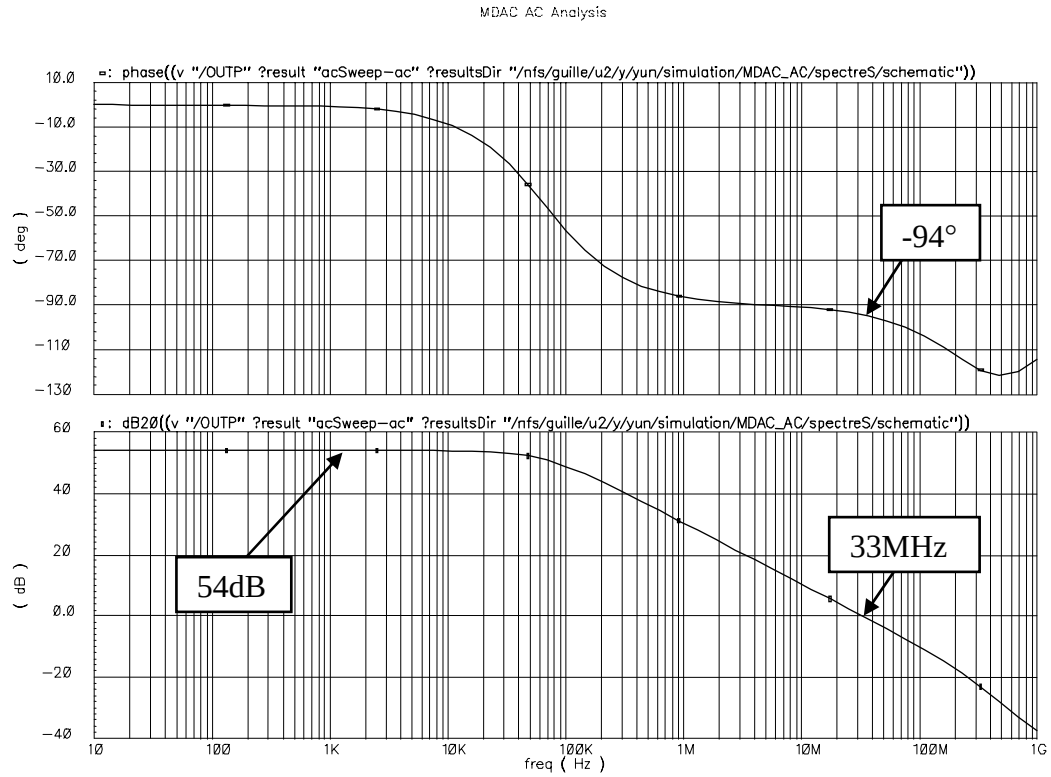


Figure 5.7. AC analysis of MDAC

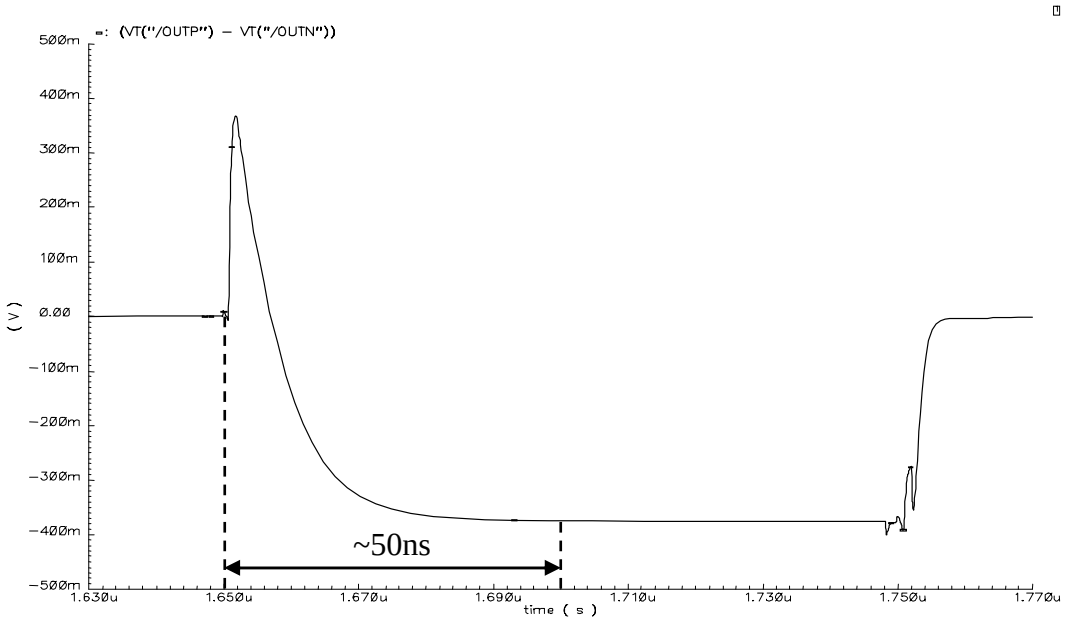


Figure 5.8. Transient analysis of MDAC

5.3. Sub-ADC

The sub-ADC for the 1-bit/stage is merely a comparator. The top-level schematic of the comparator is shown in Figure 5.9. A switched capacitor circuit is used to realize the comparator and it operates based on the same two clock phases as those for MDAC.

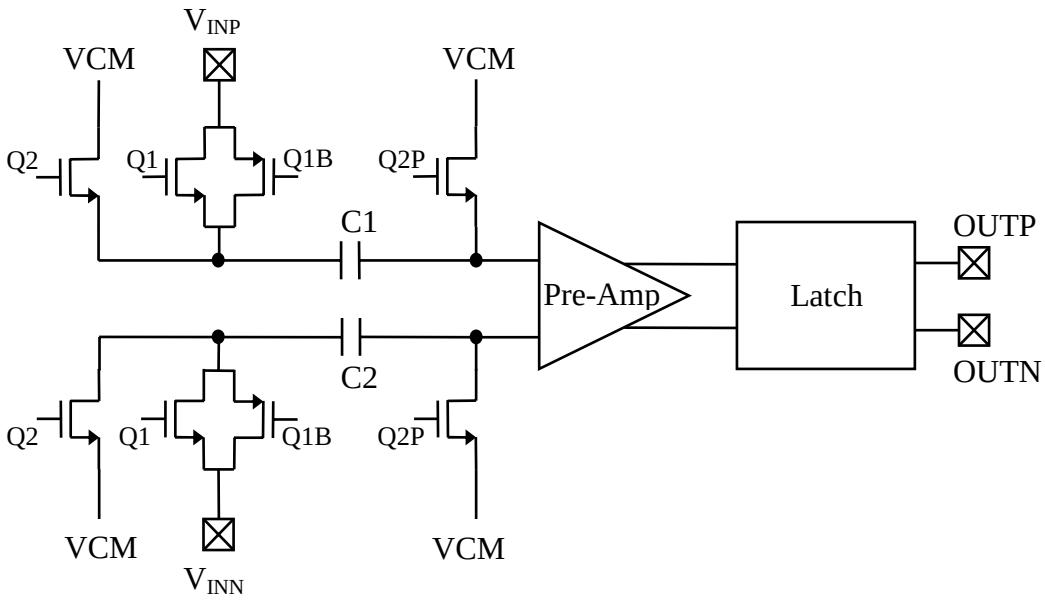
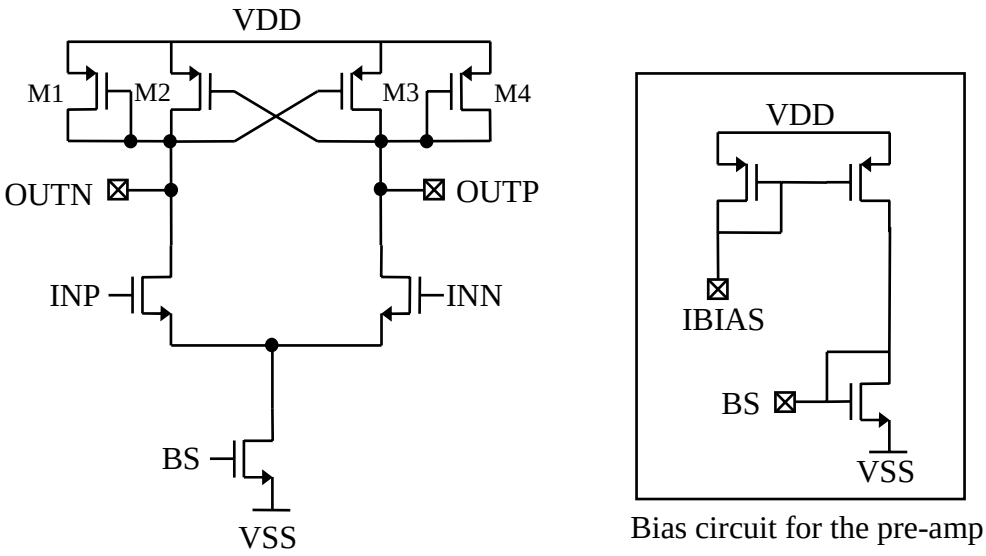


Figure 5.9. Schematic of the comparator

In the amplifying phase Q2, the sampling capacitors C1 and C2 samples the common-mode voltage VCM. In the sampling phase Q1, the input signal enters through the bottom plates of C1 and C2 and subtracts VCM. The subtracted voltage is seen at the gate of the input device of the pre-amplifier shown in Figure 5.10. M1 and M4 are diode-tied to minimize metastability at the output. The pre-amplifier is biased by the bias circuit shown in Figure 5.10. The bias current is 50μA. The pre-amplified signals are held at nodes OUTP and OUTN until Q2 turns high. The signals at OUTP and OUTN of the pre-amplifier is connected to INP and INN of the comparator latch, respectively. When Q2 is high, the outputs of the pre-amplifier are latched at the output of the comparator latch.



Bias circuit for the pre-amp

Figure 5.10. Pre-amplifier in the comparator

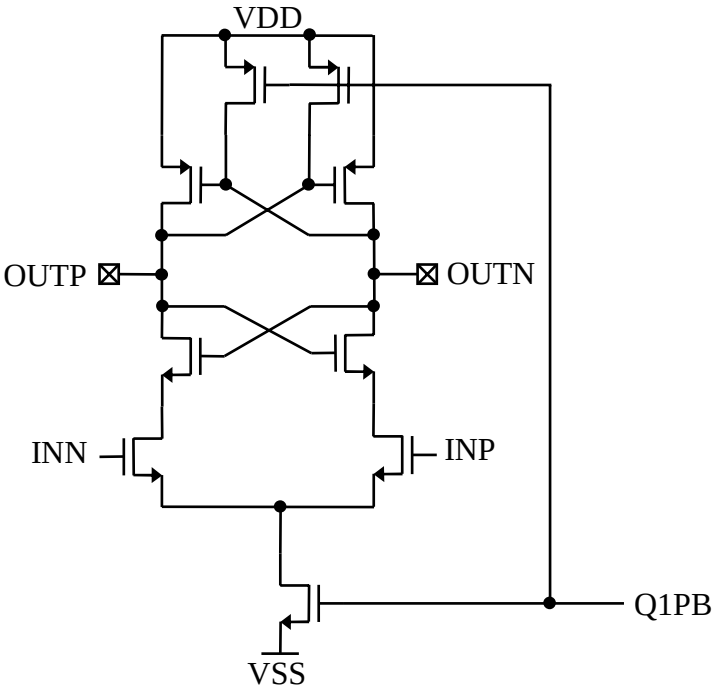


Figure 5.11. Comparator latch

5.4. Latch Block

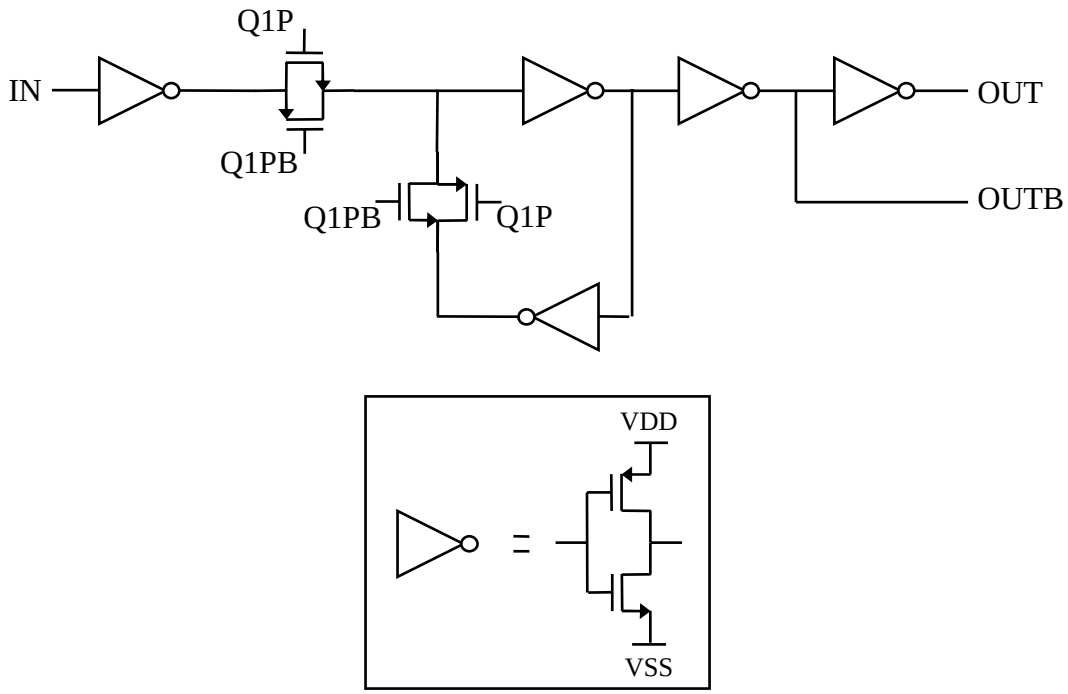


Figure 5.12. Latch block

Figure 5.12 illustrates one latch block used to align the output data in the digital delay logic block shown in Figure 4.6. The latch delays the incoming data for a half clock cycle. In the sampling phase, the input data passes through the series of inverters out to the node OUT. In the amplifying phase, the input data is latched in the latch loop.

6. SIMULATION RESULTS

System level and circuit level simulations are done to verify the radix-based calibration in the 20-stage pipelined ADC. The system level simulation is done in MATLAB. Spectre is used to simulate the circuit. The following figures plot the simulation results from both cases.

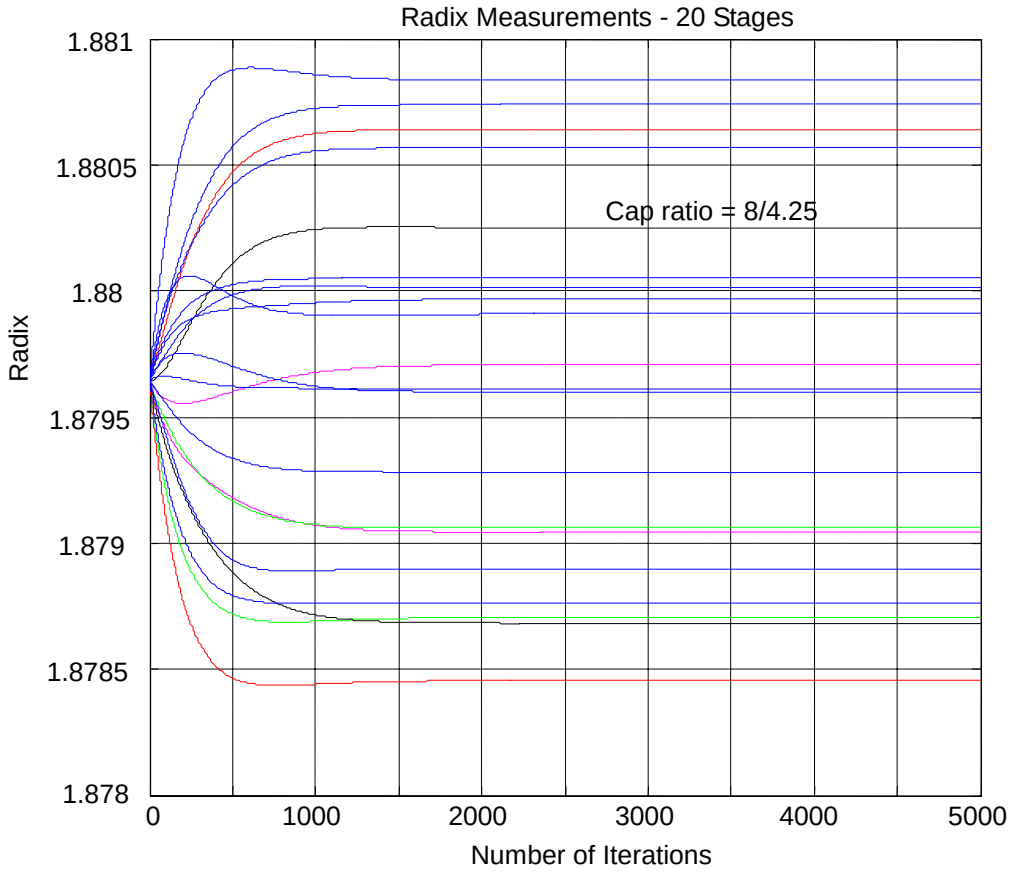
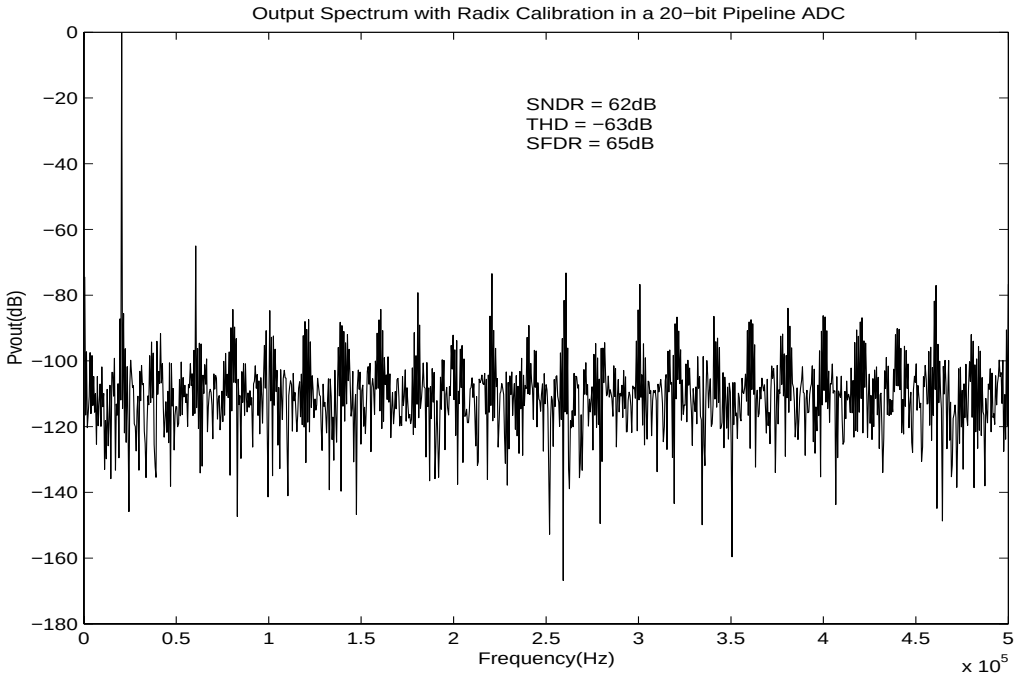
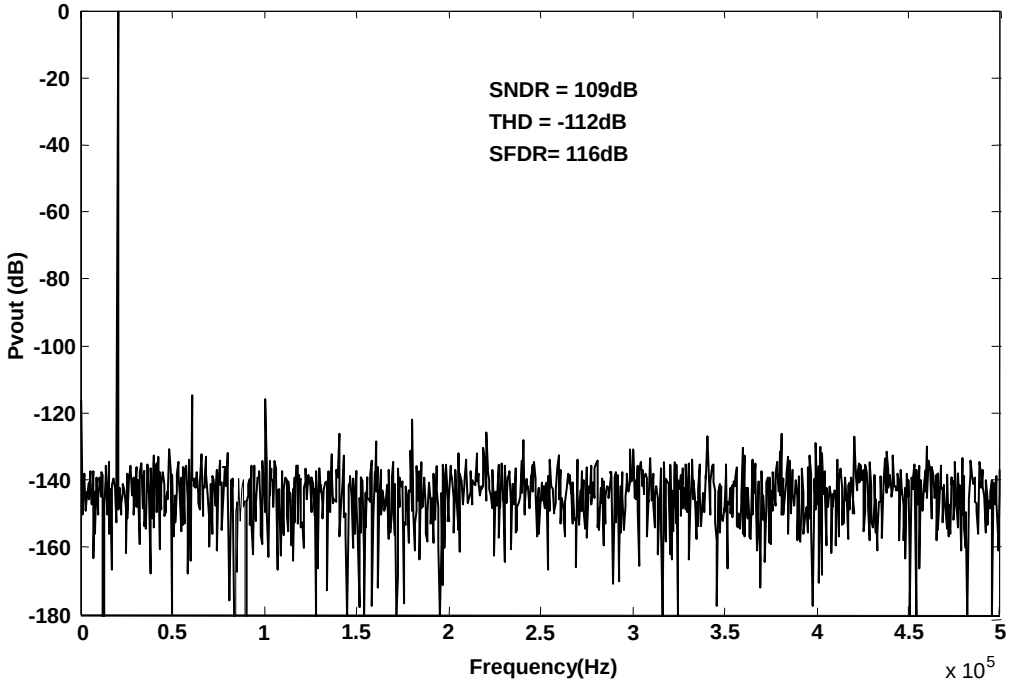


Figure 6.1. Radix measurements

Radix measurements of each stage is shown in Figure 6.1. The nominal capacitor ratio was 8/4.25. The randomly generated capacitor mismatch is 0.5% and the total offset voltage was 50mV. The plot manifests that each radix is corrected to their own values as the iteration process proceeds.

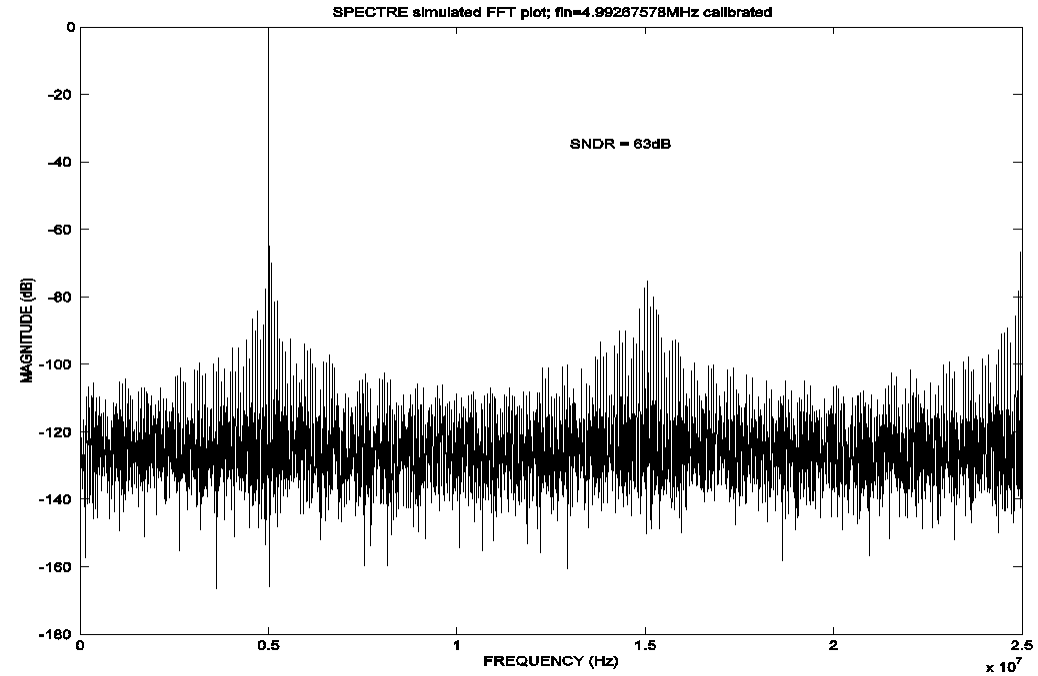


(a)

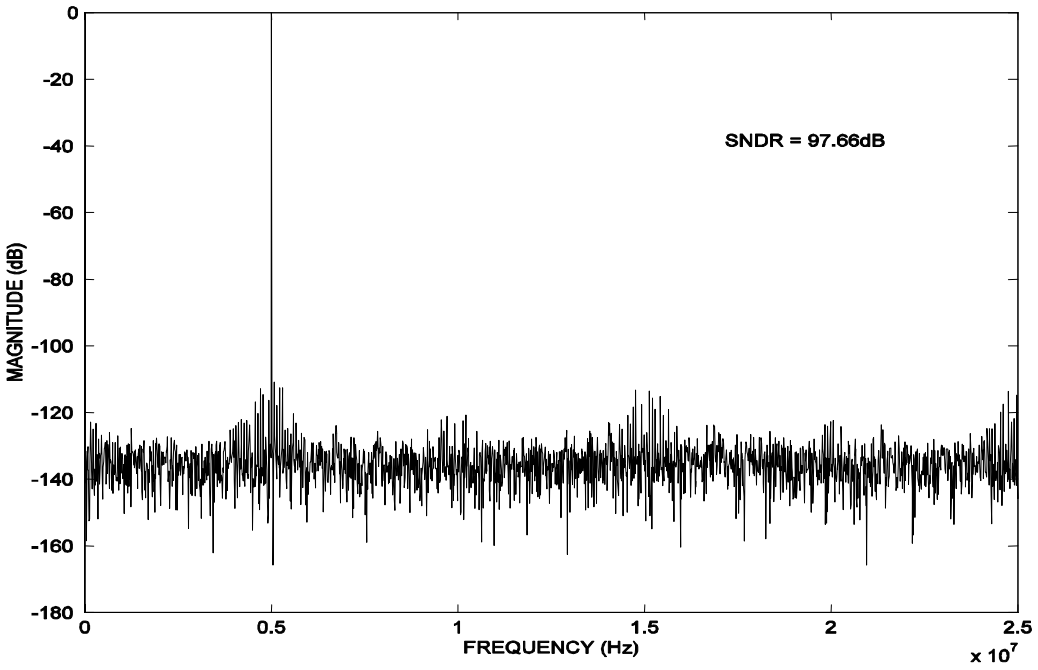


(b)

Figure 6.2. FFT plot of MATLAB simulation: (a) before calibration and (b) after calibration



(a)



(b)

Figure 6.3. FFT plot of the circuit level simulation: (a) before calibration and (b) after calibration

Figure 6.2 shows the FFT plots of the system level simulation both before and after calibration. Figure 6.3 shows the same plots for the circuit level simulation. SNDR before calibration are about the same at 63dB for both cases. The results from the system level simulation show that SNDR is 109dB, whereas the circuit simulation results show that SNDR is only 97.66dB after calibration. The effective resolution is about 16 bits for the circuit level simulation, which is closer to the reality.

7. CONCLUSION

A 20-stage pipelined ADC with radix-based calibration is presented to verify the capability of the radix-based calibration for a true multi-stage ADC in this thesis. A 1-bit/stage pipelined architecture is used for the ADC for the inherent simplicity. The radix-based calibration compensates for errors such as capacitor mismatch and finite op amp DC gain, while the use of sub-radix-2 redresses offset errors caused by charge injection and comparator offset.

The ADC is designed in the TSMC 0.35μm technology. The sampling frequency of 5MHz, the input frequency of 29.296kHz and supply voltage of 5V are used to simulate the circuit.

The system level simulation results show that the performance of the pipelined ADC is the following: SNDR is 109dB, THD is -112dB and SFDR is 116dB. The performance improves by about 50dB, which is an 8-bit accuracy improvement, after calibration. The circuit level simulation results show SNDR of only 97.66dB, thus, the accuracy improvement is only 6 bits. Calibration up to the 14^{th} stage is needed to get the accuracy shown in the results. Calibrating the rest of the stages toward the last stage does not improve the performance significantly.

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