High-Speed Switched-Capacitor Filters Based On Unity-Gain Buffers

by

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1. INTRODUCTION

Electronic filters are important blocks in many communication and instrumentation systems. Switched-capacitor (SC) and Gm-C are the most widely used implementations of integrated analog filters. Very accurate SC filters can be realized with nonlinear distortion and noise performance better than 90dB. Since an SC filter is a *sampled-data system* the clock rate (sample rate) must be at least twice that of the highest frequency to be processed in order to avoid aliasing. In many cases the clock rate is several times faster than the maximum frequency to be processed in order to reduce anti-aliasing filter requirements. This limits the ability of SC filters to process high-frequency signals. Gm-C filters are *continuous-time filters*. With no inherent limitations due to sampling requirements Gm-C filters have a significant speed advantage over SC filters. While the Gm-C filter can process high-frequency signals there are several drawbacks to this architecture. Potentially complex tuning circuitry is required to realize accurate filters. This is due to the fact that, unlike SC filters, Gm-C filter coefficients are determined by the product of two dissimilar elements such as resistors and capacitors. Achievable nonlinear distortion and noise performance is typically less than 60dB.

There are high-speed applications, such as certain data communication and video circuits, which have low distortion and noise performance requirements. Gm-C filters are suitable in these situations. In order to provide accurate high-speed analog filters with excellent distortion and noise performance it is desirable to find novel SC

circuits that can operate at clock rates of several hundred megahertz. Constructing SC filters with these novel SC circuits will allow SC filters to be operated in frequency regimes previously limited to other architectures.

High-frequency operation of conventional switched-capacitor filters is limited by the need for high-gain, large-bandwidth opamps [3]- [5]. While it is possible to realize opamps with the required gain and bandwidth, power consumption becomes an issue [6] [7]. Realizing SC filters with unity-gain buffers as active elements rather than opamps may be a solution. A simple unity-gain buffer can operate at very high-frequency with competitive power consumption.
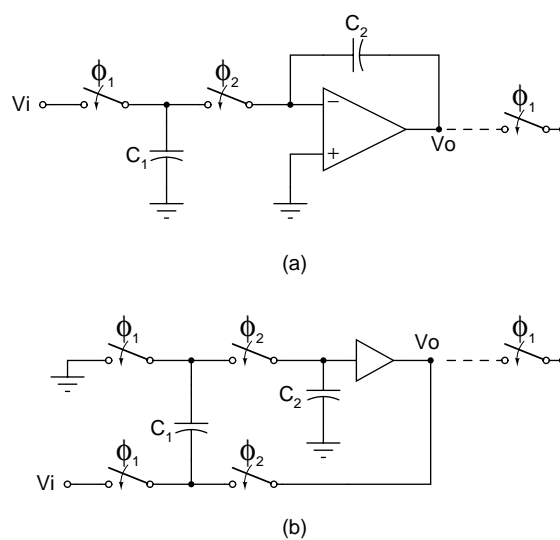
Figure 1.1. SC integrators: (a) Conventional SC integrator; (b) Unity-gain buffer SC integrator.

The SC integrator is a basic building block of many SC circuits. A conventional SC integrator is shown in Fig. 1.1 (a). This circuit operates as follows. During

clock phase ϕ_1 the input voltage is sampled by a switch and charge is stored on C_1. During clock phase ϕ_2, the top plate of C_1 is connected to the inverting input of the opamp. If the offset voltage of the opamp is zero C_1 is fully discharged since C_1 is connected between ground and virtual ground. C_2 acquires a charge of V_iC_1. A unity-gain buffer SC integrator is shown in Fig. 1.1 (b). This circuit operates as follows. As in the conventional integrator the input voltage is sampled by a switch during clock phase ϕ_1 and charge is stored on C_1. During clock phase ϕ_2, C_1 is switched across the unity-gain buffer. If the offset voltage of the buffer is zero C_1 is fully discharged and C_2 acquires a charge of $-V_iC_1$. It will be shown in Chapter 3 that the discrete time transfer functions of these two integrators are equivalent. Using a simple buffer as the active element of the integrator will allow high-speed operation, reduce power consumption, ease design complexity and reduce die area. This design approach was first proposed in [1].

This thesis is organized as follows. Chapter 2 focuses on the design of unity-gain buffers. A comparison is made between various buffer architectures to determine their suitability for use in unity-gain buffer (UGB) SC filters. Chapter 2 includes analysis of two of the more promising unity-gain buffers. In Chapter 3 the discrete-time transfer function of a UGB SC integrator is derived, a methodology for synthesizing UGB SC ladder filters is presented and design equations for a biquad filter section are shown. Chapter 4 discusses the effects of parasitic capacitances on filter performance. Chapter 5 presents equations describing the effects of non-unity buffer gain and finite buffer bandwidth on UGB SC integrators. Chapter 6 details the implementation of a biquad filter section. Chapter 7 compares prior work to that presented here and concludes the thesis.

2. UNITY-GAIN BUFFER DESIGN

The central component in UGB SC filters is the unity-gain buffer itself. Many architectures for voltage buffers have been reported in the literature [9]- [14]. The ideal buffer for use in UGB SC filters will have unity DC gain, very large bandwidth, very high linearity, no offset voltage, high slew rate, low output impedance and low power consumption. Buffers that are simple, single-stage open-loop structures are good candidates. We will now examine such buffers.

2.1. Voltage Buffer Comparison

NMOS and PMOS source-followers (SF), a differential pair in unity-gain configuration and a novel low-output impedance buffer [8] have been characterized to determine their applicability to UGB SC filters. The circuit schematics are shown in Fig. 2.1 (a)-(d) and are annotated with device dimensions, power supply voltages and bias currents used in simulations. The primary metrics used to characterize the buffers are dc gain, bandwidth and offset voltage. Hspice simulations were performed with realistic 0.5μm CMOS models. The results are summarized in Table 2.1.

The simulation results in Table 2.1 show that the PMOS SF has the most desirable characteristics. It is a very simple circuit and by tying the source and body together the body effect is eliminated. This results in the DC gain being much closer to unity. While the PMOS SF suffers from large offset voltage (|Vgs|) and relatively low bandwidth (due to the lower mobility of holes) the other buffers exhibit poor gain. Eliminating the body effect in the PMOS SF by tying the source to the n-well reduces the PMOS SF bandwidth. This is due to the additional capacitive load introduced by the n-well to substrate depletion region and source/drain diffusion
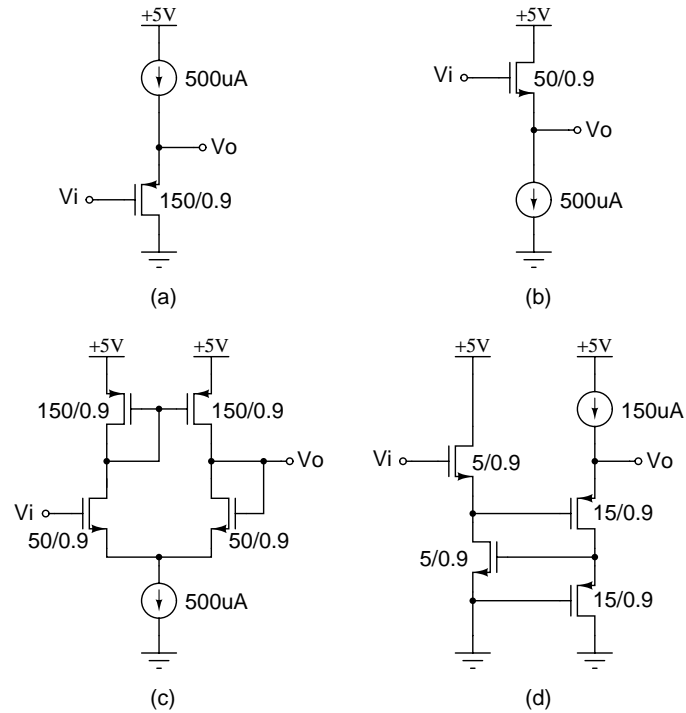
Figure 2.1. Voltage buffers: (a) PMOS source-follower, (b) NMOS source-follower, (c) differential pair, (d) high-transconductance (high-gm) buffer.

Metric	P. SF	P. SF (Vsb=0)	N. SF	Diff. Pair	High-gm
DC gain (V/V)	0.87	0.98	0.85	0.96	0.59
f-3dB, 2pF load (MHz)	221	202	266	176	148
Offset voltage (V)	1.3	1.2	1.2	0.07	0

Table 2.1. Voltage buffer comparison.

depeletion regions. Even with the elimination of the body effect the DC gain of the PMOS SF is still sufficiently below unity to degrade the accuracy of a filter and the large offset voltage will require compensation circuitry to eliminate its effect on the filter response.

The remaining sections of this chapter introduce techniques which address the PMOS SF gain and bandwidth limitations. The resulting circuit modifications lead to a new voltage buffer, the "drain-follower", which exhibits near-unity dc gain, high bandwidth and low offset voltage.

2.2. Cascoded PMOS Source-Follower

2.2.1. Gain Improvement
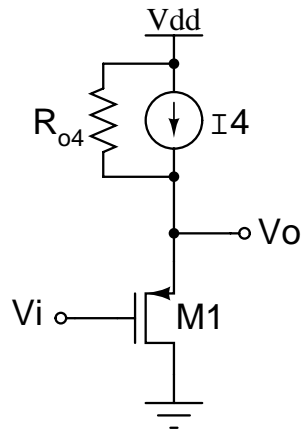
Figure 2.2. The PMOS source-follower.

A PMOS SF is shown in Fig. 2.2. The small-signal DC gain, zeros and poles of this circuit are

$$\frac{V_0(0)}{V_i(0)} = \frac{g_{m1}(R_{o1}||R_{o4})}{g_{m1}(R_{o1}||R_{o4}) + 1} \tag{2.1}$$

$$z_1 = \frac{-g_{m1}}{C_{gs1}} \tag{2.2}$$

$$p_1 = \frac{-g_{m1}}{C_{gs1} + C_L} \tag{2.3}$$

where R_{o1} is the incremental output resistance of M_1, R_{o4} is the incremental output resistance of the current source I_4, g_{m1} is the small-signal transconductance of M_1, C_{gs1} is the gate-to-source capacitance of M_1 and C_L is the load capacitance at the output, V_0. The body effect has been neglected in this analysis. If R_{o4} is very large then the products in the numerator and denominator of Eq. 2.1 become gm_1R_{o1}. For typical CMOS processes this product is approximately 30dB which leads to a dc gain of 0.97 V/V. The simulation results in Table 2.1 verify this approximation. It is interesting to note that this is equivalent to a unity-gain opamp with an open-loop dc gain of 32dB. The DC gain can be increased by increasing the output resistance of the input device. This can easily be done by cascoding the input device as explained below.

Fig. 2.3 shows a cascoded PMOS SF. The small-signal DC gain, zeros and poles of this circuit are

$$\frac{V_0(0)}{V_i(0)} = \frac{(1 + g_{m2}R_{o2})g_{m1}(R_{o1}||R_{o4})}{(1 + g_{m2}R_{o2})g_{m1}(R_{o1}||R_{o4}) + 1 + g_{m2}R_{o1}R_{o2}\left[\frac{1}{R_{o4}} + \frac{1}{R_{o5}}\right]} \tag{2.4}$$

$$z_1 = \frac{-g_{m1}}{C_{gs1}} \tag{2.5}$$

$$z_2 = \frac{-g_{m2}}{C_{gs2}} \tag{2.6}$$

$$p_1 = \frac{-g_{m1}}{C_{gs1} + C_L} \tag{2.7}$$

$$p_2 = \frac{-g_{m2}}{C_{gs2}} \tag{2.8}$$

where R_{o1} is the incremental output resistance of M_1, R_{o2} is the incremental output resistance of M_2, R_{o4} is the incremental output resistance of the current source I_4, R_{o5} is the incremental output resistance of the current source I_5, g_{m1} is the small-signal transconductance of M_1, g_{m2} is the small-signal transconductance of M_2, C_{gs1} is the gate-to-source capacitance of M_1, C_{gs2} is the gate-to-source capacitance of M_2 and C_L is the load capacitance at the output, V_0. Again, the body effect has been neglected.

In Fig. 2.3 transistor M_1 is cascoded by M_2. Small-signal analysis shows that cascoding has produced a factor of $(1+g_{m2}R_{o2})$ in the numerator and denominator of the PMOS SF dc transfer function (Eq. 2.1). This produces a $(g_m R_o)^2$ term in both the numerator and denominator, bringing the buffer gain much closer to unity. Assuming R_{o4} and R_{o5} are very large a dc gain of 0.999 should be achievable in a typical CMOS process. This is equivalent to a unity-gain opamp with an open-loop dc gain of 60dB. Cascoding has effectively boosted the output resistance of M_1 from R_{o1} to $R_{o1}(1+g_{m2}R_{o2})$.

Cascoding introduces additional zeros and poles, however the dominant pole remains the same as that of the PMOS SF without cascoding. Device dimensions and bias currents can be selected to ensure that the non-dominant pole and zeros do not have an adverse effect on the cascoded PMOS SF bandwidth.
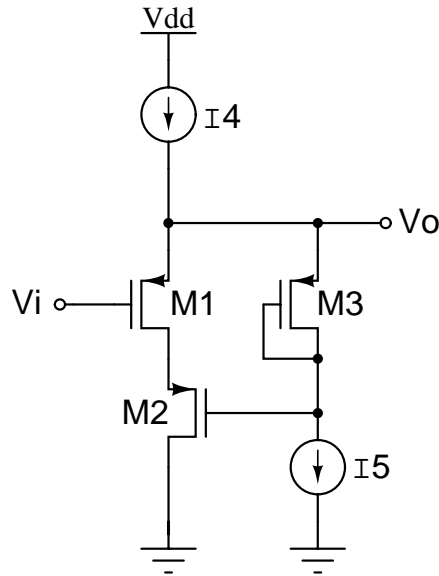
Figure 2.3. Cascoded PMOS source-follower.

2.2.2. Linearity and Slew Rate Improvement

The cascode feedback circuit in Fig. 2.3 provides additional benefits. By maintaining a constant drain-source voltage across transistor M_1 non-linear distortion due to channel length modulation is reduced, improving the PMOS SF linearity [11] [13]. The slew rate of the PMOS SF can be improved with dynamic biasing [16]. Fig. 2.4 shows a simple scheme for dynamically adjusting the source-follower bias current. With M_2 cascoding M_1 we can use the drain voltage of M_1 to adjust the gate-to-source voltage of M_6. When the input voltage moves in a positive direction, the drain of M_1 follows, increasing the gate-to-source voltage of M_6. This produces an increase in the bias current of M_6 which is mirrored to M_4 by M_5 and increases the bias current of the PMOS SF. In the PMOS SF the slew rate in the positive di-

rection is proportional to the bias current. Input signals going in a negative direction produce a decrease in the bias current of the PMOS SF by M_4 through the same mechanism and allows the driver transistor to pull down the output faster. One drawback to this scheme is the increased power dissipation when the input signal is maximum.

We have addressed the gain limitations of the PMOS SF and introduced techniques to improve linearity and slew rate. Next we examine the PMOS SF bandwidth issues.
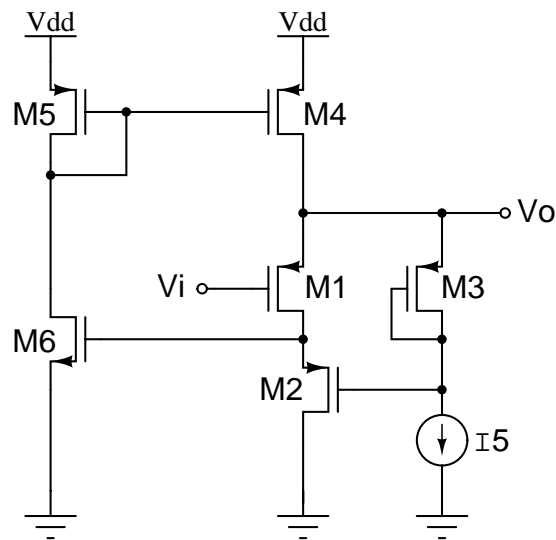
Figure 2.4. Cascoded PMOS source-follower with dynamic biasing.

2.3. The PMOS Source-Follower with N-Well Buffer

As discussed in previous sections the body effect can be eliminated in the PMOS SF by tying the source to the n-well in a standard CMOS process, but there is an accompanying reduction in bandwidth. We will now examine the PMOS SF small-signal model to determine the cause of this bandwidth reduction and present a technique for improving bandwidth in the PMOS SF when source and body terminals are shorted.

The small-signal model for a PMOS SF is shown in Fig. 2.5 with the body and drain terminal at small-signal ground. In this configuration C_{db} can be removed from the model since its terminals are shorted. We see that the current source controlled by V_{bs} will be active and so the body effect will be present. C_{sb} will be in parallel with the load at the output but will not have a large affect on performance since it is several orders of magnitude smaller than typical loads. C_{gb} will have no affect on the PMOS SF performance assuming the input signal source has sufficient drive capability.

Fig. 2.6 shows the PMOS SF small-signal model with source and body shorted. Since the body terminal is no longer at analog ground we must include C_{n-well}, the depletion capacitance associated with the pn junction formed between the n-well and substrate. Here the body effect and C_{sb} are eliminated but the load at the output has increased. Now C_{db} and C_{n-well} are in parallel with the load. The combination of C_{db} and C_{n-well} can be a large percentage of the load and will reduce the PMOS SF bandwidth. The bandwidth reduction becomes more severe for larger device sizes as C_{db} and C_{n-well} are proportional to MOS channel width and length. The parallel combination of C_{gb} and C_{gs} also contributes to bandwidth reduction since the effective C_{gs} is larger.
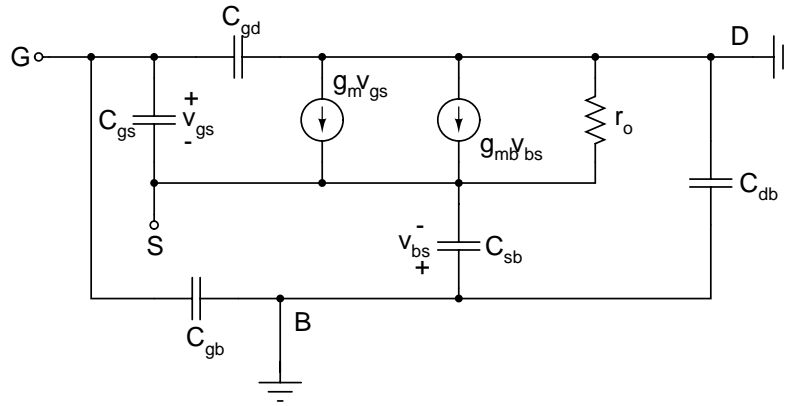
Figure 2.5. Small-signal model of the PMOS source-follower.
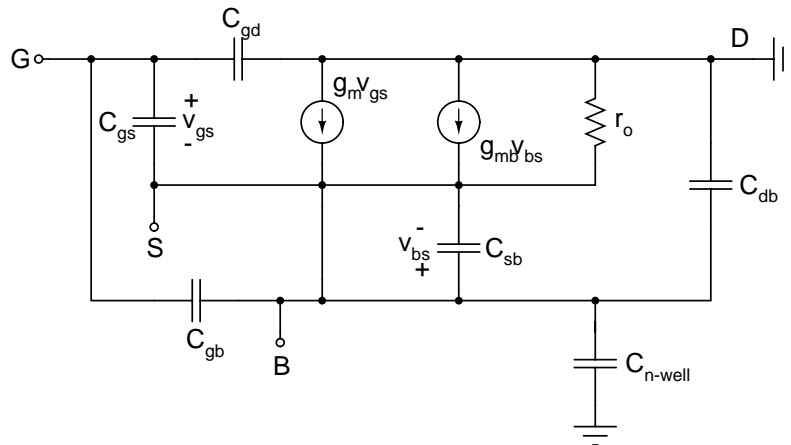
Figure 2.6. Small-signal model of the PMOS source-follower with source and body shorted.

A method for eliminating the body effect without a significant reduction in bandwidth is shown in Fig. 2.7. A buffer is connected between the source and body (n-well) terminals of the PMOS SF. The small-signal model of the PMOS SF with n-well buffer is shown in Fig. 2.8. If the bandwidth of the n-well buffer is sufficient we see that V_{bs} will be constant and the body effect is eliminated. If the input capacitance of the n-well buffer is small only C_{gs} and the load capacitance at the source determine the PMOS SF bandwidth since C_{sb}, C_{db} and C_{n-well} are no longer in parallel with the load and C_{gb} is no longer in parallel with C_{gs}.
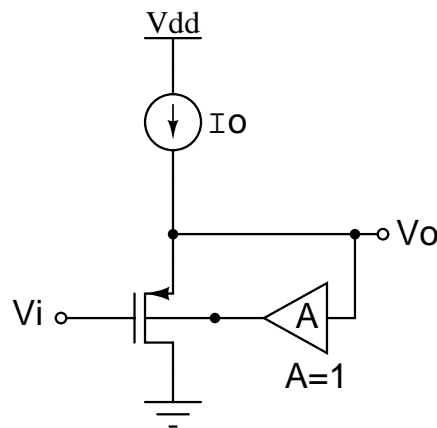
Figure 2.7. PMOS source-follower with n-well buffer.

A good candidate for an n-well buffer is another PMOS SF. A PMOS SF is a very simple circuit and will ensure that the source diffusion to n-well junction in the main PMOS SF does not become forward biased. In order to reduce the loading effect of the n-well buffer input capacitance at the PMOS SF output, the PMOS SF and the n-well buffer can both be driven by the input signal as shown in Fig. 2.9.
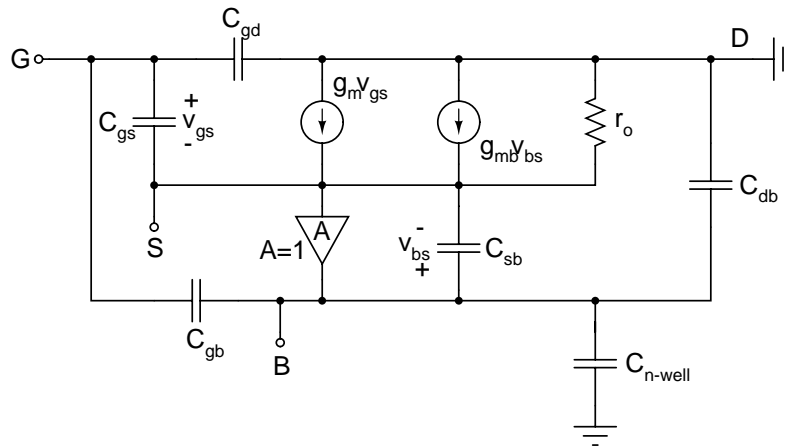
Figure 2.8. Small-signal model of the PMOS source-follower with n-well buffer.

We have addressed the PMOS SF bandwidth degradation caused by shorting the source and body terminals of the input device. While the performance of a cascoded PMOS SF incorporating an n-well buffer may be suitable for high-speed UGB SC filters, any filter which uses this PMOS SF will require additional offset voltage compensation circuitry. The following section describes a slight modification in the circuit of Fig. 2.3 which addresses this issue.

2.4. The Drain-Follower

Using the same circuit topology as the cascoded PMOS SF but taking the output at the drain of M_1, offset voltage can be minimized. The circuit is redrawn in Fig. 2.10 with NMOS devices. Neglecting channel-length modulation the dc output voltage is

$$V_o = V_i - V_{gs1} + V_{gs2} + V_{gs3} - V_{gs4} \qquad (2.9)$$
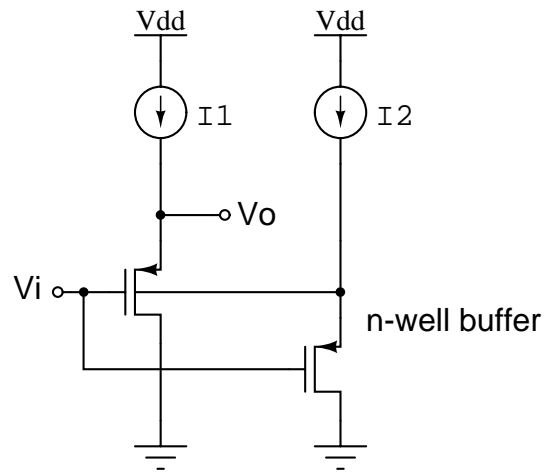
Figure 2.9. Biasing the n-well buffer.
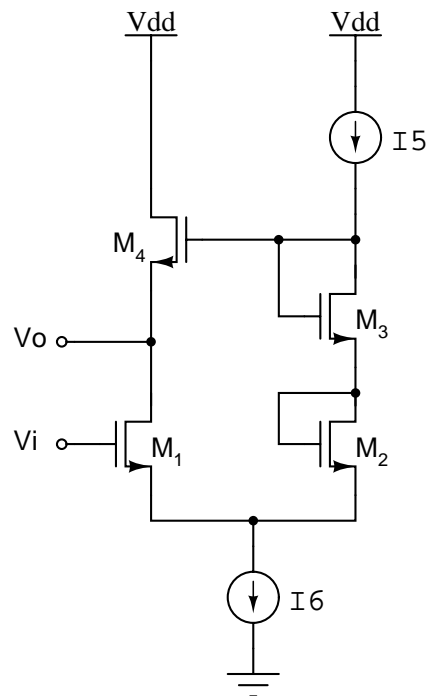
Figure 2.10. NMOS drain-follower.

For

$$V_{gs1} = V_{gs2} = V_{gs3} = V_{gs4} \tag{2.10}$$

the dc output voltage becomes

$$V_o = V_i \tag{2.11}$$

With proper device sizing and bias currents the dc output voltage can be set very close to the dc input voltage.

Another benefit of this circuit is the inherent body effect cancellation. Proper device sizing and biasing cause V_{gs1} and V_{gs2} as well as V_{gs3} and V_{gs4} to experience similar changes in their magnitude due to body effect. Without body effect there is no need to short the source and body terminals of the devices in the drain-follower and there will be no bandwidth degradation as discussed in section 2.2. With no body effect, NMOS devices, with relatively high carrier mobility, can be used in the drain-follower to maximize bandwidth and minimize power consumption and area.

The small-signal DC gain, zeros and poles of this circuit are

$$\frac{V_0(0)}{V_i(0)} = \frac{g_{m1} R_{o1} g_{m2} R_{o2}}{g_{m1} R_{o1}(1 + g_{m2} R_{o2}) + 1 + g_{m2} R_{o1} R_{o2} \left[\frac{1}{R_{o5}} + \frac{1}{R_{o6}}\right]} \tag{2.12}$$

$$z_1 = \frac{(-g_{m1} g_{m2} C_{gs1} C_{gs2})^{1/2}}{C_{gs1} C_{gs2}} \tag{2.13}$$

$$z_2 = \frac{-(-g_{m1} g_{m2} C_{gs1} C_{gs2})^{1/2}}{C_{gs1} C_{gs2}} \tag{2.14}$$

$$p_1 = \frac{-g_{m2}}{C_{gs2} + C_L} \tag{2.15}$$

$$p_2 = \frac{-g_{m1}}{C_{gs1}} \hspace{4cm} (2.16)$$

where R_{o1} is the incremental output resistance of M_1, R_{o2} is the incremental output resistance of M_2, R_{o5} is the incremental output resistance of the current source I_5, R_{o6} is the incremental output resistance of the current source I_6, g_{m1} is the small-signal transconductance of M_1, g_{m2} is the small-signal transconductance of M_2, C_{gs1} is the gate-to-source capacitance of M_1, C_{gs2} is the gate-to-source capacitance of M_2 and C_L is the load capacitance at the output, V_0. The body effect has been neglected in this analysis.

Eq. 2.12-2.16 for the drain-follower and Eq. 2.4-2.8 for the cascoded PMOS SF are very similar and it is expected that the two circuits will have nearly identical gain and bandwidth.

3. UNITY-GAIN BUFFER SWITCHED CAPACITOR FILTER SYNTHESIS

This chapter presents circuits used to synthesize UGB SC filters. First, the discrete-time transfer function of the basic ingredient of UGB SC filters, the UGB SC integrator, is derived. Then the design of UGB SC ladder filters is illustrated with an example followed by the presentation of a biquad filter section. The derivation of the discrete-time transfer functions presented in this chapter follows the methodology described in [2] and [3].

3.1. Unity-Gain Buffer SC Integrators

SC integrators are important building blocks in many SC circuits such as filters and oversampling data converters. In this section it will be shown that a UGB SC integrator is equivalent to a conventional SC integrator. A conventional SC integrator is shown in Fig. 3.1 (a). Its discrete-time transfer function can be expressed as [3]

$$H_{conv}(z) = \frac{V_o(z)}{V_i(z)} = \frac{\frac{-C_1}{C_2}z^{-1}}{1 - z^{-1}} \tag{3.1}$$

A UGB SC integrator is shown in Fig. 3.1 (b). A diagram of the clock signals used to control the switches in Fig. 3.1 (b) is shown in Fig. 3.2. In order to derive the discrete-time transfer function of the UGB SC integrator we refer to the timing diagram and assume that V_i and V_o change only during ϕ_2.

At time $t_{n-1/2}$ C_1 acquires a charge of

$$q_1(t_{n-1/2}) = C_1 V_i(t_{n-1/2}) \tag{3.2}$$

and the charge on C_2 is
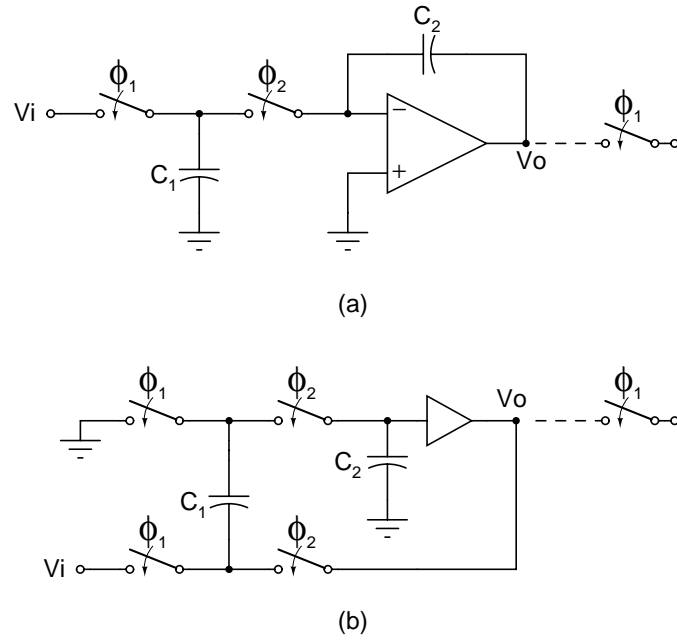
Figure 3.1. SC integrators: (a) Conventional SC integrator; (b) Unity-gain buffer SC integrator.
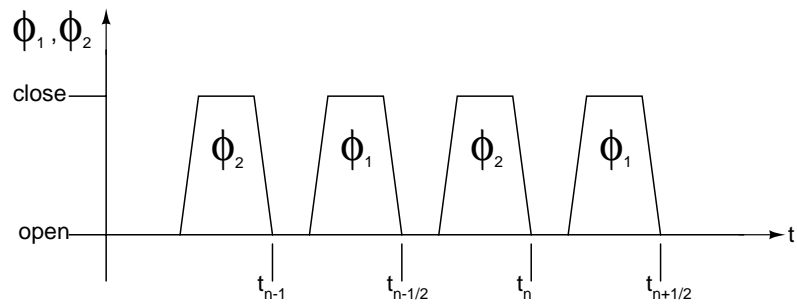
Figure 3.2. Timing diagram.

$$q_2(t_{n-1/2}) = C_2 V_o(t_{n-1/2}) \tag{3.3}$$

Since V_i and V_o change during ϕ_2 only the values of these voltage at $t_{n-1/2}$ are the same at t_{n-1} and Eqs. 3.2 and 3.3 become

$$q_1(t_{n-1}) = C_1 V_i(t_{n-1}) \tag{3.4}$$

$$q_2(t_{n-1}) = C_2 V_o(t_{n-1}) \tag{3.5}$$

At time t_n C_1 is discharged by the buffer and this charge is transferred to C_2. The charge on the capacitors at time t_n is

$$q_1(t_n) = 0 \tag{3.6}$$

$$q_2(t_n) = C_2 V_o(t_n) \tag{3.7}$$

The charge difference on the capacitors from t_{n-1} to t_n is

$$\Delta q_1 = q_1(t_n) - q_1(t_{n-1}) = 0 - C_1 V_i(t_{n-1}) = -C_1 V_i(t_{n-1}) \tag{3.8}$$

$$\Delta q_2 = q_2(t_n) - q_2(t_{n-1}) = C_2 V_o(t_n) - C_2 V_o(t_{n-1}) \tag{3.9}$$

Summing the charge changes at the input of the buffer, taking z-transforms and solving for $V_o(z)/V_i(z)$ as shown in Eq. 3.10-3.14 produce the desired result.

$$\Delta q_2 - \Delta q_1 = 0 \tag{3.10}$$

$$\Delta q_2 = \Delta q_1 \tag{3.11}$$

$$C_2 V_o(t_n) - C_2 V_o(t_{n-1}) = -C_1 V_i(t_{n-1}) \tag{3.12}$$

$$C_2 V_o - C_2 V_o(z^{-1}) = -C_1 V_i z^{-1} \tag{3.13}$$

$$H_{ugb}(z) = \frac{V_o(z)}{V_i(z)} = \frac{\frac{-C_1}{C_2} z^{-1}}{1 - z^{-1}} \tag{3.14}$$

Eqs. 3.1 and 3.14 are identical. For a detailed discussion on the performance of SC integrators in general see [3].

3.2. Unity-Gain Buffer SC Ladder Filters

When high order, very selective filters are required, the most widely used technique is to simulate the response of a doubly terminated reactance two-port (LCR ladder) [3]. Very selective filters have high-Q poles and the low-sensitivity of the two-port helps maintain the accuracy of the filter response in the presence of circuit non-idealities. The design process will be illustrated with an example of a third-order low pass UGB SC filter.

The design will be performed in the following steps:

1. Choose LCR prototype to meet filter specification.

2. Modify LCR circuit topology to facilitate application of bilinear transform.

3. Derive state equations for LCR prototype.

4. Transform state equations to z-domain using bilinear transform.

5. Realize z-domain state equations with UGB SC integrators.

3.2.1. LCR Prototype

From [18] an LCR prototype is selected and shown in Fig. 3.3 along with filter specifications and normalized element values.

$C_a = 1.0512$
$C_b = 0.2019$

CO3 20 $\theta = 30°$

$A_{min} = 25dB$ $A_p = 13.9dB$

$C_c = 1.0512$

$R_{dB} < 0.2dB$ $f_s = 2f_p$

$L_2 = 0.9612$
$R_s = R_L = 1$

Figure 3.3. LCR prototype, filter specifications and element values.

3.2.2. Modified LCR Prototype

To facilitate the application of the bilinear transform we split C_b into the parallel combination of $-C_{L2}$ and C'_2 where C_{L2} is defined as

$$C_{L2} \equiv \frac{T^2}{4L_2} \tag{3.15}$$

where T is the sampling period of the SC filter. Using Norton's Theorem C'_2 is eliminated from the parallel branch in Fig. 3.3 and I_2 is redefined as the current

flowing into the tank. The modified LCR prototype is shown in Fig. 3.4 and the new capacitor values are

$$C_1' = C_a + C_b + \frac{T^2}{4L_2} \tag{3.16}$$

$$C_2' = C_b + \frac{T^2}{4L_2} \tag{3.17}$$

$$C_3' = C_b + C_c + \frac{T^2}{4L_2} \tag{3.18}$$
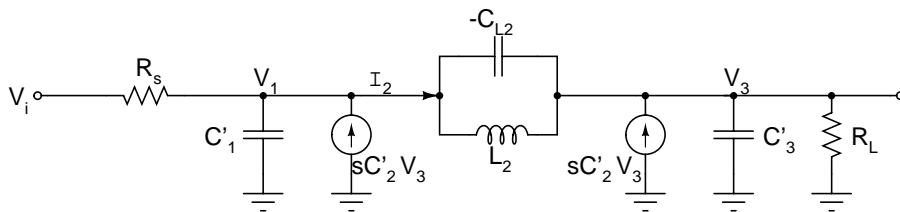
Figure 3.4. Modified LCR prototype.

3.2.3. S-Domain State Equations

We can derive the s-domain the state variables of the modified LCR prototype as

$$V_1(s) = \frac{1}{C_1'}\left[\frac{V_i - V_1}{sR_s} + C_2'V_3 - Q_2\right] \tag{3.19}$$

$$Q_2(s) = (V_1 - V_3)\left[C_{L2} + \frac{1}{s^2L_2}\right] \tag{3.20}$$

$$V_3(s) = \frac{1}{C_3'}\left[\frac{-V_3}{sR_s} + C_2'V_1 + Q_2\right] \tag{3.21}$$

Note that in the s-domain state variable I_2 can be conveniently expressed as charge.

3.2.4. S-to-Z Domain Transformation

The bilinear s-to-z transform will be used to map the s-domain state variables to the z-domain. The bilinear s-to-z transformation is defined as [3]

$$s \equiv \frac{2}{T}\frac{(z-1)}{(z+1)} \tag{3.22}$$

Substituting Eq. 3.22 into Eqs. 3.19-3.21 we have

$$V_1(z) = \frac{T}{2C_1'R_s}\left(\frac{z+1}{z-1}\right)V_i - V_1 + \frac{C_2'V_3}{C_1'} - \frac{Q_2}{C_1'} \tag{3.23}$$

$$Q_2(z) = \frac{T^2}{L_2}\frac{z^{-1}}{(1-z^{-1})}(V_1 - V_3) \tag{3.24}$$

$$V_3(z) = \frac{-T}{2C_3'R_L}\left(\frac{z+1}{z-1}\right)V_3 + \frac{C_2'V_3}{C_3'} + \frac{Q_2}{C_3'} \tag{3.25}$$

3.2.5. Realization of Z-Domain State Equations

In the following we choose the value of all sampling capacitors to be T/R where R is the source or load resistance of the prototype filter. Fig. 3.5 shows a unity-gain buffer filter section that realizes Eq. 3.23. Its discrete-time transfer function is

$$V_1(z) = \frac{C_s}{C_x}\left(\frac{z+1}{z-1}\right)(V_i - V_1) + \frac{C_d V_3}{C_x} - \frac{C_3 V_2 z^{-1}}{C_x(1 - z^{-1})} \tag{3.26}$$

$$C_x = C_1 + C_2 + C_d \tag{3.27}$$

The capacitor values in terms of the original LCR prototype elements can be found by matching the coefficients of Eqs. 3.23 and 3.26 resulting in

$$C_1 = \frac{T}{R_s} \tag{3.28}$$

$$C_2 = C_a - \frac{T}{R_s} \tag{3.29}$$

$$C_3 = \frac{T}{R_s} \tag{3.30}$$

$$C_d = C_b + \frac{T^2}{4L_2} \tag{3.31}$$

$$C_s = \frac{T}{2R_s} \tag{3.32}$$

Fig. 3.6 shows a unity-gain buffer filter section that realizes Eq. 3.24. Its discrete-time transfer function is

$$Q_2(z) = \frac{C_3}{C_1}\frac{z^{-1}}{1 - z^{-1}}(V_1 - V_3) \tag{3.33}$$

The capacitor values in terms of the original LCR prototype elements can be found by matching the coefficients of Eqs. 3.24 and 3.33 resulting in

$$C_1 = \frac{L_2}{R_s^2} \tag{3.34}$$

$$C_3 = \frac{T}{R_s} \tag{3.35}$$
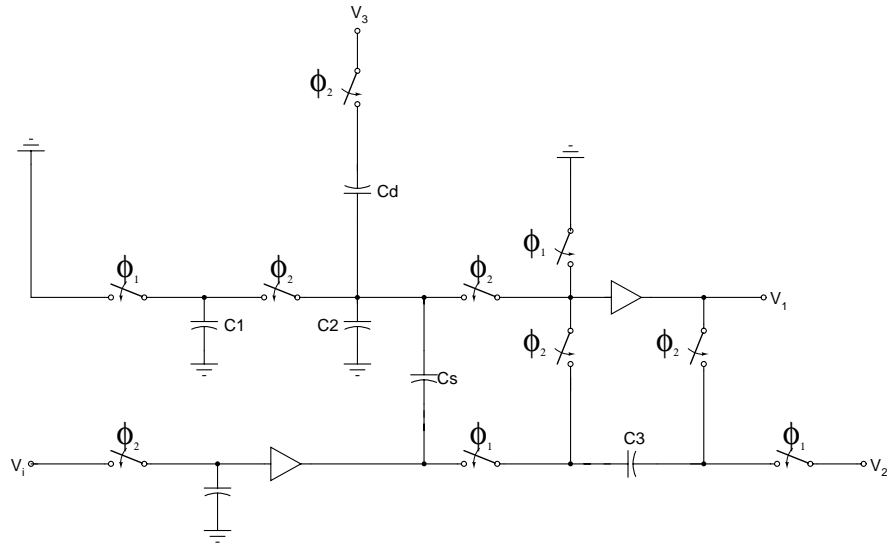
Figure 3.5. Unity-gain buffer filter section realizing $V_1(z)$.
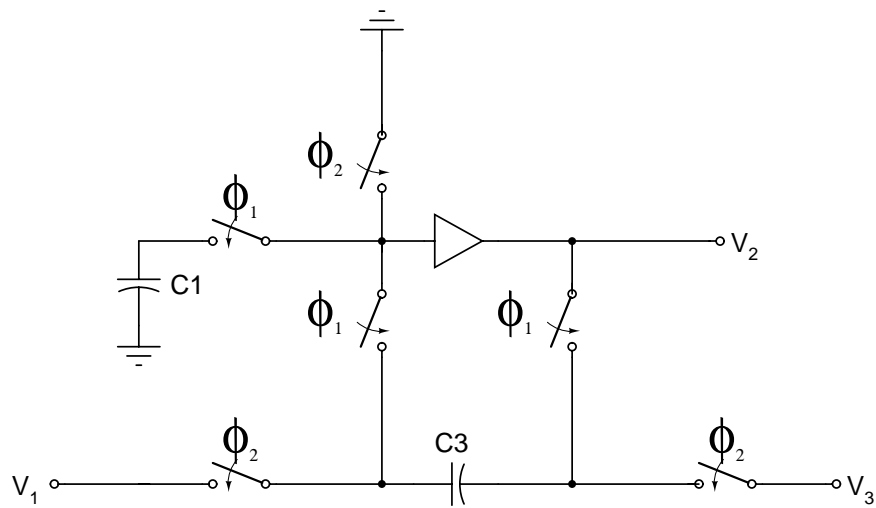
Figure 3.6. Unity-gain buffer filter section realizing $Q_2(z)$.

Fig. 3.7 shows a unity-gain buffer filter section that realizes Eq. 3.25. Its discrete-time transfer function is

$$V_3(z) = -\frac{C_1}{2C_x}\left(\frac{z+1}{z-1}\right)V_3 + \frac{C_5 V_3}{C_x} + \frac{C_3 V_2 z^{-1}}{C_x(1-z^{-1})} \tag{3.36}$$

$$C_x = \frac{C_1}{2} + C_2 + C_5 \tag{3.37}$$

The capacitor values in terms of the original LCR prototype elements can be found by matching the coefficients of Eqs. 3.25 and 3.36 resulting in

$$C_1 = \frac{T}{R_L} \tag{3.38}$$

$$C_2 = C_c - \frac{T}{2R_L} \tag{3.39}$$

$$C_3 = \frac{T}{R_L} \tag{3.40}$$

$$C_5 = C_b + \frac{T^2}{4L_2} \tag{3.41}$$

3.2.6. Circuit Schematic and Simulation Results

Fig. 3.8 shows the complete third-order ladder filter. The circuit was simulated with Switcap using ten times oversampling. The results are plotted in Fig. 3.9 which shows that the filter meets all of the design specifications.

3.3. Unity-Gain Buffer SC Biquad

Fig. 3.10 shows the circuit schematic for a UGB biquad suitable for realizing low-Q transfer functions. The transfer function for this circuit can be found in
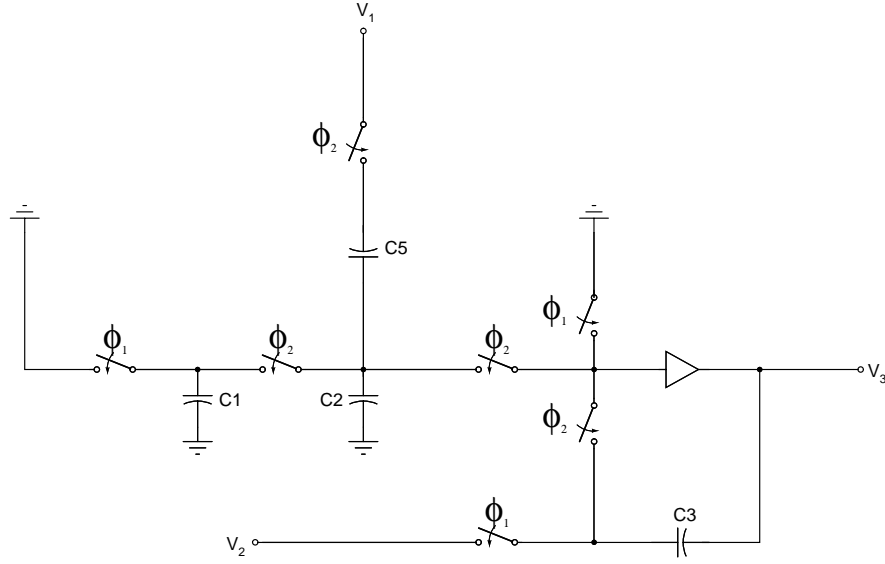
Figure 3.7. Unity-gain buffer filter section realizing $V_3(z)$.

the same manner as the transfer function of the UGB SC integrator. The transfer function is

$$H_{BIQ}(z) = \frac{C_c z^2 + (C_d - 2C_c)z + C_c - C_d + \frac{C_a C_e}{C_{i1}}}{(C_{i1} + C_c)z^2 + (C_e - 2C_{i1} - 2C_c)z + C_{i1} + C_c - C_e + \frac{C_e C_b}{C_{i1}}} \quad (3.42)$$

A discrete-time biquad transfer function has the form

$$H(z) = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0} \quad (3.43)$$

By matching the coefficients of Eqs. 3.42 and 3.43 the capacitor values for the circuit in Fig. 3.10 can be found as

$$C_a = \frac{(a_2 + a_1 + a_0)(b_2 - a_2)}{b_1 + 2b_2} \quad (3.44)$$

$$C_b = \frac{(b_2 + b_1 + b_0)(b_2 - a_2)}{b_1 + 2b_2} \quad (3.45)$$
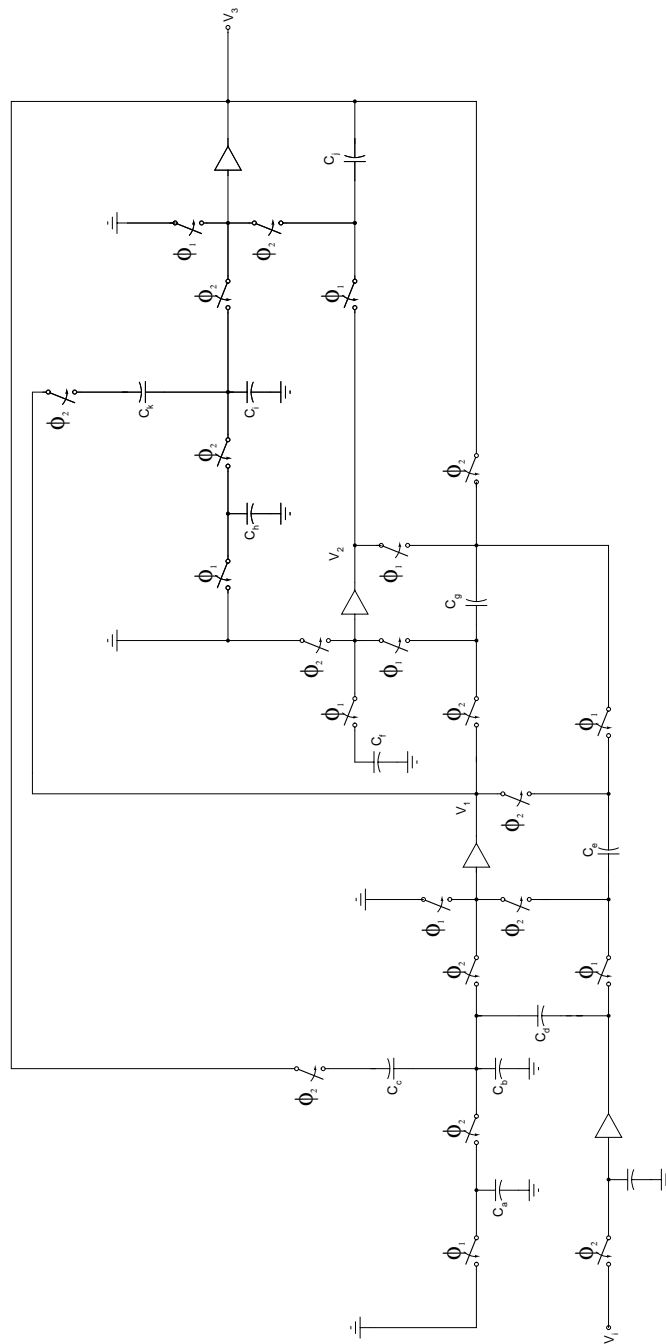
Figure 3.8. Third-order unity-gain buffer SC ladder filter.
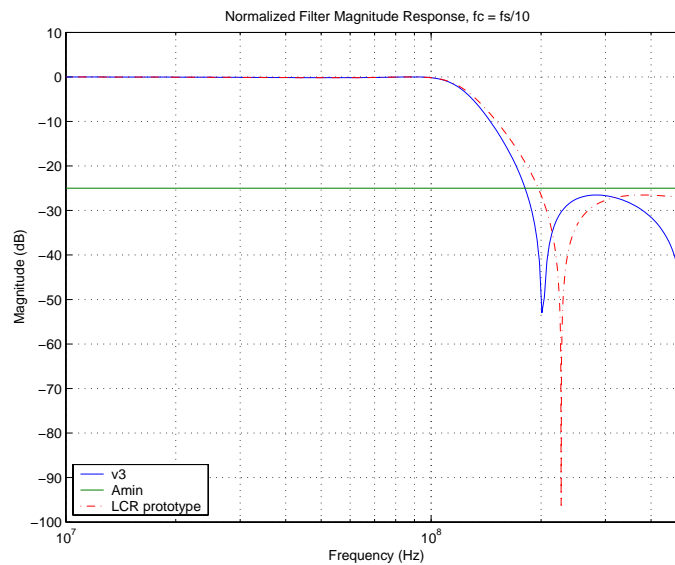
Figure 3.9. Simulation results for the third-order unity-gain buffer SC ladder filter.

$$C_c = a_2 \tag{3.46}$$

$$C_d = a_1 + 2a_2 \tag{3.47}$$

$$C_e = C_{e1} = C_{e2} = b_1 + 2b_2 \tag{3.48}$$

$$C_{i1} = C_{i2} = \; = b_2 - a_2 \tag{3.49}$$

Eq. 3.44-3.49 can be used to design a biquad filter section which realizes the discrete-time transfer function of Eq. 3.43. Higher order filters can be realized by cascading several biquad filter sections.
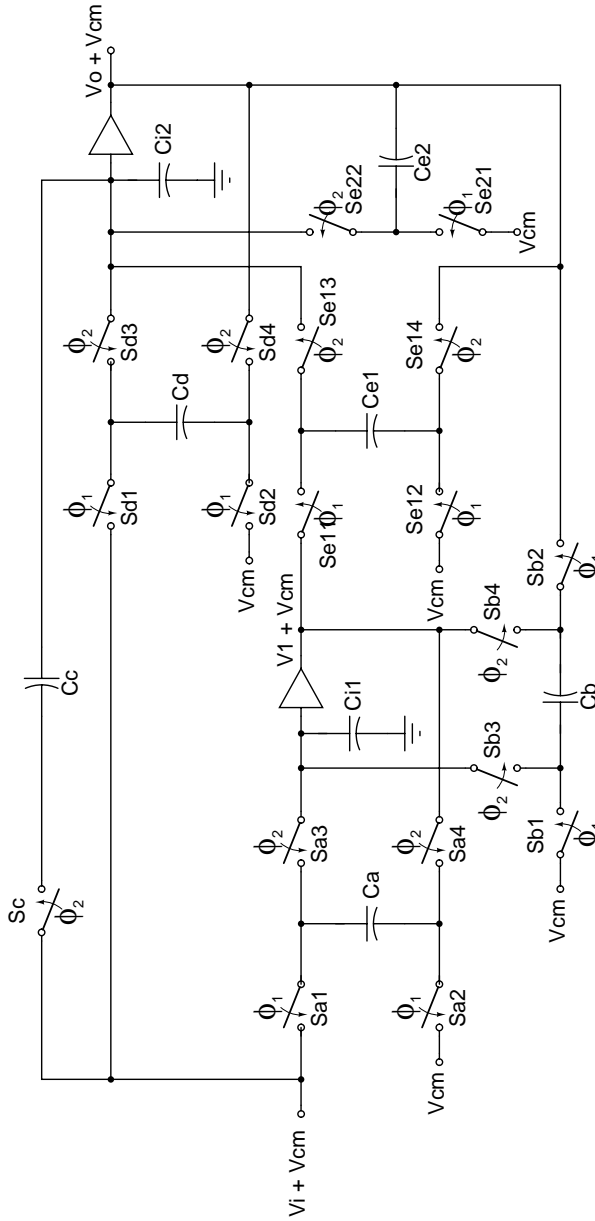
Figure 3.10. Low-Q unity-gain buffer biquad.

4. EFFECT OF PARASITIC CAPACITANCE ON UNITY-GAIN BUFFER SWITCHED-CAPACITOR FILTERS

One major drawback of UGB SC circuits is their sensitivity to stray capacitances between various circuit nodes and ground. These stray capacitances stem from transistor gates (buffer input), interconnect and source-drain diffusions of MOS switches. The effective buffer input capacitance for a typical buffer used in UGB SC circuits is $C_{gs}(1\text{-}A)$, where A is the gain of the buffer. For buffer gains close to unity this capacitance is negligible. The rest of this chapter deals with minimizing the effects of interconnect and source-drain diffusion capacitance.

Since damped integrators are used in both UGB SC ladder filters and UGB biquads, the analysis of a damped integrator with parasitic strays will give good insight as to how these strays effect filter accuracy and how to minimize the effect. Fig. 4.1 shows a damped UGB SC integrator with parasitic capacitors. C_{i2} is the interconnect capacitance between the top plate of C_a and ground, C_{j2} is the total diffusion capacitance between the top plate of C_a and ground, C_{i3} is the interconnect capacitance between the top plate of C_b and ground, C_{j3} is the total diffusion capacitance between the top plate of C_b and ground, C_{i7} is the interconnect capacitance between the top plate of C_f and ground and C_{j8} is the total diffusion capacitance between the top plate of C_f and ground.

The discrete-time transfer function of the circuit assuming a buffer gain of A is

$$H(z) = \frac{(C_a + C_{i2} + C_{j2})A}{(C_b + C_x + (C_a + C_f)(1 - A))z - C_b + C_f A - C_{i3} - C_{j3}} \qquad (4.1)$$

where

$$C_x = C_{i2} + C_{j2} + C_{i3} + C_{j3} + C_{i7} + C_{j8} \qquad (4.2)$$
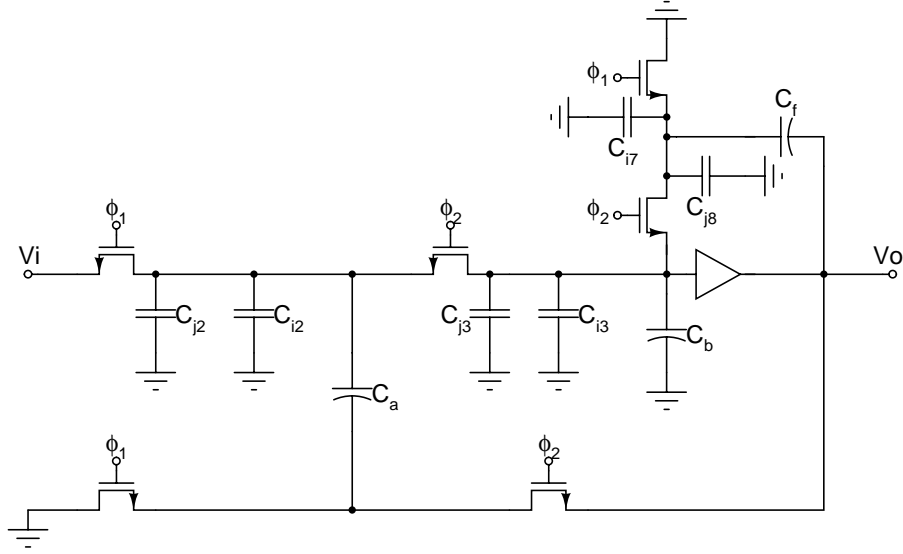
Figure 4.1. Damped unity-gain buffer SC integrator.

The magnitude response for $C_a = C_f = 1\text{pF}$, $C_b = 3\text{pF}$ and all stray capacitance equal to zero is shown in Fig. 4.2. The magnitude response for all interconnect capacitors equal to 1fF, $C_{j2} = 3\text{fF}$, and $C_{j3} = C_{j8} = 10\text{fF}$ is shown in Fig. 4.3 where the effects of these stray capacitors are clear.

From Eq. 4.1 we find the dc gain and pole location of the damped integrator to be

$$H(z)_{z=1,A=1} = \frac{C_a + C_{i2} + C_{j2}}{C_f + C_{i2} + C_{j2} + C_{i7} + C_{j8}} \tag{4.3}$$

$$P_1 = \frac{C_b - C_f A + C_{i3} + C_{j3}}{C_b + (C_a + C_f)(1 - A) + C_x} \tag{4.4}$$

We can set Eq. 4.3 equal to the desired dc gain and solve for C_f (C_a) in terms of C_a (C_f) and the stray capacitance. Using this value for C_f (C_a) will eliminate the error in the filter response due to the strays. The pole location can be adjusted in
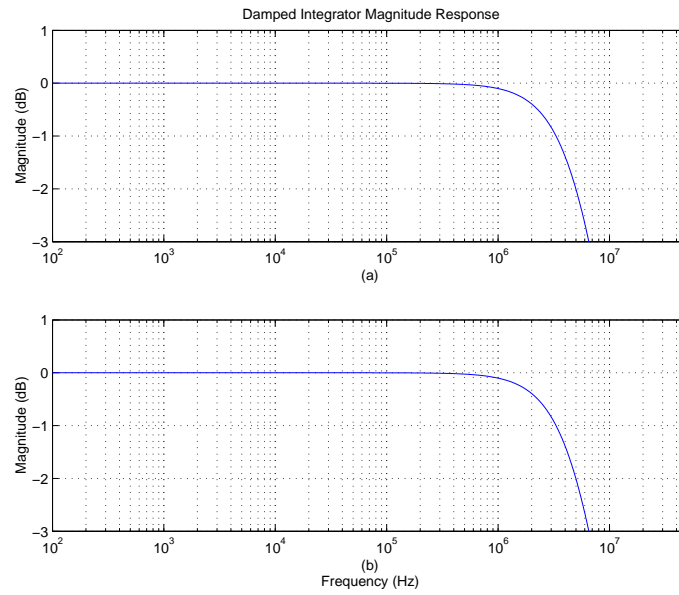
Figure 4.2. Damped UGB SC integrator magnitude response: (a) H(z), (b) simulation.
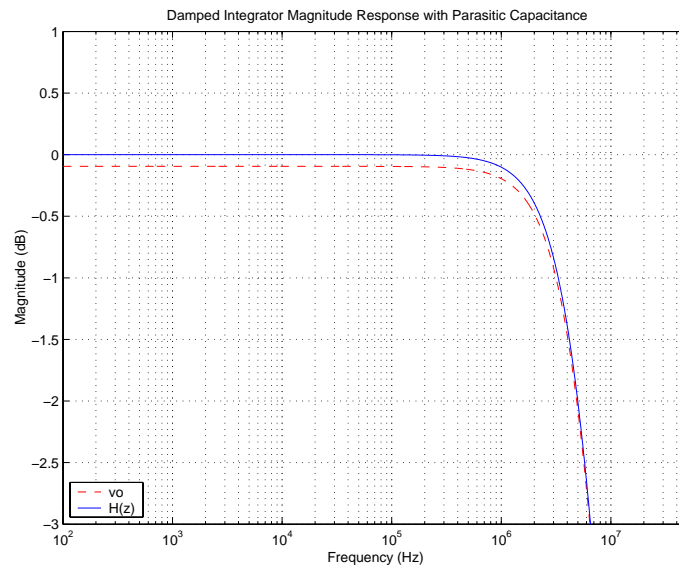
Figure 4.3. Damped UGB SC integrator magnitude response with parasitic capacitances.

the same manner. Fig. 4.4 shows the filter magnitude response after tuning where we see that the error due to the stays has been corrected. It should be noted that the diffusion capacitance associated with MOS switches is non-linear and can produce harmonic distortion which is not corrected by the method of tuning presented here.
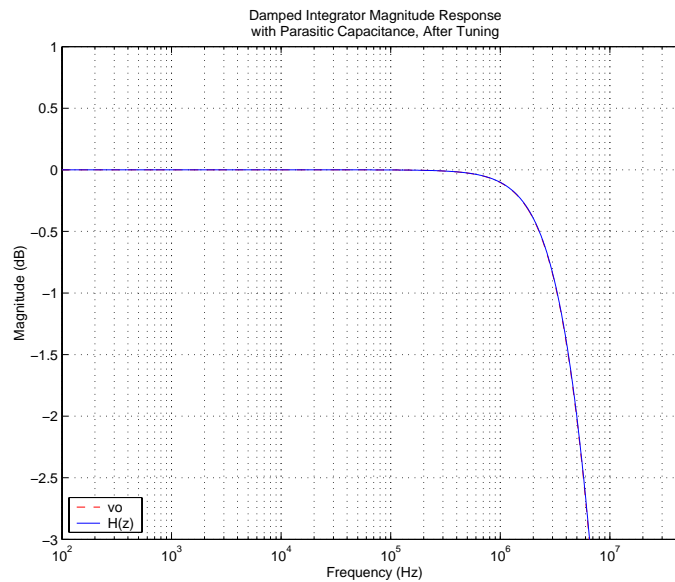
Figure 4.4. Damped UGB SC integrator magnitude response with parasitic capacitances, after tuning.

This method for reducing the effects of stray capacitance on the filter response depends heavily on how well we can estimate the value of the strays. Good process information is critical. Another method for reducing the stray interconnect capacitance is to run a poly or metal layer as a shield between the interconnect layer and the substrate [2]. The shield layer should be tied to the output of the buffer. The interconnect strays can be can be significantly reduced at the expense

of additional load on the buffer. In most cases the additional load on the buffer is negligible.

5. EFFECTS OF NON-UNITY BUFFER GAIN AND FINITE BUFFER BANDWIDTH IN UNITY-GAIN BUFFER SWITCHED-CAPACITOR FILTERS

In Chapter 3 the discrete-time transfer functions of several UGB SC filters were presented. In deriving these transfer functions it was assumed that the buffers had unity gain and infinite bandwidth. In practical circuits the non-unity gain and finite bandwidth of the buffer must be taken into account, especially for high-frequency operation where the buffer performance more dramatically effects the filter response. In this chapter we examine the effects of non-unity buffer gain and finite buffer bandwidth in UGB SC integrators. Understanding non-unity buffer gain and finite buffer bandwidth effects in UGB SC integrators gives insight to their effects in higher order filters.

5.1. Effects of Non-Unity Buffer Gain on UGB SC Integrators

The magnitude response of an inverting UGB SC integrator with buffer gain A_o can be derived as [2]

$$H(z) = \frac{-C_1}{C_2} \frac{z^{-1}}{(1 - z^{-1})/A_o + C_1/C_2(1/A_o - 1)} \tag{5.1}$$

For

$$z = e^{j\omega T} = cos(\omega T) + jsin(\omega T) \tag{5.2}$$

Eq. 5.8 becomes

$$H(\omega) = \frac{-C_1}{C_2} \frac{A_o e^{-j\omega T/2}}{2jsin(\omega T/2)\left[1 + \frac{C_1}{2C_2}(1 - A_o) - j\frac{C_1(1-A_o)}{2C_2 tan(\omega T/2)}\right]} \tag{5.3}$$

The magnitude error is

$$m(\omega) = \frac{C_1}{2C_2}(A_o - 1) \tag{5.4}$$

The phase error is

$$\theta(\omega) = \frac{C_1(1 - A_o)}{2C_2 tan(\omega T/2)} \tag{5.5}$$

For buffer gains close to unity the magnitude and phase errors are negligible.

5.2. Effects of Finite Buffer Bandwidth on UGB SC Integrators

The magnitude response of an inverting UGB SC integrator with a buffer 3dB bandwidth of ω_p can be derived as [2]

$$H(z) = \frac{-C_1}{C_2} \frac{z^{-1}}{(1 - z^{-1})(1 + \frac{e^{-2K}z^{-1}}{1 - z^{-1}} + \frac{e^{-K}}{1 - z^{-1}})} \tag{5.6}$$

where

$$K = \frac{\omega_p T}{2} \tag{5.7}$$

For

$$z = e^{j\omega T} = cos(\omega T) + jsin(\omega T) \tag{5.8}$$

Eq. 5.6 becomes

$$H(\omega) = \frac{-C_1}{C_2} \frac{e^{-j\omega T/2}}{2jsin(\omega T/2)\left[1 + \frac{e^{-K}}{2} - e^{-2K} - j\frac{e^{-2K} + \frac{e^{-K}}{2}}{tan(\omega T/2)}\right]} \tag{5.9}$$

The magnitude error is

$$m(\omega) = \frac{e^{-K}}{2} \frac{1}{tan(\omega T/2)} \tag{5.10}$$

The phase error is

$$\theta(\omega) = \frac{e^{-K}}{2} \tag{5.11}$$

Eqs. 5.10 and 5.11 illustrate the need for buffers with very large bandwidth when high-speed operation is desired.

6. IMPLEMENTATION OF A UNITY-GAIN BUFFER SC BIQUAD FILTER

To demonstrate the unity-gain buffer SC circuit techniques presented in the preceding chapters a low-pass unity-gain buffer SC biquad filter has been implemented in 0.5μm CMOS technology provided by Cypress Microsystems. The goal of this implementation is to maximize the sampling frequency of the filter. This chapter details the design of the unity-gain buffer and the system level filter design. The clock generation circuit producing necessary clock phases for switching is described and layout issues are discussed.

6.1. Unity-Gain Buffer Design

The results of Chapter 5 show that high-frequency UGB SC filters require a voltage buffer with very high bandwidth and dc gain close to unity. In Chapter 2 several buffers were examined to determine their suitability for use in UGB SC filters. Because of its high bandwidth, near unity dc gain and low offset voltage, the drain-follower (DF) will be used as the active component in the biquad filter. Two versions of the DF were designed, an NMOS DF, shown in Fig. 6.1, and an NMOS-PMOS DF consisting of two DF operating in parallel shown in Fig. 6.2. Several design issues are common to both circuits.

The output voltage swing of the DF is limited by the threshold voltage of the input and output devices and the minimum drain-source voltage of the devices in the bias circuits. From Fig. 6.1 we see that V_{omin} and V_{omax} are

$$V_{omin} = V_{TH1} + \Delta_{M1} + \Delta_{Mx1} + \Delta_{Mx2} \tag{6.1}$$

$$V_{omax} = V_{DD} - (V_{TH2} + \Delta_{M2} + \Delta_{My1} + \Delta_{My2}) \tag{6.2}$$
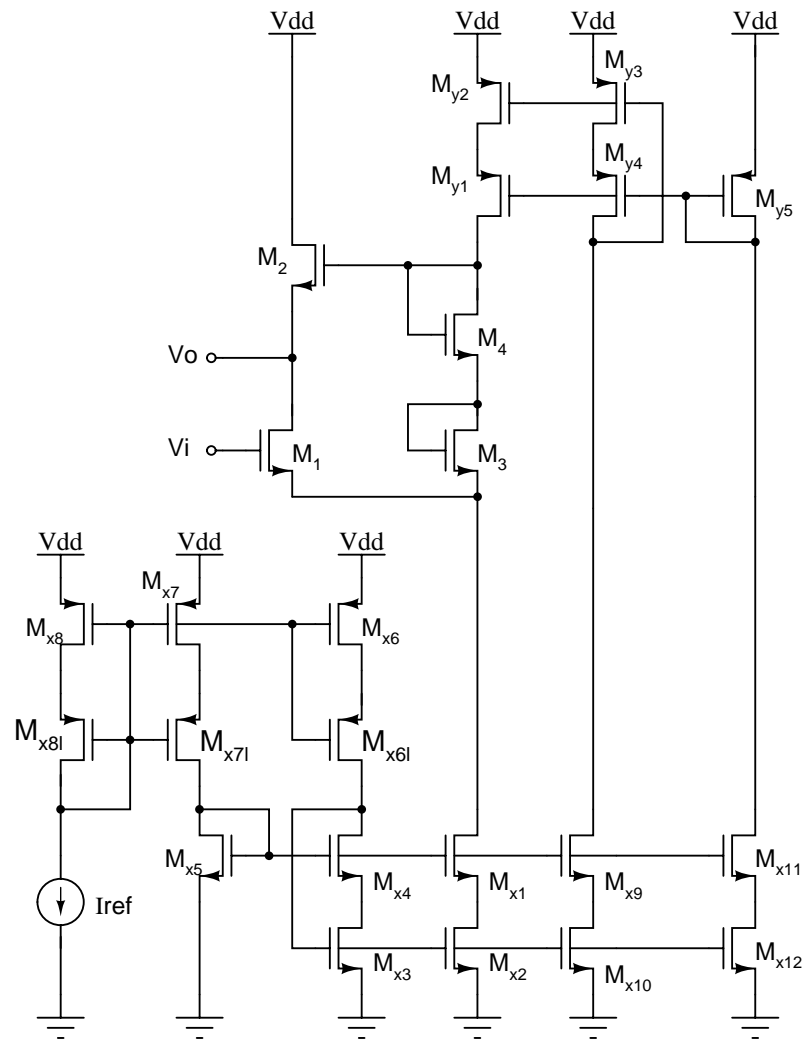
Figure 6.1. NMOS drain-follower.
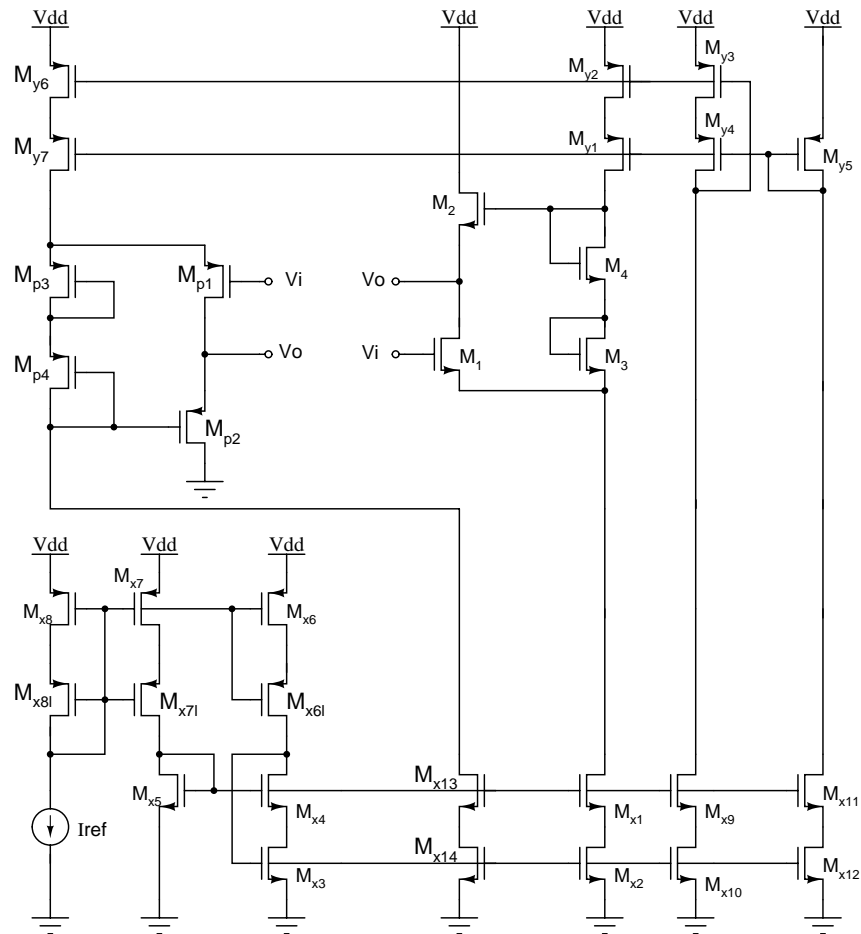
Figure 6.2. NMOS-PMOS drain-follower.

$$\Delta = V_{gs} - V_{TH} \tag{6.3}$$

In the Cypress Microsystems 0.5μm CMOS process it is possible to create NMOS transistors which are isolated from the substrate. In both versions of the buffer all of the devices in the signal path have their source and body tied together which helps maximize dynamic range by assuring that the buffers operate with zero body-bias transistor threshold voltages.

In Chapter 2 the small-signal dc gain, poles and zeros for the DF were presented. From Eq. 2.12 we see the importance of maximizing the output resistance of the bias current sources. Maximizing the dynamic range of the buffer is also desirable. In order to achieve these objectives bias circuits for both buffers are realized with wide-swing, high-output impedance cascoded current sources.

6.1.1. NMOS Drain-Follower Simulation Results

Simulation results for the NMOS DF are shown in Fig. 6.3-6.5 and Fig. 6.9. The device dimensions are listed in Table 6.1.

The magnitude response shown in Fig. 6.3 verifies the dominant pole behavior predicted by the small signal analysis of Chapter 2. The dc transfer characteristic shown in Fig. 6.3 indicates a maximum input voltage swing near $2V_{pp}$. The dc transfer characteristic is non-monotonic for buffer input voltages below 1V. This can be explained as follows. When the buffer input voltage goes low enough to turn off M_1 in Fig. 6.1, current continues to flow through the branch containing M_3 and M_4 and creates a bias voltage at the gate of M_2. With M_1 off, M_2 pulls the output voltage up to

Figure 6.3. NMOS drain-follower magnitude response and dc transfer characteristic.
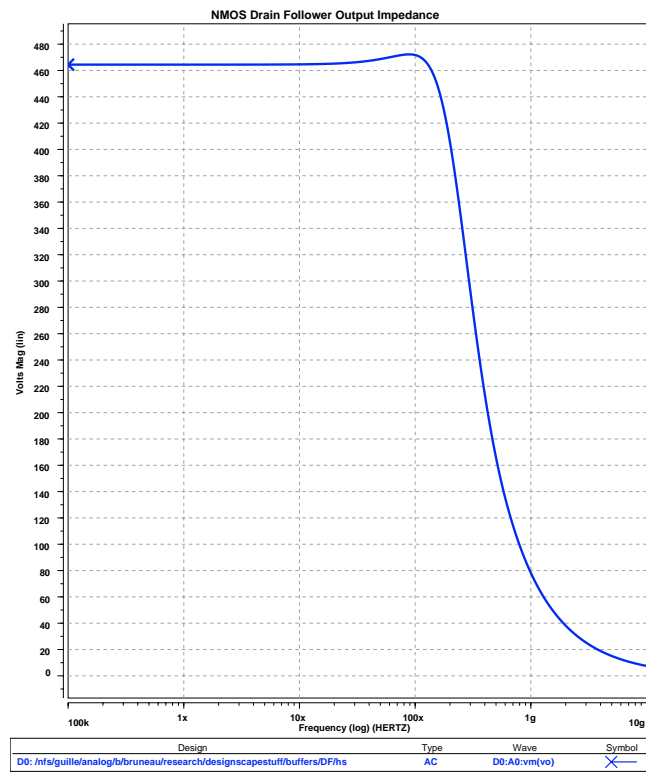
Figure 6.4. NMOS drain-follower output impedance.
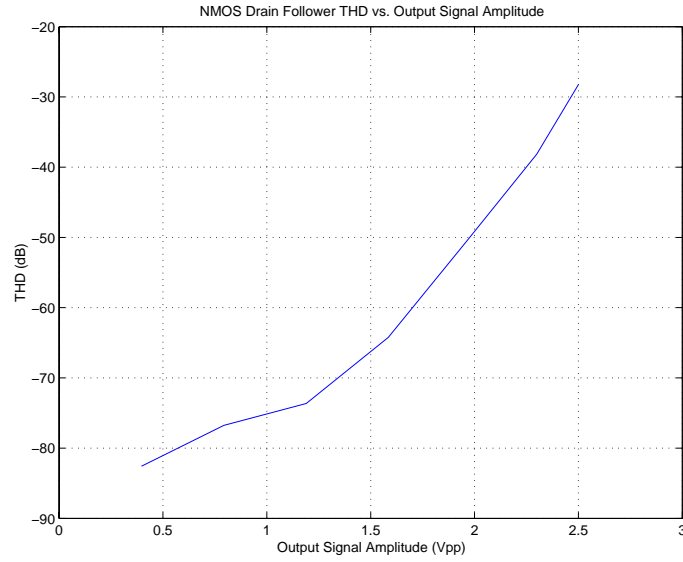
Figure 6.5. NMOS drain-follower THD vs. output voltage amplitude.

Transistor	W(μm)	L(μm)
M1, M2	72	0.9
M3, M4	24	0.9
Mx1, Mx2	48	0.9
Mx3, Mx4, Mx9-Mx12	12	0.9
Mx5	2	0.9
Mx6-Mx8, Mx6l-Mx8l, My1-My4	38	0.9
My5	6	0.9

Table 6.1. NMOS drain-follower device dimensions.

$$V_o = V_{DD} - (V_{gs2} + V_{dsy1} + V_{dsy2}) \qquad (6.4)$$

The output impedance shows slight peaking at higher frequencies. The output impedance of many circuits employing feedback exhibit this inductive behavior [8]. The simulation for total harmonic distortion was performed with a 2MHz input sinewave.

6.1.2. NMOS-PMOS Drain-Follower Simulation Results

Simulation results for the NMOS-PMOS DF are shown in Fig. 6.6-6.8 and Fig. 6.9. The device dimensions are listed in Table 6.2.

The simulation results for the NMOS-PMOS DF show the same trends as the NMOS DF but, unlike the NMOS DF the dc transfer characteristic shown in Fig. 6.6 is monotonic at high and low input voltages. At low input voltages the PMOS DF section of the circuit has sufficient drive capability to pull the output voltage down to

$$V_o = V_{THp2} + \Delta_{Mp2} + V_{dsx13} + V_{dsx14} \qquad (6.5)$$

As for the NMOS DF, simulation for total harmonic distortion was performed with a 2MHz input sinewave.

The slew rate of the two buffers are compared in Fig. 6.9. The simulation was performed with a 1.5V step input and 20pF capacitive load. Under these conditions the slew rate of the NMOS DF is $15V/\mu s$ while slewing has been virtually eliminated with the NMOS-PMOS DF, a significant improvement.
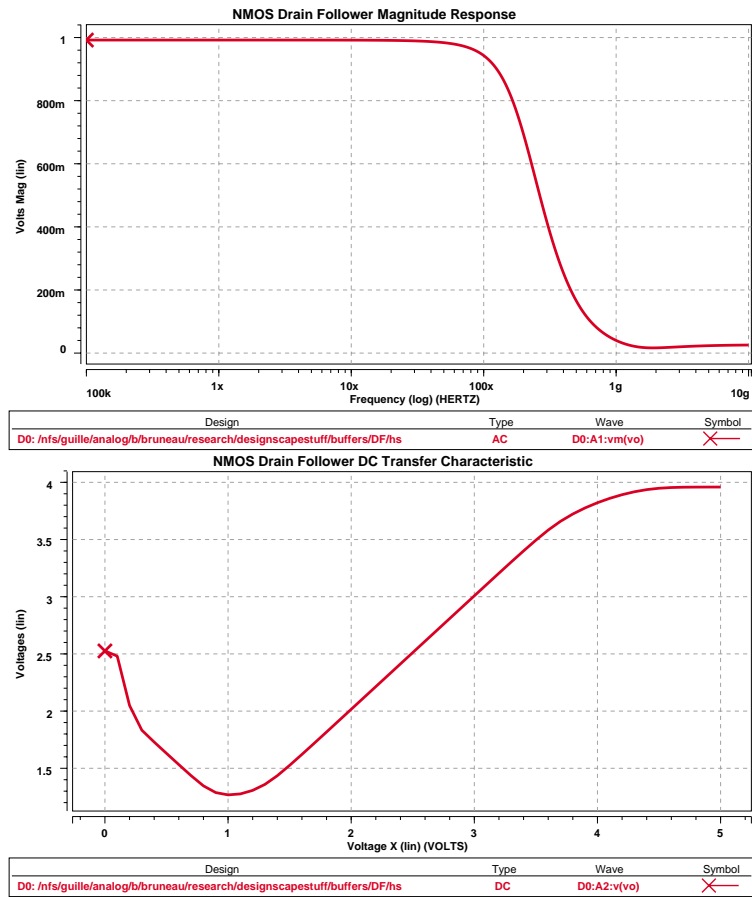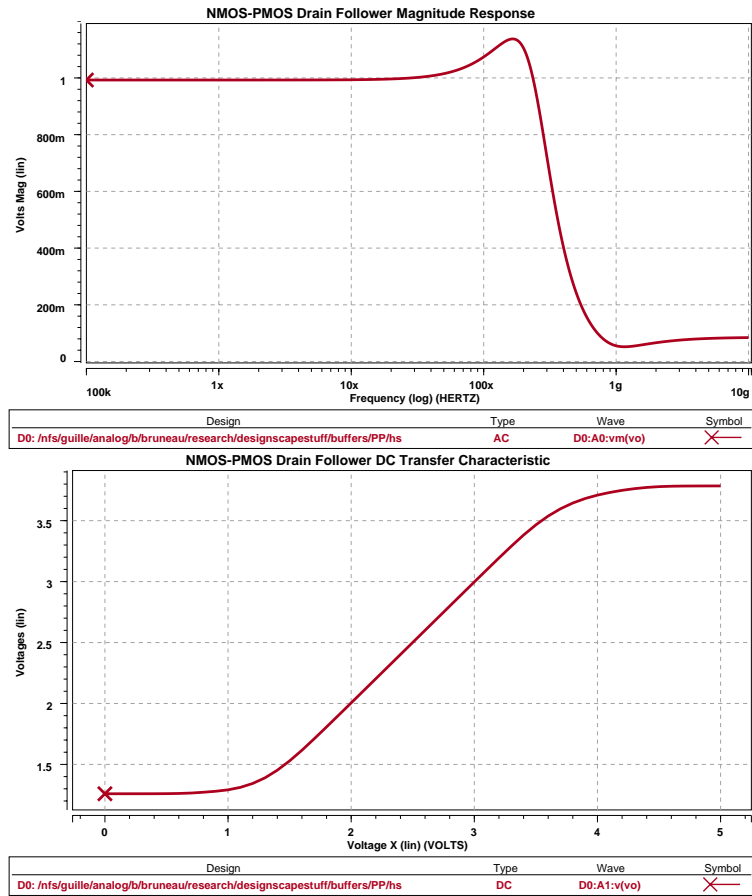
Figure 6.6. NMOS-PMOS drain-follower magnitude response and dc transfer characteristic.
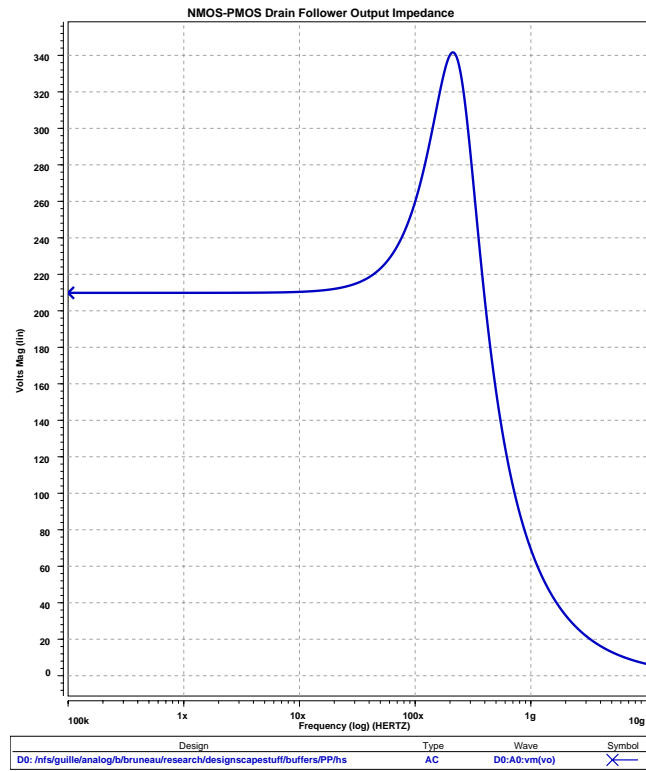
Figure 6.7. NMOS-PMOS drain-follower output impedance.

Transistor	W(μm)	L(μm)
M1, M2	72	0.9
M3, M4	24	0.9
Mp1, Mp2	216	0.9
Mp3, Mp4	72	0.9
Mx1, Mx2	48	0.9
Mx3, Mx4, Mx9-Mx14	12	0.9
Mx5	2	0.9
Mx6-Mx8, Mx6l-Mx8l, My1-My4	38	0.9
My5	6	0.9
My6, My7	152	0.9

Table 6.2. NMOS-PMOS drain-follower device dimensions.
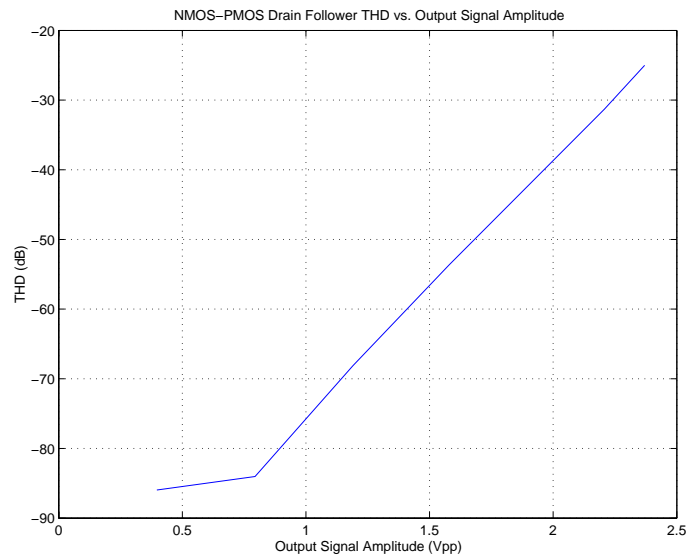
Figure 6.8. NMOS-PMOS drain-follower THD vs. output voltage amplitude.

6.1.3. Summary of Simulation Results

The results of simulations are summarized in Table 6.3. Both versions of the buffer have comparable DC gain. The NMOS-PMOS DF shows a 54% improvement in 3dB bandwidth over the NMOS DF while consuming 46% more power and twice the area. However, the NMOS-PMOS DF has much lower offset voltage and improved slew rate. Since the buffers will be driving capacitive loads in this application output impedance is not an issue. Both buffers exhibit total harmonic distortion near -60dB for a fairly wide range of input signals.

Since maximizing speed is the main objective of this implementation the NMOS-PMOS DF, with its relatively high bandwidth and slew rate, will be used as the active element in the UGB SC biquad filter design.
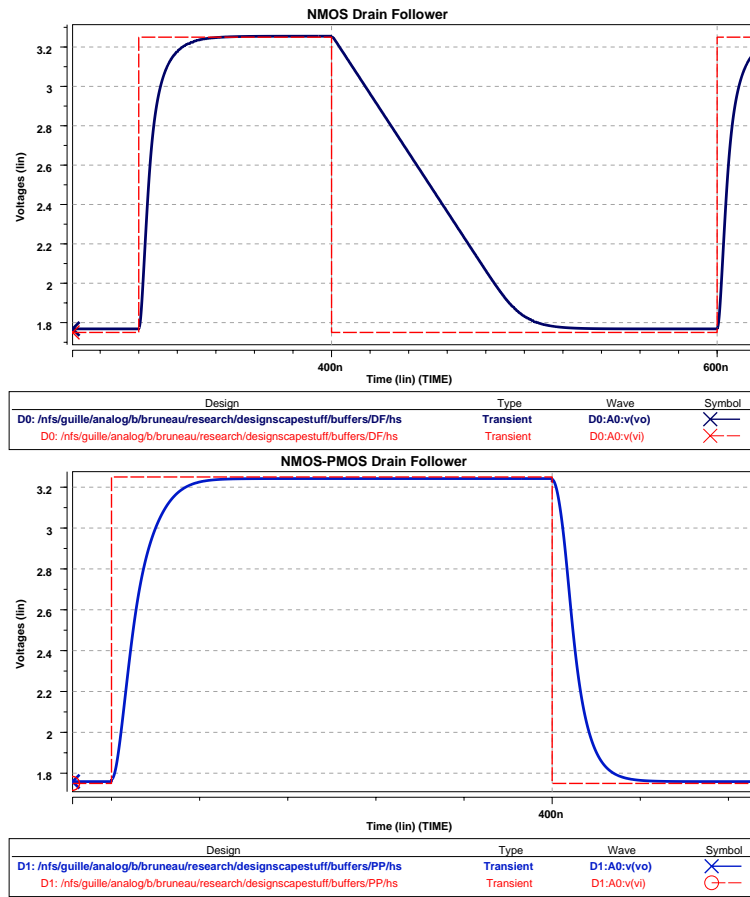
Figure 6.9. Drain-Follower slew rate comparison.

Metric	NMOS Drain-Follower	NMOS-PMOS Drain-Follower
f-3dB, 2pF load (MHz)	197	305
DC gain (V/V)	0.992	0.993
Offset Voltage (V)	0.012	0.001
THD at $V_o = 2V_{pp}$	-49dB	-38dB
Zout at 1MHz (Ω)	464	210
$P_{tot}(V_{DD} = 5V)$	4.5mW	6.6mW
$Area(\mu m^2)$	673	1486

Table 6.3. NMOS, NMOS-PMOS drain-follower comparison.

6.2. System Level Filter Design

6.2.1. Realizing A Discrete-Time Transfer Function

A discrete-time transfer function is found with the aid of a digital-filter design program.

$$H(z) = \frac{0.1596z^2 + 0.0695z + 0.1596}{z^2 - 1.043z + 0.455} \tag{6.6}$$

Eq. 6.6 will be realized with the UGB SC biquad filter shown in Fig. 3.10. The normalized capacitor values for the UGB SC biquad are found using the design equations presented in Chapter 3 and listed in Table 6.4. The capacitor values were adjusted to ensure maximum dynamic range. The adjusted capacitor values are listed in Table 6.4 as well. The magnitude response of the UGB SC biquad is shown in Fig. 6.10.
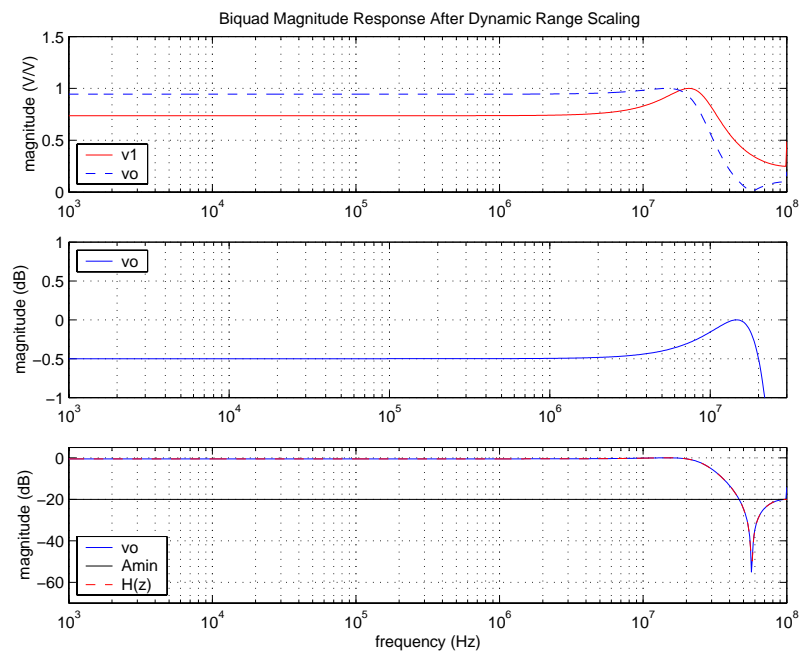
Figure 6.10. UGB SC biquad magnitude response.

Capacitor	Before Dynamic Range Scaling	After Dynamic Range Scaling
C_a	2.1388	2.1388
C_b	2.2656	2.2656
C_c	1	1
C_d	2.4354	2.4354
C_{e1}	5.9936	4.3753
C_{e2}	5.9936	5.9936
C_{i1}	5.2639	3.8426
C_{i2}	5.2639	5.2639

Table 6.4. Normalized biquad capacitor values before and after dynamic range scaling.

6.2.2. Selecting Minimum Capacitor Size

The final value of the capacitors in the biquad will be set by examining the amount of kT/C noise that each capacitor introduces into the system. The buffers in the biquad will produce distortion greater than 60dB for large input signals. This implies choosing capacitor sizes that allow for a signal-to-noise ratio (SNR) of 60dB. Additionally, we would like to keep the minimum capacitor size as small as possible to allow the biquad to be operated at high speed.

In some cases kT/C noise will be shaped by a transfer function in such a way that its contribution to the total noise power at the biquad output is negligible. The noise contributions of C_d, C_{e1} and C_{e2} are effectively high-pass filtered and

their contribution will be neglected. The noise from C_c will be neglected as well since it will be attenuated by the voltage divider formed between C_c and C_{i2}. In this implementation the attenuation is approximately 1/5. Making C_c as small as possible is desirable since the attenuation will increase as the ratio C_c/C_{i2} decreases. The noise introduced by C_a and C_b is the most significant since it appears at the output shaped by the biquad transfer function in the same manner as an input signal.

To calculate the kT/C noise contribution of C_a and C_b we will assume a minimum capacitor size of 0.25pF. With this minimum capacitor size C_a and C_b are 0.534pF and 0.566pF respectively.

The kT/C noise powers of C_a and C_b are

$$V_{na}^2 = \frac{kT}{C_a} = 7.75nV^2 \tag{6.7}$$

$$V_{nb}^2 = \frac{kT}{C_b} = 7.32nV^2 \tag{6.8}$$

where k = $1.38 \times 10^{-23} JK^{-1}$ and T = 300 K.

In the biquad filter buffer dynamic range limits the maximum output signal amplitude. From the preceding section on buffer design we see that the maximum input signal amplitude is approximately 1V. For an input sinewave with amplitude of 1V the output signal power is $0.707V^2$. The biquad SNR based on kT/C noise alone is

$$SNR = 10log_{10}\left[\frac{0.707V^2}{V_{na}^2 + V_{nb}^2}\right] = 75dB \tag{6.9}$$

Using a minimum capacitance of 0.25pF is sufficient to ensure that kT/C noise will not limit the SNR of the filter.

6.2.3. Switch Sizing

CMOS transmission gates will be used to implement the switches in the UGB SC biquad. The NMOS and PMOS transistors that comprise the transmission gates will have the same width and length. This will provide first-order cancellation of charge-injection and coupling of the clock signal onto the sampling capacitor at the expense of a reduced dynamic range [3].

Simulations were performed using the circuit in Fig. 6.11 to determine the minimum switch size which allows settling to within 0.1% accuracy. Simulations of the UGB SC biquad filter show that the buffers limit the maximum clock frequency to approximately 100MHz for 0.5pF unit-capacitance. In the final UGB SC biquad implementation the switches are slightly over designed to ensure that they do not limit the clock frequency.
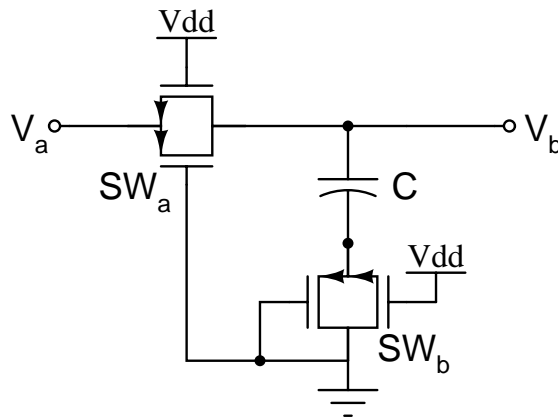

Figure 6.11. Switch test circuit.

With $(W/L)_a = (W/L)_b = 10/0.5$ and C = 1pF, 0.1% settling is achieved in 3.5ns. This corresponds to a clock frequency of 143MHz.

In Chapter 4 we saw that parasitic strays associated with switches degrade the accuracy of the filter. This is an incentive to try to minimize the switch parasitics and we have used asymmetrical switch sizing to accomplish this. As an example of asymmetrical switch sizing we will determine the switch size for C_a in Fig. 3.10.

During ϕ_1 C_a is in series with the switches S_{a1} and S_{a2}. Assuming C_a is 1pF, $(W/L)_{a1}$ and $(W/L)_{b2}$ should be 10/0.5 if 0.1% settling in 3.5ns is desired. If instead we set $(W/L)_{a1} = 7/0.5$ and $(W/L)_{a2} = 35/0.5$ we achieve the same settling but we have reduced the parasitic depletion capacitance of S_{a1} by 30%, reducing its effect on the filter response. Increasing $(W/L)_{a2}$ has no adverse effects on the filter performance. The remaining switches in the circuit have been sized in the same manner. The final switch device dimensions are listed in Table 6.5.

6.2.4. Capacitor Tuning

To minimize the effects of stray capacitors on the filter response parasitic capacitances were extracted from Spice simulation results and the capacitor values of the filter were adjusted using the methodology presented in Chapter 4. Fig. 6.12 shows the filter response with parasitic strays included in the circuit and Fig. 6.13 shows the filter response after tuning. Tuning has resulted in the filter response being very close to ideal. The final capacitor values used in the UGB SC biquad are listed in Table 6.6.

Switch	W(μm) (L = $0.5\mu m$)
S_{a1}, S_{a3}, S_{b3}	7
S_{a2}, S_{a4}, S_{b4}	35
S_{b1}	4
S_{b2}	30
S_c	6
S_{d1}, S_{d3}, S_{e21}, S_{e22}	8
S_{d2}, S_{d4}	40
S_{e11}, S_{e13}	14
S_{e12}, S_{e14}	70

Table 6.5. Switch device dimensions.

Capacitor	Before Tuning (pF)	After Tuning (pF)
C_a	0.5347	0.5347
C_b	0.5664	0.5664
C_c	0.25	0.25
C_d	0.6088	0.6088
C_{e1}	1.094	1.094
C_{e2}	1.4984	1.4984
C_{i1}	0.9606	0.4966
C_{i2}	1.3160	0.8279

Table 6.6. Final UGB SC biquad capacitor values.
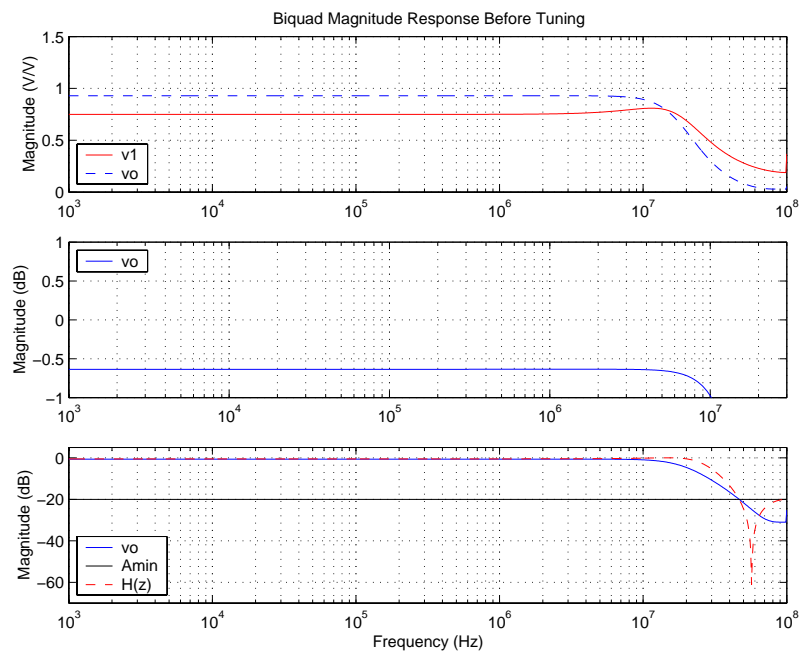
Figure 6.12. UGB SC biquad magnitude response before capacitor tuning.
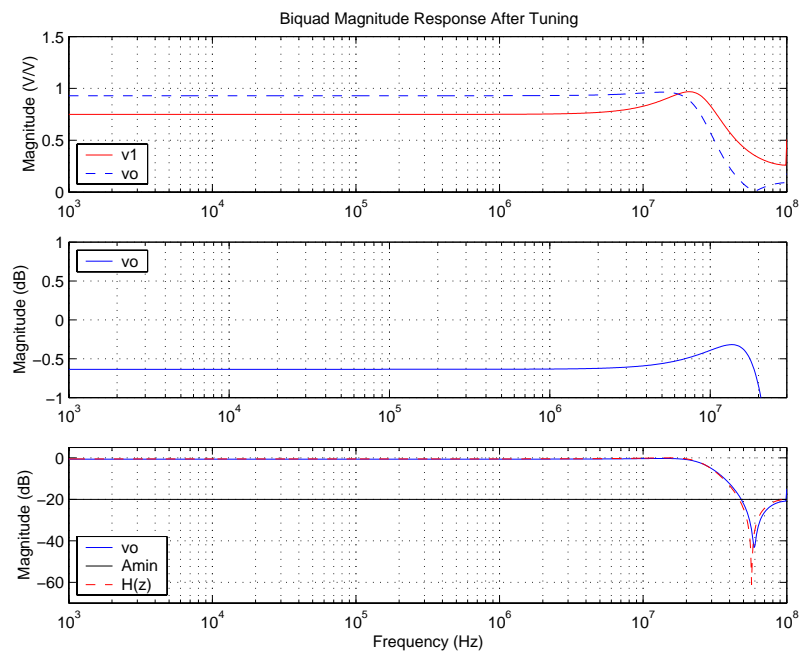
Figure 6.13. UGB SC biquad magnitude response after capacitor tuning.

6.3. Clock Generation Circuit

The clock generation circuit which generates the waveforms that control the switches in the biquad is shown in Fig. 6.14. The circuit produces two non-overlapping phases and their complements. The circuit also produces versions of the non-overlapping phases and their complements which have late rising edges and early falling edges. The latter waveforms are used to control switches that connect a capacitor terminal to common mode voltages such as buffer outputs and the common mode reference (V_{cm}). Switching in this manner will reduce distortion due to signal dependent charge-injection [19].
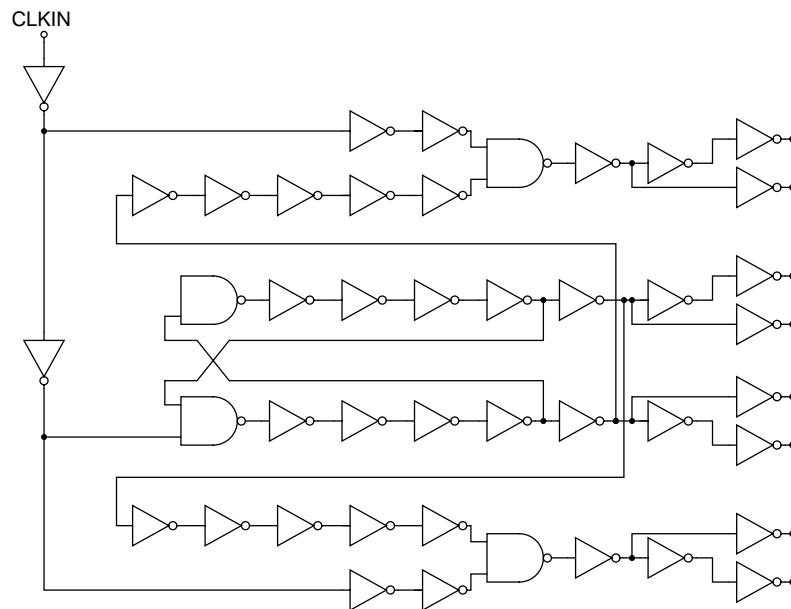
Figure 6.14. Clock generator.
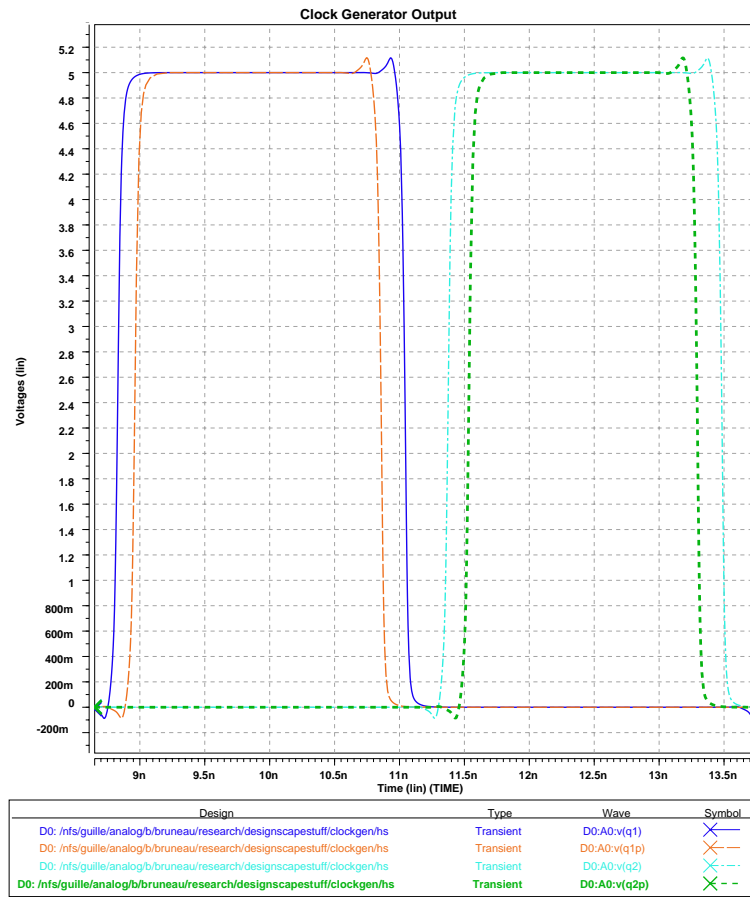
Figure 6.15. Clock generator output.

6.4. UGB SC Biquad Simulation Results

The complete filter was simulated with Hspice. Settling at each node in the circuit was examined to determine the maximum clock frequency that can be achieved for a given power dissipation and unit-capacitor. Fig. 6.16 shows the filter output for a 200mVpp input sinewave that is well within the filter passband. The spice simulations show a passband gain of 0.9V/V which matches Switcap simulation results very closely. Simulation results indicate that the filter can operate at a clock frequency greater than 100MHz with power consumption of 20mW from a 5V supply. The power consumption includes a track and hold circuit between the signal source and the filter input. The track and hold is necessary to eliminate analog feedthrough which would occur during the sampling phase.

Figure 6.16. UGB SC biquad simulation results.

6.5. Layout

The UGB SC biquad was fabricated in 0.5μm CMOS technology provided by Cypress Microsystems. The layout is shown in Fig. 6.17. Common layout techniques for SC circuits were employed [3] [15]. Fo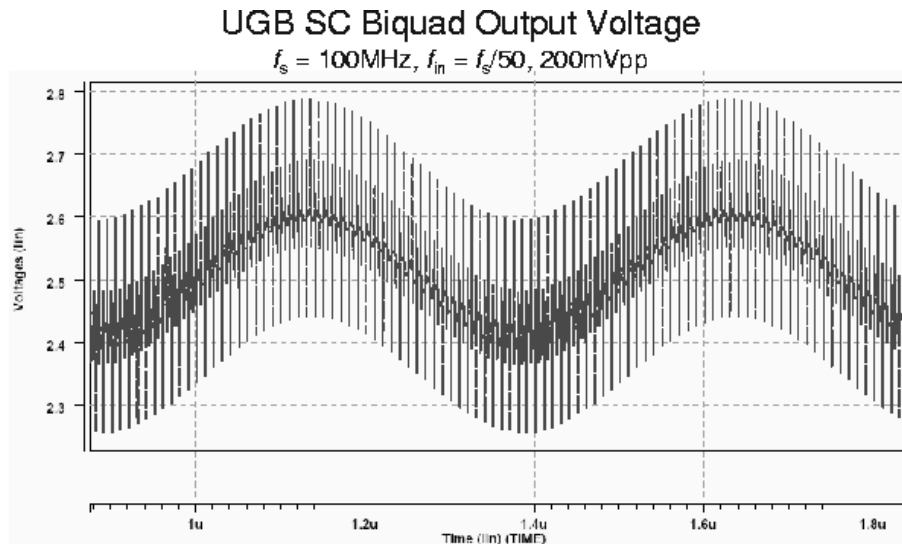r this implementation two single-ended biquads were placed symmetrically on the die which allows the filter to be operated pseudo-differentially. Assuming that common-mode signals appear in the signal paths of each biquad in a similar manner, operating the filter pseudo-differentially should provide good immunity from noise and reduced harmonic distortion [15]. There are three NMOS-PMOS DF in a single-ended filter, one in the track-and-hold circuit and one in each integrator of the filter. The track-and-hold circuits share a common external current reference, the buffers in the first integrator of the filters share a common external current reference and the buffers in the second integrator of the filters share a common external current reference. Each of these external current references can be adjusted independently which allows flexibility during testing.

Two PMOS SF are included as output buffers. Each biquad filter output is connected to the input of a PMOS SF while the output of the PMOS SF connects to a bonding pad. An on-chip digital logic circuit which is controlled externally allows the input of the PMOS SF to be switched from the filter output to a bonding pad. This allows the PMOS SF output buffer to be characterized separately and its performance can be taken into account when characterizing the filter. The PMOS SF output buffers share an external current reference.

An NMOS-PMOS drain-follower is included in order to verify the design of the buffers used in the filter. It has its own input and output pads and external current reference.
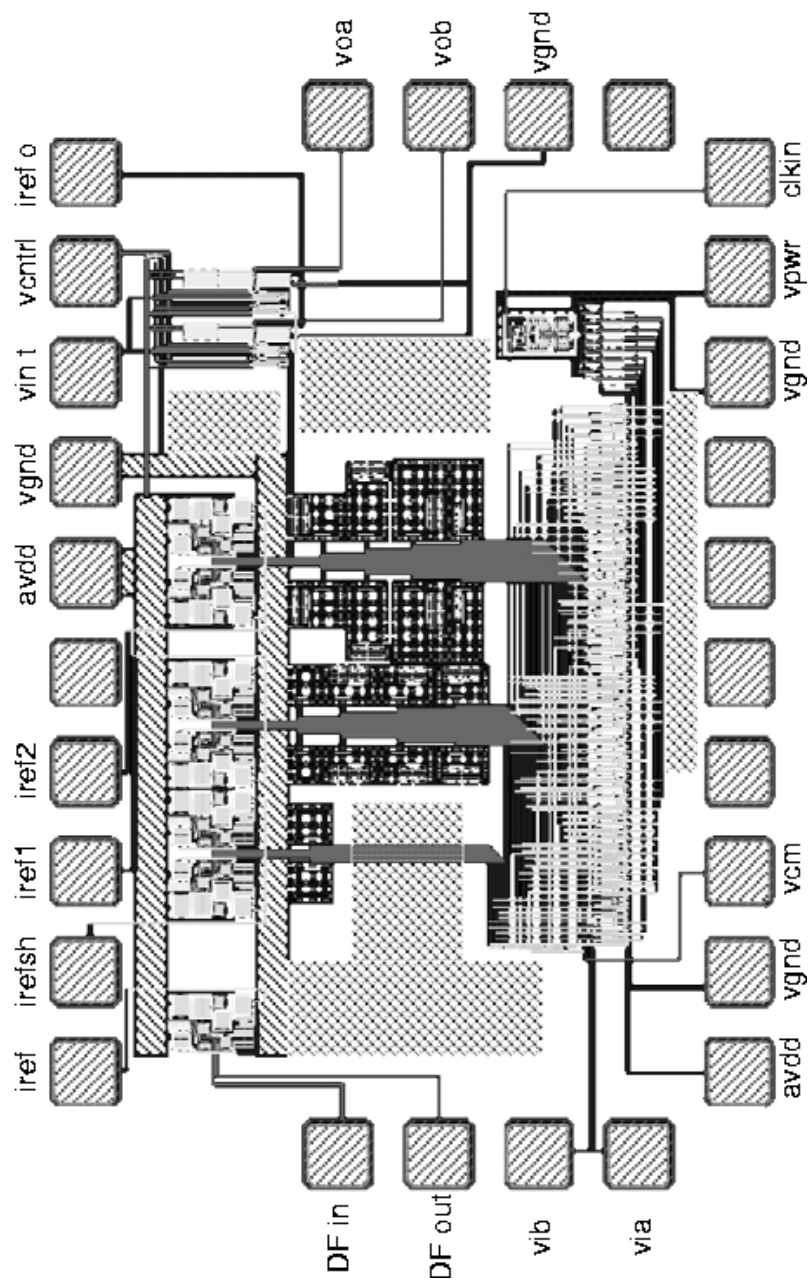
Figure 6.17. UGB SC biquad circuit layout.

Implementation	[2]	[20]	[21]	[22]	UGB SC Biquad
Technology	3μm	2.5μm	3.5μm	0.5μm	0.5μm
Cut-off frequency (MHz)	0.22	0.185	1	20	10
Sampling frequency (MHz)	12	10	21	200	100
Power supply (V)	10	5	10	3	5
Power consumption (mW)	5.7	18	165	10	20

Table 7.1. Comparison of unity-gain buffer SC filter implementations.

7. CONCLUSION

The work presented in this thesis is compared to previous implementations in Table 7. An opamp based implementation [22] is included in the comparison to show how UGB SC filter designs perform versus conventional SC filter architectures. The conventional architecture seems to offer the best performance. It achieves a clock frequency of 200MHz and 10mW power consumption from a 3V supply using double-sampling techniques. The UGB SC biquad implemented here would benefit from more optimization which would increase the performance of the circuit, making it a more viable option for discrete-time analog signal processing. If a double-sampling scheme is devised for UGB SC filters we will see an immediate doubleing of the clock frequency with no increase in power consumption. Other areas for optimization are reducing or eliminating the effects of stray capacitors, eliminating the need for track-and-hold circuits and reducing power consumption.

In this work a new voltage buffer, the drain-follower, achieves 300MHz bandwidth with 2pF load, a dc gain of 0.993V/V, 1mV offset voltage, -60 dB total harmonic distortion at 1.4Vpp output voltage and 6.5mW power dissipation from 5V supply. A unity-gain buffer switched-capacitor biquad filter has been implemented in 0.5μm CMOS technology. The circuit has been sent for fabrication. Simulation results of the biquad indicate operation at 100Ms/s with 20mW power consumption from a 5V supply can be achieved.

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