Design Techniques for Low-Voltage Analog-to-Digital Converter

By

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Chapter 1.

Introduction

The continued down scaling of transistor dimensions in submicron CMOS technology brings much optimism to the current and future state-of-the-art digital IC systems because of the dramatically improving IC density and frequency response. As the supply voltages are also scaled proportional to the transistor dimensions, the power dissipation of digital circuits is dramatically reduced. This trend widely satisfies the emerging market for portable electronic systems such as wireless devices and portable consumer electronics. However, low-voltage *analog* design does not necessarily imply low power consumption. In order to compensate for the reduced signal swing and to achieve the same dynamic range, power consumption generally increases [1].

One of the most important advantages of CMOS process is that both analog and digital circuits can be integrated onto the same die. Typically small but critical to the mixed-signal system, analog circuits routinely act as the interface between the real world (inherently analog) and the digital signal processor. Therefore, it is highly desirable for the traditional analog functions to migrate easily to digital CMOS processes. Today's state-of-the-art digital CMOS processes, however, are making the power supply transition below 1-V. This naturally brings attention to the difficult analog IC design challenges ahead. One class of circuits strongly affected

by this trend is the switched-capacitor (SC) circuits, used in many practical analog signal processing applications including a majority of CMOS data converters because of its inherently superior sample-and-hold function and good linearity. The fundamental limitation on the operation of a floating switch in SC circuits arises when the supply voltage becomes about same as or less than the sum of the absolute values of the PMOS and NMOS threshold voltages. There are several well-known solutions such as clock voltage boosting/bootstrapping, multi-threshold MOSFET, and the switched-opamp technique to bypass the problem. However, they all have their limitation to degrade circuit performance. In this work, the *Opamp-Reset Switching Technique* (ORST) topology is proposed for stable and high-speed low-voltage operation. Two integrated circuits have been implemented using this technique as a low-voltage analog circuit implementation. They are 10-bit 25MSPS pipelined analog-to-digital converter (ADC) and two-stage algorithmic ADC. The reset-opamp concept first appeared in [2] and a $\Delta\Sigma$ modulator design example using reset-opamp integrators was demonstrated in [3]. However, ICs introduced in this thesis are the very first two works done for the video-rate analog signal processing.

The thesis is organized as follows. In Chapter 2, CMOS device scaling theory and secondary effects of short-channel device are covered. Chapter 3 reviews the existing low-voltage SC circuit techniques and introduces the ORST. In Chapter 4, the basic operating principles of three types of high-speed ADC are compared. Actual design examples are attached in Chapter5 and Chapter 6. Chapter 5 shows the design of 1.4V 10-bit 25MSPS pipelined ADC based on the ORST. In Chapter 6, a 0.9V 1MSPS two-stage algorithmic ADC is presented with radix-based digital calibration in addition to the low-voltage design techniques. A highly linear input sampling circuit is also introduced. Finally, conclusions are given in Chapter 7.

Chapter 2.

CMOS Device Scaling

2.1 Motivation of CMOS Scaling

There are three major reasons to scale MOS transistor. The first reason is that the cutoff frequency (f_T) of the device increases. Given the small signal equivalent circuit of Figure 2.1, it is possible to estimate the maximum operating frequency of a MOS transistor. Let f_T be defined as the frequency where the MOSFET is no longer amplifying the input signal under optimum conditions. In other words, the frequency where the absolute value of the output current to input current ratio is unity when the output of the transistor is short-circuited. By inspection, the input current with the output short-circuited is

$$i_{in} = j\omega(C_{gs} + C_{gd})v_g \cong j(2\pi f)C_o v_g \tag{2.1}$$

where C_{gd} is taken to be small and C_o is C_{gs}. The output current is

$$i_{in} \cong g_m v_g \tag{2.2}$$

Under $i_{in}=i_{out}$, f_T can be obtained as

$$f_T = \frac{g_m}{2\pi C_o} = \frac{\mu_n v_d}{2\pi L^2} \tag{2.3}$$

Since f_T is a strong function of the channel length, as the device becomes smaller, the frequency response improves. The parasitic capacitance also tends to decrease. Second reason is the improved current drive. Eq (2.4) shows the transconductance (g_m) of the transistor.

$$g_m = \left.\frac{\partial i_d}{\partial v_g}\right|_{v_d = const.}$$

$$\cong \frac{W}{L}\mu_n \frac{\varepsilon_{ox}}{x_{ox}} v_d \qquad \text{for } v_d < v_{dsat}\text{, linear region} \tag{2.4}$$

$$\cong \frac{W}{L}\mu_n \frac{\varepsilon_{ox}}{x_{ox}} (v_g - v_{th}) \qquad \text{for } v_d > v_{dsat}\text{, saturation region}$$

where ε_{ox} is the permittivity of oxide and x_{ox} is the oxide thickness. Decreasing the channel length and gate oxide thickness increases g_m, i.e. the current drive of the transistor. Much of the scaling is therefore driven by decrease in L and x_{ox}. The third is the increasing density of circuit integration, which implies that more functional blocks can be fabricated on the same die.

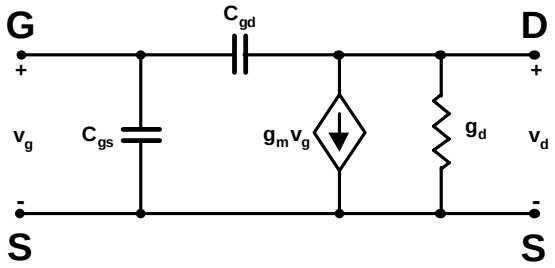


Figure 2.1 High-frequency small-signal equivalent circuits characterizing the ac response of the MOSFET.

However, full scaling requires that the voltages should be reduced by the same factor. If only device dimensions are scaled which is called constant-voltage scaling, many problems are encountered (e.g. increased electric field). It is impractical scaling. In 1974 Dennard proposed a scaling methodology, which maintains the electric field in the device constant [11].

Device / Circuit Parameter		Constant Field Scaling Factor
Dimension	x_{ox}, W, L, x_j	1/K
Substrate doping	N_a	K
V_{DD}	V	1/K
I_{DD}	I	1/K
Gate capacitance	WL / x_{ox}	1/K
Gate delay	CV / I	1/K
Power consumption	$CV^2 / delay$	$1/K^2$

Table 2.1 Constant field scaling of MOSFET device.

Here x_j is the junction depth. In reality, constant field scaling has not been observed strictly. Since the transistor current is proportional to the gate overdrive (V_G-V_{th}), high performance demands have dictated the use of higher supply voltage. However, higher supply voltage implies increased power dissipation. This opposes the recent trend of widely emerging market for portable electronic systems such as wireless devices and portable consumer electronics. This is because the power dissipation in digital circuits has a quadratic dependence on the supply voltage. Therefore, CMOS scaling is mainly driven by digital VLSI. Table 2.2 shows the roadmap of the device scaling [12].

However, the most important limitation to scaling theory arises from the fact that the device physics of small-geometry MOSFETs can be significantly different from the results obtained by scaling the gradual channel equations. The remaining Sections of this Chapter examine secondary effects from small dimension device that are important in circuit performance.

Near-term	2001	2002	2003	2004	2005	2006	2007
ASIC physical L_{MIN} (nm)	90	75	65	53	45	37	32
Digital minimum V_{DD}	1.2	1.1	1.0	1.0	0.9	0.9	0.7
Analog minimum V_{DD}	3.3 – 1.8		2.5 – 1.8				

Table 2.2 Road map of near-term CMOS device scaling.

2.2 Limitations of Scaled CMOS

2.2.1 Threshold Voltage Modification

The threshold voltage used to describe a MOSFET can be written as

$$V_{th} = V_{FB} + 2|\phi_F| + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_a(2|\phi_F|)} + \frac{qD_I}{C_{ox}} \tag{2.5}$$

where V_{FB} is called flat band voltage, Φ_F is bulk Fermi potential, D_I is the ion dose in substrate ion implantation, and N_a is the substrate doping concentration. In a short channel MOSFET, a significant fraction of the total bulk depletion charge underneath the gate originates from the *pn* junction depletion of source and drain. This charge should not be accounted for the threshold voltage expression since it is not controlled by gate voltage. Although the actual geometry of the problem is quite complicated, a simple model that exhibits reasonable accuracy may be constructed as shown in Figure 2.2. A geometry dependent *form factor* that accounts for the reduction in bulk charge from a long-channel case can be written as

$$\Delta L = \frac{L - L'}{2}$$

$$f = 1 - \frac{\Delta L}{L} < 1 \tag{2.6}$$

while source and drain are biased to ground. A closed-form expression can be developed for *f* by making two approximations. First, the pn^+ source and drain edges are taken to be quarter-circular arcs; each has a radius equal to the junction depth x_j. Second, the *pn* junction depletion regions are assumed to extend a distance x_{dm} into the p-type substrate, where x_{dm} is the maximum MOS depletion depth

$$x_{dm} \cong \sqrt{\frac{2\varepsilon_{si}}{qN_a}(2|\phi_F|)} \tag{2.7}$$

Note that x_{dm} follows the curvature of the n^+. One way to define a short-channel MOSFET is to require that L be the same order of magnitude as x_{dm}. Specifying this condition then allows the geometry partitioning shown in Figure 2.3.

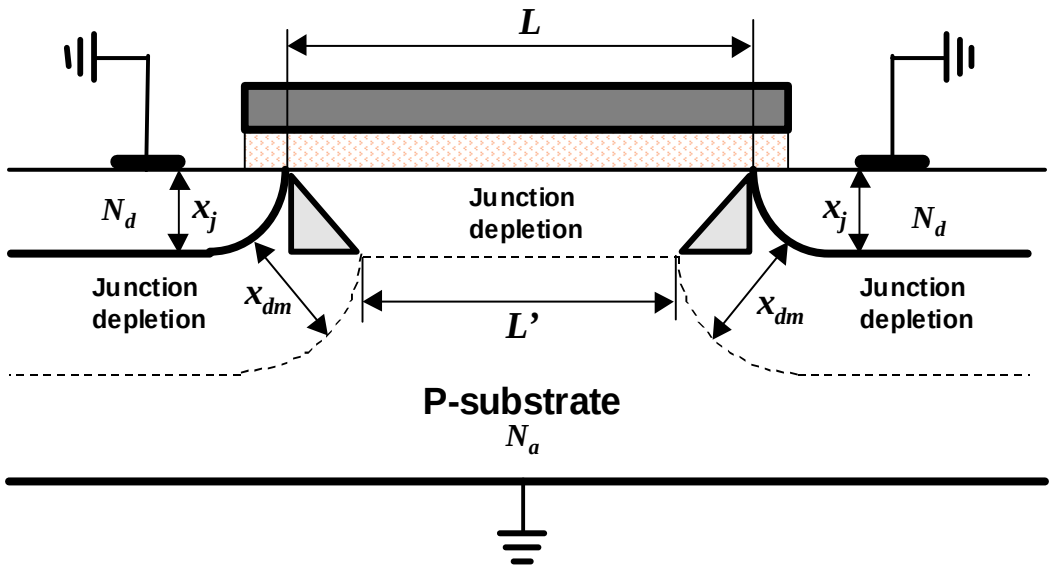


Figure 2.2 Simplified MOSFET model for calculation of threshold voltage in a short-channel device.

Computation of f requires a finding ΔL. This can be obtained with the aid of the triangle. By inspection,

$$(x_j + x_{dm})^2 = x_{dm}{}^2 + (x_j + \Delta L)^2 \tag{2.8}$$

Solution of a simple quadratic for ΔL is

$$\Delta L = -x_j + \sqrt{x_j{}^2 + 2x_j x_{dm}} \tag{2.9}$$

Using this result, the form factor can be rewritten as

$$f = 1 - \frac{x_j}{L}\left[\sqrt{1 + \frac{2x_{dm}}{x_j}} - 1\right] \tag{2.10}$$

as an approximate expression for f within the limit of this model. The threshold voltage can be obtained by simply applying Eq. (2.10) to Eq. (2.5). Thus,

$$V_{th} = V_{FB} + 2|\phi_F| + \frac{qD_I}{C_{ox}} + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_a(2|\phi_F|)}\left[1 - \frac{x_j}{L}\left(\sqrt{1 + \frac{2x_{dm}}{x_j}} - 1\right)\right] \tag{2.11}$$

gives complete expression for the threshold voltage with a modification term. From Eq. (2.11), the threshold shift can be easily computed to be

$$\Delta V_{th} = -\frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_a(2|\phi_F|)}\,\frac{x_j}{L}\left(\sqrt{1 + \frac{2x_{dm}}{x_j}} - 1\right) \tag{2.12}$$

Since this shift is proportional to (x_j / L), one alternately defines a short-channel MOSFET as the channel length becomes comparable to the junction depth. The plot in Figure 2.4 shows the threshold voltage variations predicted by Eq. (2.12).

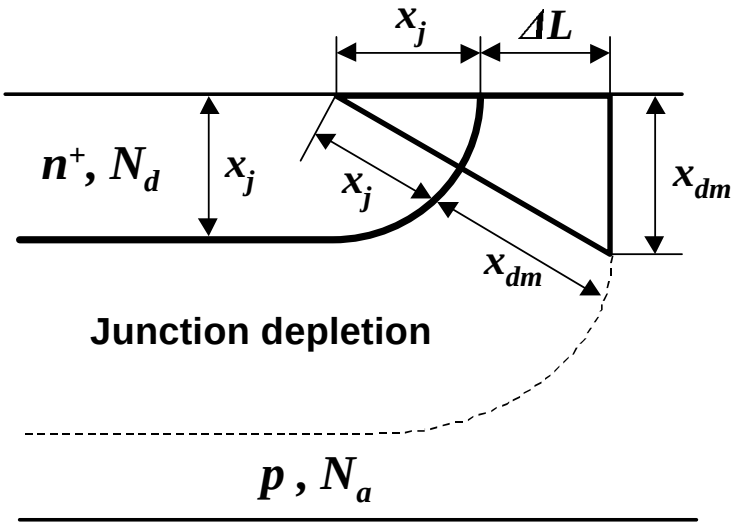


Figure 2.3 Simplified MOSFET providing a triangle model.

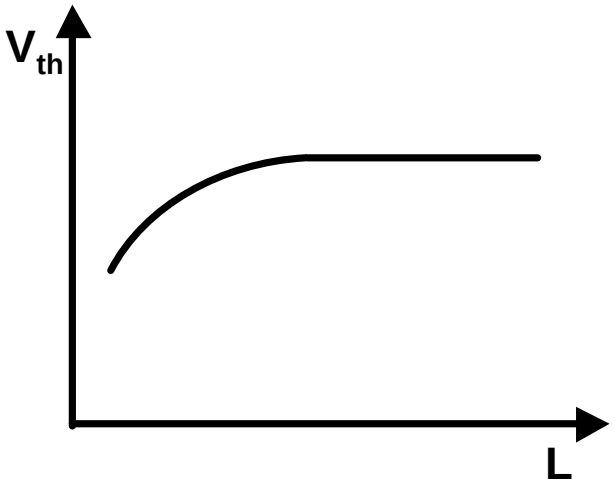


Figure 2.4 Threshold voltage variations in a short-channel device.

2.2.2 Subthreshold Conduction

When the surface is in weak inversion (i.e. $V_G < V_{th}$), the current flow is viewed as being blocked by a *barrier potential* Φ_B. Increasing the gate-source voltage to $V_{GS} > V_{th}$ reduces the barrier potential to $\Phi_B=0$, allowing drift current to flow. The most important effect in small MOSFETs arises from variations in the barrier potential with $V_{GS} < V_{th}$. In long-channel device, this would correspond to cut-off. However, the physics of barrier control shows that the current flow does exist. This results in subthreshold conduction in the device. There are several subthreshold conduction phenomena in short-channel MOS devices, which are drain-induced barrier lowering (DIBL) and punch-through effect, discussed next.

For short-channel devices, the electric field from the drain begins to have a significant influence on the channel charge. This is called drain-induced barrier lowering (DIBL). Figure 2.5 shows how two-dimensional effects alter the internal potential distribution in a MOSFET. The electric field lines induced by V_{DS} point away from the n^+ drain region. In a short channel

MOSFET, a significant fraction point toward the source, changing the potential barrier seen by electrons. A simple model for the barrier potential is

$$\phi_B = \phi_r + AV_{GS} + BV_{DS} \tag{2.13}$$

where Φ_r (< 0) is a reference potential and *A*, *B* are structural constants determined by the geometry. *A* is less than unity and $B << A$ generally holds in this model. The expression for Φ_B shows a reduction in barrier magnitude with increasing V_{DS}. If V_{DS} is increased (or the channel length is decreased), barrier-control equation changes to

$$\phi_B = \phi_r + AV_{GS} + BV_{DS} - CV_{GS}V_{DS} \tag{2.14}$$

This results in punch-through effect.

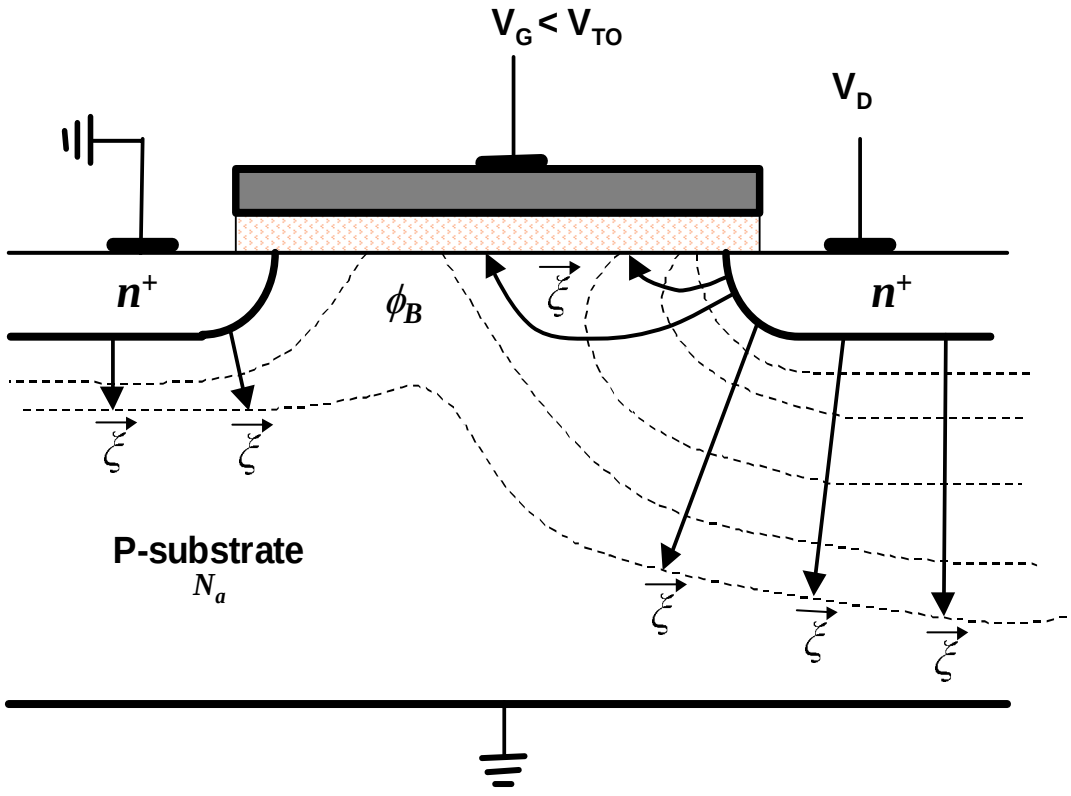


Figure 2.5 Potential region of a MOSFET.

Punch-through occurs when the source and drain are separated by a few microns or less. It becomes possible for the *pn* junction depletion regions around the source and drain to touch or punch-through as shown in Figure 2.6. When punch-through occurs, a significant change takes place in the operation of the MOSFET. Notably, the gate loses control of the subgate region except for a small portion of the region immediately adjacent to the Si-SiO_2 interface. The source-to-drain current is then no longer constrained to the surface channel, but begins to flow beneath the surface through the touching depletion regions. As a practical manner, punch-through in small-dimension MOSFETs is routinely suppressed by increasing the doping of the subgate region and thereby decreasing the source/drain depletion widths. This can be accomplished by increasing the substrate doping. However, increasing the substrate doping has the adverse effect of increasing the parasitic capacitance. Consequently, it is common practice to perform a deep-ion implantation to selectively increase the doping of the subgate region.

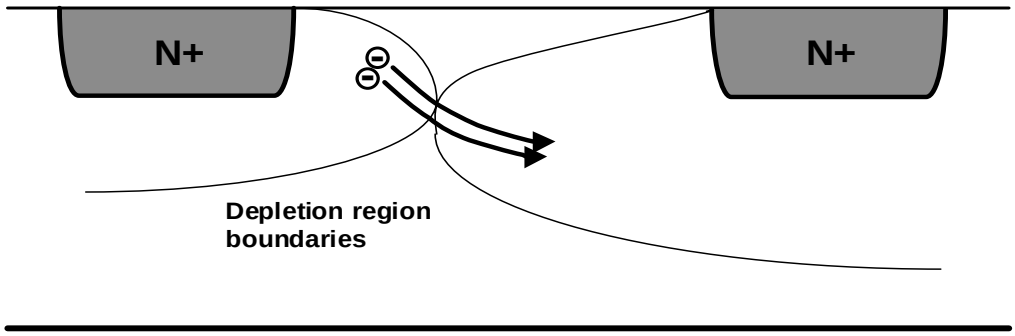


Figure 2.6 Punch-through and space charge current in a short-channel MOSFET.

2.2.3 Velocity Saturation

In the conventional analysis of the long-channel MOSFET, there is no theoretical limitation on the velocity that the carriers can attain in the surface channel. It is implicitly assumed

the carrier velocities increase as needed to support the current. In reality, the carrier drift velocities inside silicon approach a maximum value when accelerating electric field exceeds about 10^4V/cm for electrons. Therefore, velocity saturation causes the channel current to reach saturation before $V_D=V_G-V_{th}$. Instead of I_{Dsat} being proportional to $(V_G-V_{th})^2$ it is linearly proportional to V_G-V_{th} and is approximately given by

$$I_{Dsat} = WC_{ox}(V_G - V_{th})V_{sat} \tag{2.15}$$

This is shown in Figure 2.7.

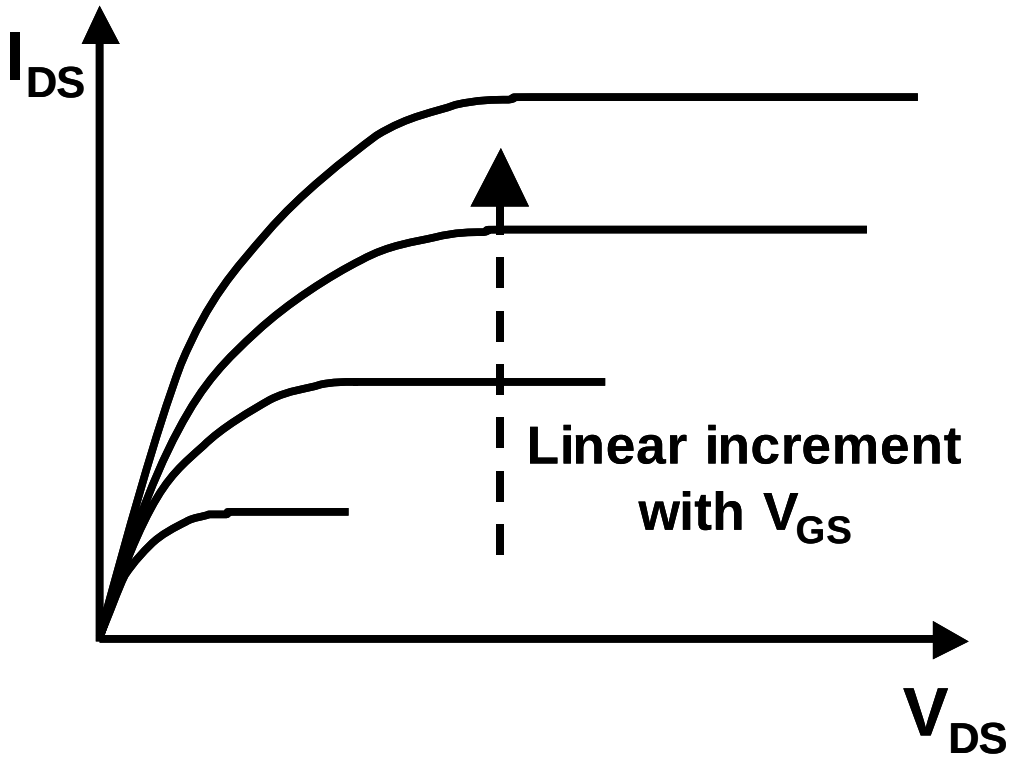


Figure 2.7 Effect of velocity saturation on the MOSFET I-V characteristics.

2.2.4 Hot Carrier Effect

There is a certain amount of carrier multiplication in the high field depletion region near the drain in all MOSFETs. In long-channel devices, the multiplication is negligible. However, in

short-channel devices, carrier multiplication coupled with regenerative feedback can dramatically increase the drain current and place a reduced limit on the maximum operating V_D. The basic mechanism is illustrated in Figure 2.8.

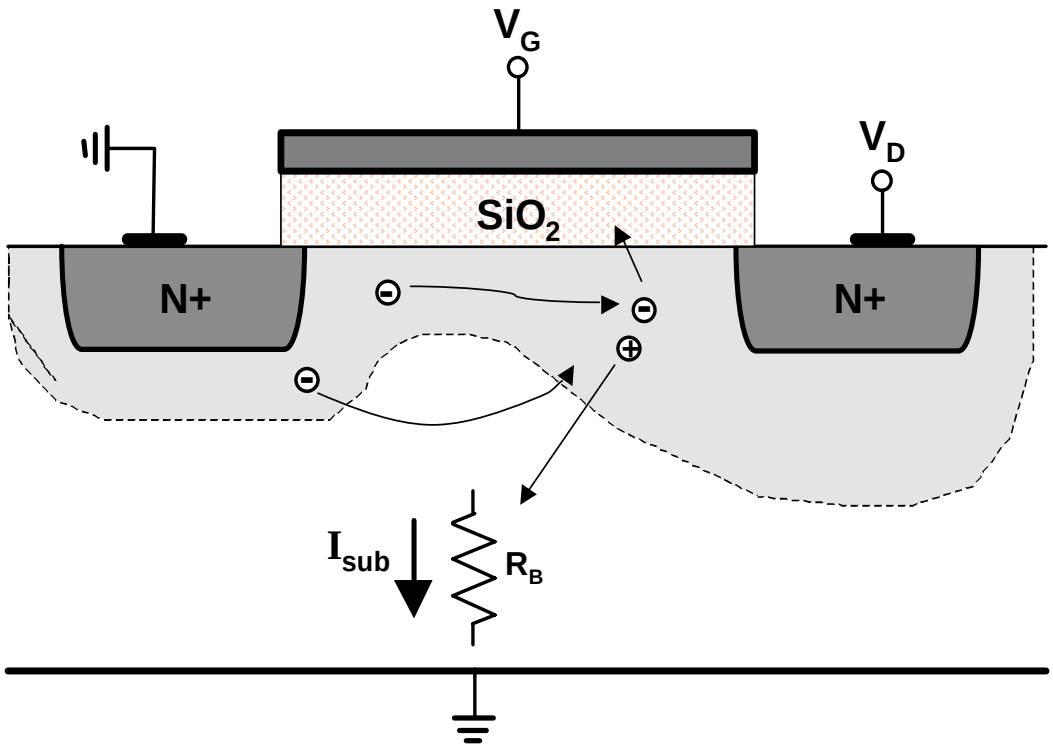


Figure 2.8 Visualization of hot carrier effect in a short-channel MOSFET.

The process is initiated by channel current entering the high lateral electric field region in the vicinity of the drain. Hot carriers can have sufficient energy to overcome the Si-SiO_2 barrier. They are injected from channel to the gate oxide and cause gate current. Trapping of some of this charge can change threshold voltage permanently. In the channel, avalanching can also take place producing electron-hole pairs (EHPs) through impact ionization. The holes produced by avalanching drifts into substrate and are collected by the substrate contact causing voltage drop

due to I_{sub}. This drop can cause substrate-source junction to be forward biased causing electrons to be injected from source into substrate. Some of injected electrons are collected by the reverse biased drain and cause a parasitic BJT action. These electrons are then cause more impact ionization, which make regenerative feedback loop. The process is stable as long as the fractional increase in the drain current or the multiplication factor is less than $1/\alpha$, where α is the common-base gain of the parasitic BJT. At high-enhanced currents there is the potential for excessive current flow through the device and device failure.

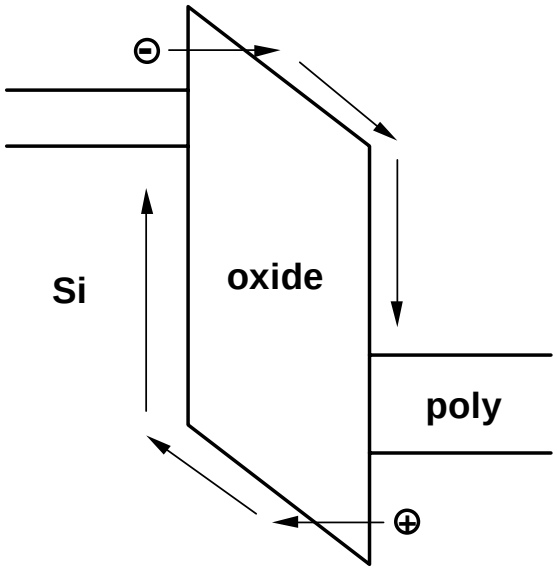


Figure 2.9 Electron tunneling into the oxide conduction band.

2.2.5 Breakdown

One important dimension that cannot be arbitrarily scaled is the gate oxide thickness (x_{ox}). Note that thin gate oxide is desirable because it increases the current density of the MOSFET and control the channel charge effectively. There are two basic reasons inhibiting the reduction of the

thickness. The first is a processing limitation. It is very difficult to grow uniform oxide layer with a thickness very thin because of the presence of *pinholes*, localized points where the oxide has failed to flow to the thickness of surrounding regions. When a gate is formed around pinhole, an electrical short with the substrate may occur. This, of course, eliminates the field effect and renders the device (chip) inoperative. However, as technology improves, the minimum attainable x_{ox} can be reduced safely and this *pinhole* effect is typically the statistically least common failure.

Second is that electrons tunnel into the oxide conduction band as shown in Figure 2.9. Once these electrons reach the conduction band of the oxide, the electric field accelerates them toward the gate. Some theories propose that these energetic electrons generate EHPs. A fraction of these holes can then be trapped into the oxide. These charges locally increase the electric field and tunneling flow. If enough positive charges are accumulated, the tunneling barrier is reduced sufficiently to let current to freely flow and the oxide has been broken down. Alternative theory explains that the electrons with enough energy collide into the crystal lattice at the gate-SiO_2 interface and break Si-O bond, resulting in forming defects. The positively charged defects locally attract more electrons that deepen the damage into the oxide. Eventually a conductive path is formed through the oxide. This process is illustrated in Figure 2.10. Those oxide breakdowns happen under oxide electric field greater than about $8x10^6$V/cm.

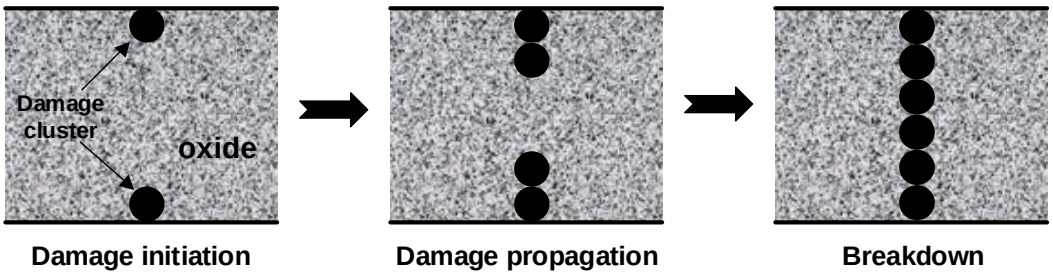


Figure 2.10 Oxide damage by electron colloision into SiO_2.

Both theories imply that the time to oxide failure is a function of applied voltage, time duration, and defect's density. One quantitative model for the lifetime T_{BD} of gate oxide combines these three parameters [13].

$$1=\frac{1}{\tau_o}\int_0^{T_{BD}} \exp\left(-\frac{GX_{eff}}{V_{ox}(t)}\right)dt \tag{2.16}$$

τ_0 and G are constants and X_{eff} is the effective oxide thickness due to defects, and $V_{ox}(t)$ is the time-dependent voltage across the oxide. Eq. (2.16) shows that it is accumulation of stress over time that determines breakdown. Thus, instant ac or transient stress is less harmful than dc stress. Eq. (2.16) can be simplified when V_{ox} is constant.

$$V_{ox} < \xi_{BD} \cdot xt_{ox} \tag{2.17}$$

$$t_{BD} = \tau_o(T) e^{G(T)\, x_{ox}/V_{ox}} \tag{2.18}$$

Eq. (2.18) shows that under such dc stress, the lifetime of gate oxide is exponentially dependent on the field in the oxide. ξ_{BD} is the breakdown electric field. For lifetime of 30 years, E_{bd} is typically $5\text{x}10^6$V/cm. As the oxide voltage exceeds ξ_{BD}, the lifetime of oxide decreases exponentially.

Another problem in implementing the scaling transformations originates from the requirement that the substrate doping N_a be increased. This tends to lower the MOSFET drain-source breakdown voltage, as can be seen from a simplified analysis. Assuming that the results from a one-sided step junction can be used, the total depletion width is approximately

$$x_d \cong \sqrt{\frac{2\varepsilon_{si}}{qN_a}(\phi_o + V_{DS})} \tag{2.19}$$

where Φ_o is a built-in potential. The maximum depletion electric field occurs at the junction with

$$\xi_{\max} \cong \frac{qN_a x_d}{\varepsilon_{si}} \tag{2.20}$$

When the maximum field intensity reaches a critical value ξ_{BD}, the reverse bias junction will break down. For example, avalanching occurs. To compute the drain-source breakdown voltage $V_{DS,BD}$, two equations are combined to write

$$\xi_{BD}{}^{2} \cong \frac{2qN_a}{\varepsilon_{si}}(\phi_o + V_{DS,BD}) = const. \tag{2.21}$$

This implies that breakdown voltage is inverse proportional to N_a. Increasing N_a for bypassing puchthrough and other secondary effects may result in lowering the junction breakdown voltage.

Chapter 3.

Low-Voltage Switched-Capacitor Circuit Design

The switched-capacitor (SC) technique is routinely used in analog building blocks for its inherently superior sample-and-hold function and good linearity. Under very low-voltage conditions, however, SC circuits suffer from a severe switch-overdrive problem. A new novel switching technique including some of the well-known techniques that can alleviate this problem are summarized in this Chapter.

3.1 Floating Switch Problem

One of the key limitations of future CMOS technologies remains the restricted supply voltage, limited primarily by the thin gate oxide that is prone to voltage stress (reliability) and breakdown. Thus, all analog circuits should adapt to the downscaled supply voltages and operate reliably. One class of circuits strongly affected by this trend is the switched-capacitor (SC) circuits, used in many practical analog signal processing applications. The fundamental limitation on the operation of a floating switch in SC circuits arises when the supply voltage becomes about same as or less than the sum of the absolute values of the PMOS and NMOS threshold voltages.

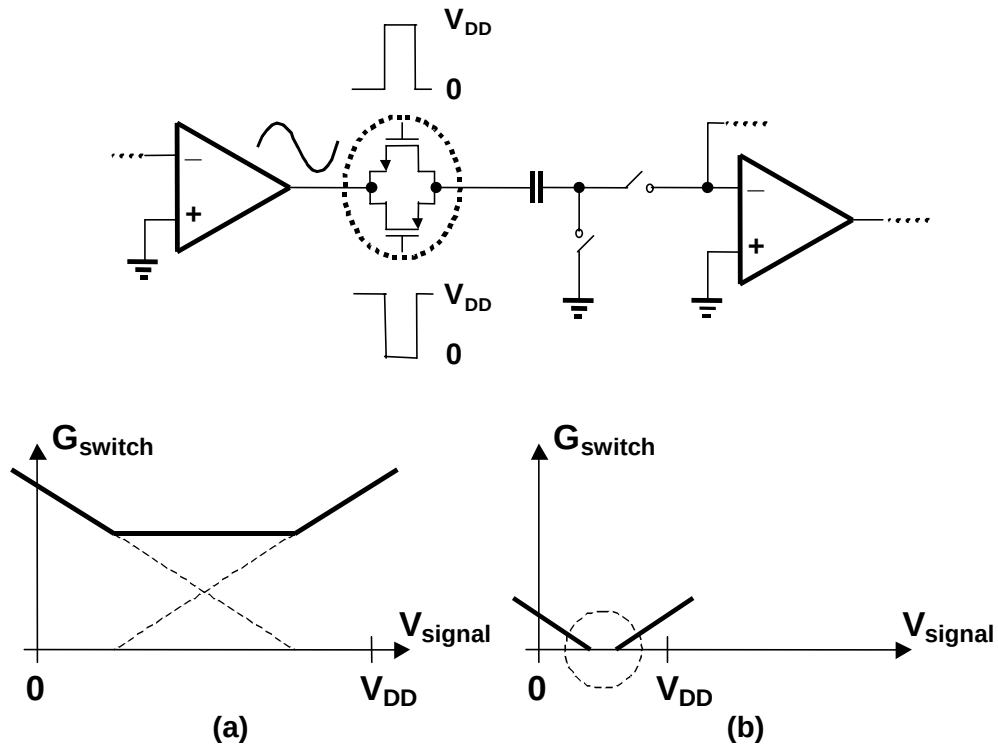


Figure 3.1 Switch conductance: (a) under high-V_{DD} and (b) under low-V_{DD}.

Figure 3.1 shows the conductance of a CMOS switch versus analog input signal. The dashed line implies individual conductance of the NMOS and PMOS devices. When V_{DD} is much larger than $V_{th,N} + |V_{th,P}|$, it is easy to achieve large on-conductance for rail-to-rail swing. As V_{DD} approaches $V_{th,N} + |V_{th,P}|$, switch resistance and signal-dependent nonlinearity increase dramatically. In the case where V_{DD} is smaller than $V_{th,N} + |V_{th,P}|$, there will be a signal range where the switch will not conduct. In this case, although we can still use the reduced signal range near V_{DD} or *GND*, the signal swing range will suffer. To ensure certain level of signal-to-noise ratio (SNR), large capacitors should be used for *kT/C* consideration. This is not very practical for

high-speed applications. Another reason to avoid signal range shifting is that the range near the rail is not the optimal operation range for opamps. This is because of dc gain reduction.

3.2 Multi-Threshold MOSFET

Special process steps can be used to reduce the threshold voltage of either or both NMOS and PMOS transistors [14]. This option is possible at the cost of extra mask layers in the CMOS process, which is not always available in typical CMOS processes, or avoided to reduce cost in the high-volume IC market. Thus, using the multi-threshold MOSFETs detracts from the cost benefits of mixed-signal integration. Perhaps more technological drawback of low-threshold devices is the increased leakage current (i.e. low-threshold makes transistors easy to be turned *on* but difficult to be turned *off* due to number of secondary effect mentioned at the previous Chapter). This limits the resolution of SC circuits whose operation is based on charge conservation.

3.3 Clock Voltage Booster

Instead of reducing the threshold voltages, the clock voltage booster approach increases the gate-source overdrive, typically achieved by doubling the clock voltage applied to the gate of an NMOS floating switch. A commonly used boosting circuit by Nakagome *et al.* [15] is shown in Figure 3.2. By applying an input clock signal with a swing of V_{DD}, the capacitors C_1 and C_2 are alternatively charged to V_{DD} through cross-coupled NMOS transistors. When the input signal is low, an inverted clock will pump the voltage at the top plate of C_2 to be near $2V_{DD}$ and PMOS device M1 will turn on to pass the boosted voltage to the gate of the floating (sampling) switch MS. The peak voltage of he boosted clock signal is determined by

$$V_{HI} = 2V_{DD}\frac{C_2}{C_2 + C_p + C_{gate,MS}} \tag{3.1}$$

where C_p is the parasitic capacitance at the top plate node of C_2 and $C_{gate,MS}$ is the gate capacitance of the floating switch MS. To avoid latch-up, the n-well bias of M1 needs to be provided carefully. When the input clock is high, switch M2 pulls down the gate voltage to *GND*.

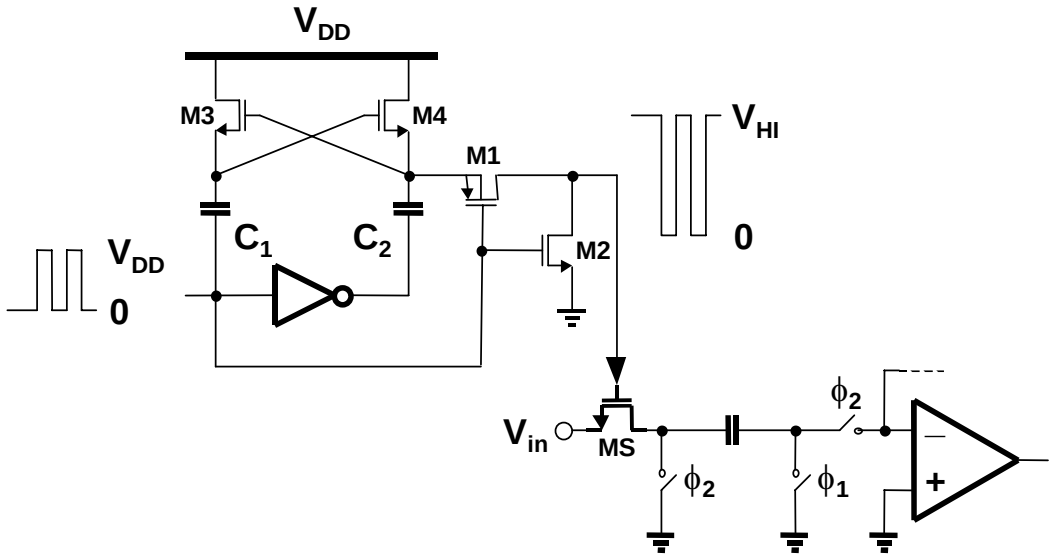


Figure 3.2 Schematic of clock boosting circuit.

The boosting circuit applied to the design of a pipelined ADC was reported in [16]. However, the fine-line width CMOS technologies with thin gate oxide are not intended to tolerate the increased voltage stress ($2V_{DD}$). While the clock voltage booster is effective for higher voltage CMOS processes requiring low-voltage supply, this may no longer be an option for future low-voltage CMOS processes.

3.4 Bootstrapping Circuit

Another scheme offering an elegant solution to the low-voltage switch problem is using the bootstrapped circuit [17]-[19]. Its conceptual operation is illustrated in Figure 3.3. During the

off phase, the switch is tuned off by grounding the gate. Simultaneously the capacitor, which acts as the battery, is charged to the supply voltage. During the on state, the capacitor is switched across the gate and source of the device. Since the capacitor is precharged to V_{DD} level, the circuit provides a boosted clock with constant V_{gs} to the switches for all levels of V_{in}.

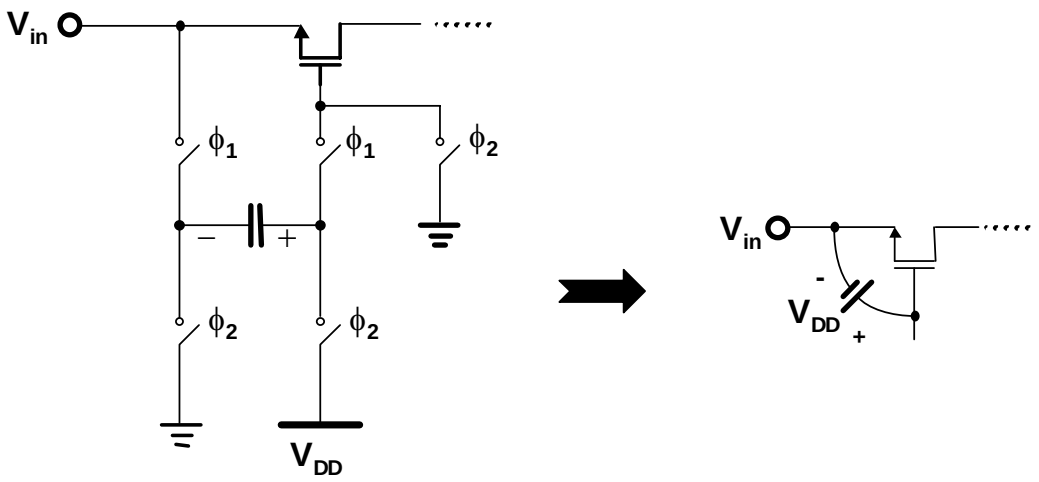


Figure 3.3 Conceptual diagram of bootstrapping circuit.

Figure 3.4 shows the actual bootstrapping circuit reported in [17]. The circuit operates with a single-phase clock (Φ_1) that controls the floating switch. During the off phase, Φ_1 is low due to discharging via M7 and M10. At the same time, V_{DD} is applied across the capacitor C_3 by M3 and M12. This capacitor will act as a battery across the gate and source. Device M8 and M9 isolate the floating switch from C_3 while it is being charged. When Φ_1 goes high, M5 pulls down the gate of M8, allowing charge from the battery capacitor C_3 to flow onto the gate of the floating switch. This turns on both M9 and M11. M9 enables the gate to track the input signal shifted by V_{DD}, keeping the gate-source voltage constant regardless of the input signal. Because the body (nwell) of M8 is tied to its source, latch-up is suppressed. Two devices are not functionally

necessary but improve circuit reliability. Device M7 keeps V_{ds} and V_{gs} of M10 within V_{DD} level when M8 is on. The channel length of M7 should be made long to prevent punch-through effect. Device M13 keeps V_{gs} of M8 from exceeding V_{DD}.

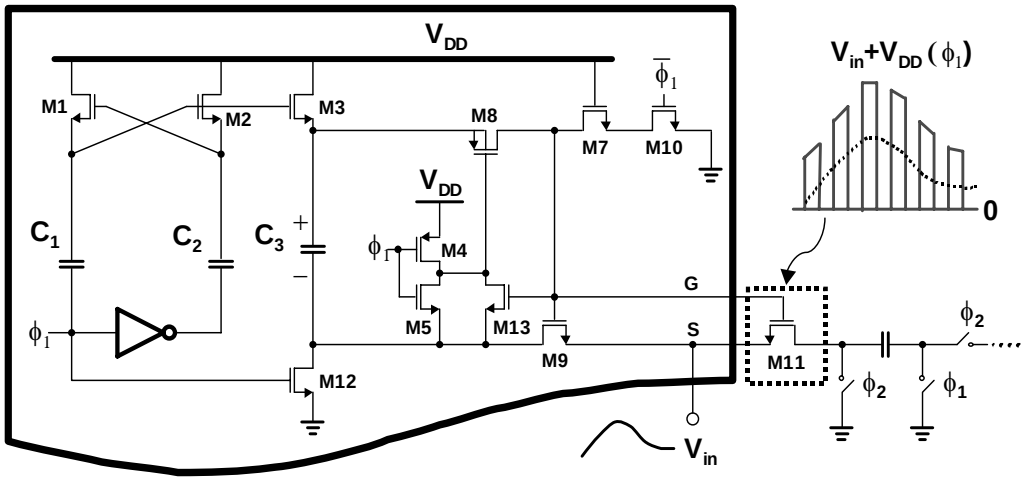


Figure 3.4 Full schematic of bootstrapping circuit.

This approach has an important advantage over the previous ones. Because of the constant on-resistance due to the fixed overdrive voltage, it improves the sampling linearity in high-speed applications. However, there are some drawbacks. Since separate bootstrapping circuits are used for all floating switches, the die area and signal loading increase, which directly leads to increased power consumption and/or speed reduction. The bootstrapped clock also increases switching noise. Moreover, the devices are subjected to large voltage glitches across the gate oxide, which could affect long-term reliability even though the problem is greatly minimized in comparison to clock boosters.

3.5 Switched-Opamp Technique

The approaches described in the above minimize the problem by increasing the conductance of sampling switches. The switched-opamp (SO) technique tackles this problem in a different way [20]-[24]. It eliminates the sampling (floating) switches altogether and connects the input signal (or the signal from the previous stage) directly to the sampling capacitor. The operation from [20] is summarized in Figure 3.5. During Φ_1, the previous stage opamp output is sampled onto the sampling capacitor. During Φ_2, the previous stage opamp is turned off to provide a high impedance output, and that node is connected to a fixed reference (e.g. *GND*).

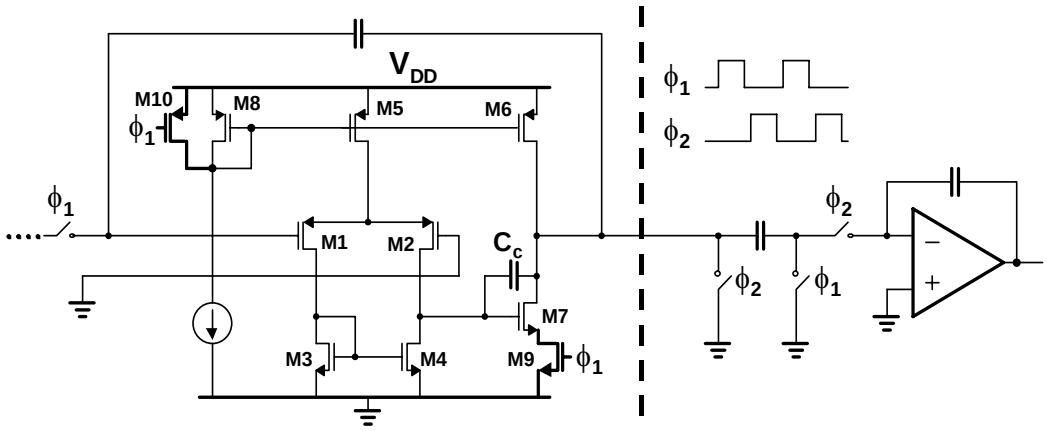


Figure 3.5 Switched-opamp technique.

A switched opamp, shown in Figure 3.5, is a Miller-compensated amplifier with two added switches. The opamp is turned on and off by means of its bias current. In the off state, device M10 pulls the V_{gs} of top current mirrors to zero. Device M9 is used to interrupt the current path through M7, so that the Miller compensation capacitor C_c will not be discharged. Otherwise, from the off-state to on-state, long time would be needed to recharge C_c.

The SO technique has shown promising performance in low frequency (e.g. audio) applications [20]-[22]. Although high-frequency applications have been attempted [24], accuracy remains limited due to the slow on/off transients.

3.6 Opamp-Reset Switching Technique (ORST)

As demonstrated by the SO circuits, eliminating the floating switches enables true low-voltage operation. However, it would be desirable for the opamps to remain in the active-state during all clock phases to maintain higher operating speed. Here we propose a new low-voltage SC scheme, the *Opamp-Reset Switching Technique* (ORST) [25]. The rudimentary concept of the ORST is depicted in Figure 3.6. After the previous stage output is sampled onto the sampling capacitor (during Φ_1), the sourcing opamp is placed into the unity-gain feedback configuration (during Φ_2) to provide the fixed reset reference. The opamp does not have to enter the off state, as in the SO technique. This enables high-speed operation. As with the SO technique, neither any floating switch is used nor does it require clock boosting or bootstrapping circuits. The ORST is free of any reliability issues and fully compatible with low-voltage submicron CMOS technologies.

While the new scheme is expected to be much faster than the SO technique, two distinctions should be made from the traditional SC circuits. The first distinction is that there are two settling events happening at the same time during Φ_2: the sourcing opamp output settles to *GND* and the amplifying opamp output settles to the desired value. The second distinction is that the output common-mode (i.e. average voltage) should change from *GND* in one phase to approximately the mid-level ($\approx V_{DD}/2$) during the other phase. This results from the inherent pseudo-differential architecture of the ORST that is to be adopted for realistic IC implementations. This will increase the slewing time because the amplifier operates inherently as a single-ended

amplifier. Despite these distinctions, the overall settling time is still much faster than the SO architecture.

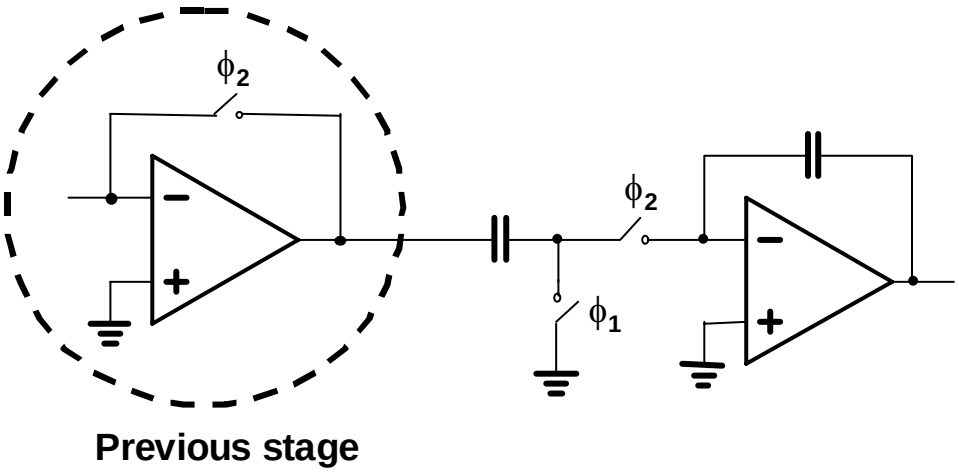


Figure 3.6 Conceptual diagram of opamp-reset switching technique (ORST).

Chapter 4.

High-Speed Data Converter Architectures

Before going through the low-voltage ADC design, this chapter quickly reviews the architectures of high-speed ADC.

4.1 Full Flash Architecture

For video-rate (>10MHz) medium resolution (8-12 bits) applications, there are several different approaches to implement the ADC. Full flash ADC is the most straightforward way as shown in Figure 4.1 [28]-[32]. An N-bit flash ADC consists of a resistor string and 2^N-1 comparators, which evaluate the analog input and generate the digital output as a thermometer code. The codes are then encoded to N-bit Binary or Gray code by encoding circuitry.

Since the converter requires only one clock cycle per conversion, the architecture is the fastest of all the current structure. Because references are made by a resistor string, they are inherently monotonic resulting in good differential linearity.

However, there are several drawbacks in this architecture. Since 2^N-1 comparators are needed in an N-bit ADC, the hardware complexity increases exponentially with resolution. This

implies that power consumption and die area also increase exponentially with the resolution. The second drawback is that the front-end block should drive large capacitance of the comparators, which further increases the total power and aggravate the nonlinearity of the converter due to nonlinear input capacitance [53]. Third, the resistors matching of a resistor string and comparator performance limit the linearity of the flash ADC.

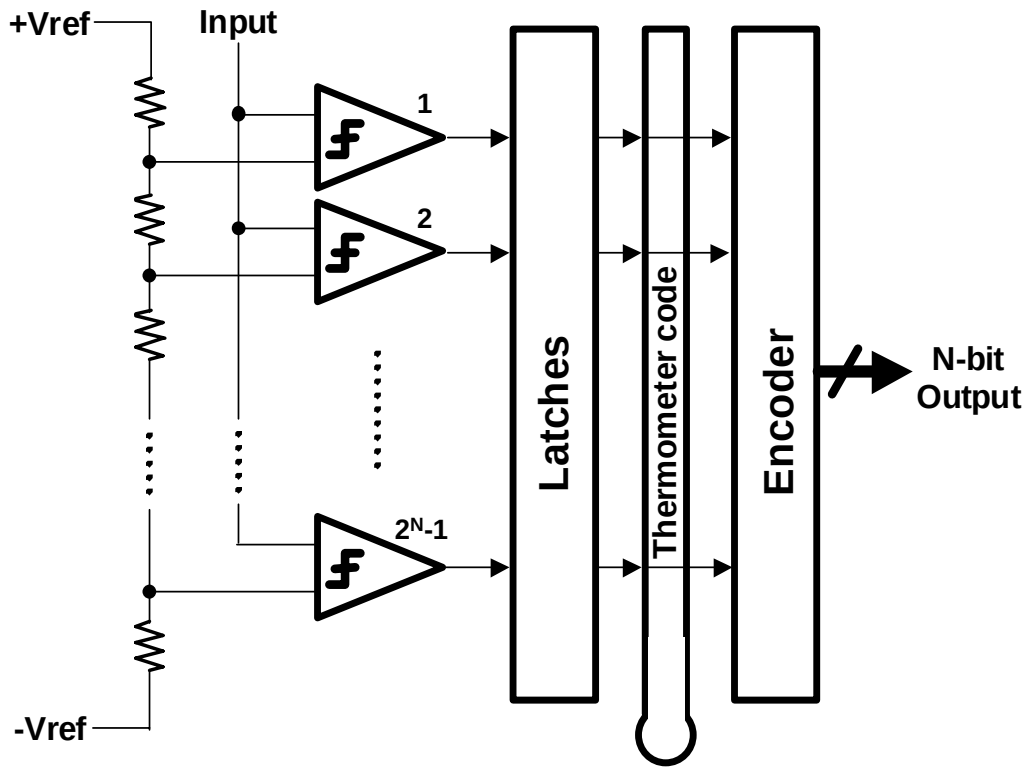


Figure 4.1 Full flash ADC.

In order to have a good matching, three effects should be considered to have an impact on relative accuracy: geometry (which is determined by shape), width, and length, resulting in local mismatch, gradients of sheet resistance, and variations in the polysilicon-metal contacts. Better matching can be obtained by using unit resistor element with increased width and length. This is

because most of the randomness stems from the perimeter due to lithography. The gradients of the sheet resistance can be first order cancelled by cross-coupled layout [33]. Contact resistance also becomes an important factor to achieve a good matching in a low resistor string in high-resolution converters.

There are three important factors in comparator performance, which are input offset, kickback noise, and sparkle (or bubble) error. The sparkle error results from the lack of a sample-and-hold amplifier with a fast-varying input signal. It can be resolved with a digital correction logic [28]-[29]. Kickback noise generally corrupts sampling of the analog input signal. The general solution to suppress it is adding a preamplifier before the latched-comparator. Comparator input offsets can be reduced by numerous offset cancellation techniques [34].

4.2 Two-Step Architecture

A 2N-bit two-step flash ADC is illustrated in Figure 4.2 [4], [35], [36]. It needs three clock cycles for conversion. In the first clock phase, an analog input is sampled and held by an S/H block. In the second clock phase, the held voltage is converted by N/N+1 flash sub-ADC. These coarse N bits are stored in the digital correction logic, and an analog voltage corresponding to the coarse N bits is generated by an N-bit sub-DAC. In the third phase, a residue voltage, which is the voltage difference between the held input and the output of the DAC, is amplified by 2^N. This time fine (N+1) bits are determined by the same sub-ADC, which is over-ranged by one extra bit to correct an error, generated in the previous coarse decision.

The main advantage over flash converters is that there is significant reduction in area, power consumption and input capacitance compared with those for the flash converters. However, there are several disadvantages. The two-step ADC requires a DAC whose linearity should be better than N bits. It also requires a residue amplifier, which can be the major speed bottleneck. In

addition, the conversion time is longer than a flash ADC because the two-step ADC has to wait until the residue signal is settled and quantized.

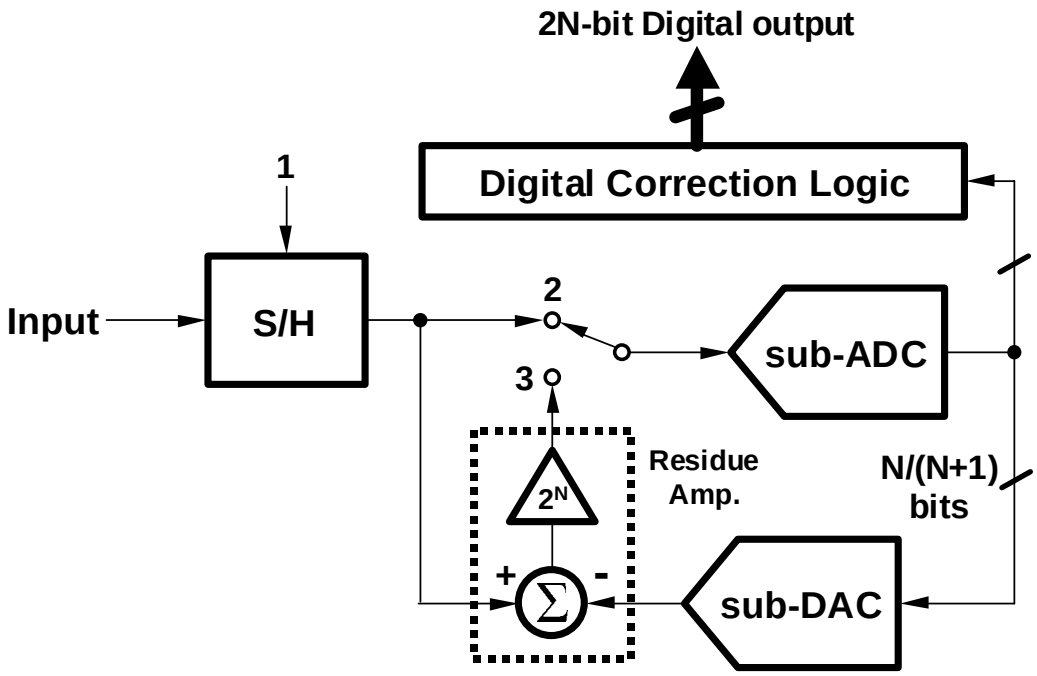


Figure 4.2 Two-step ADC.

4.3 Pipeline Architecture

The pipelined architecture as shown in Figure 4.3 consists cascaded conversion stages. Each stage carries out a conversion mechanism similar to that of two-step converters. An analog input (or the previous residue voltage) is sampled by the S/H block. An n-bit sub-ADC generates digital output based on the sampled data. The digital output is transferred to the sub-DAC makes quantized analog output. The analog signal is subtracted from the sampled input signal to generate residue voltage, which is then amplified by 2^n. The next stage performs the same A/D conversion

with this voltage. Because the input of a stage is the output of the previous stage, it is called pipelined converter.

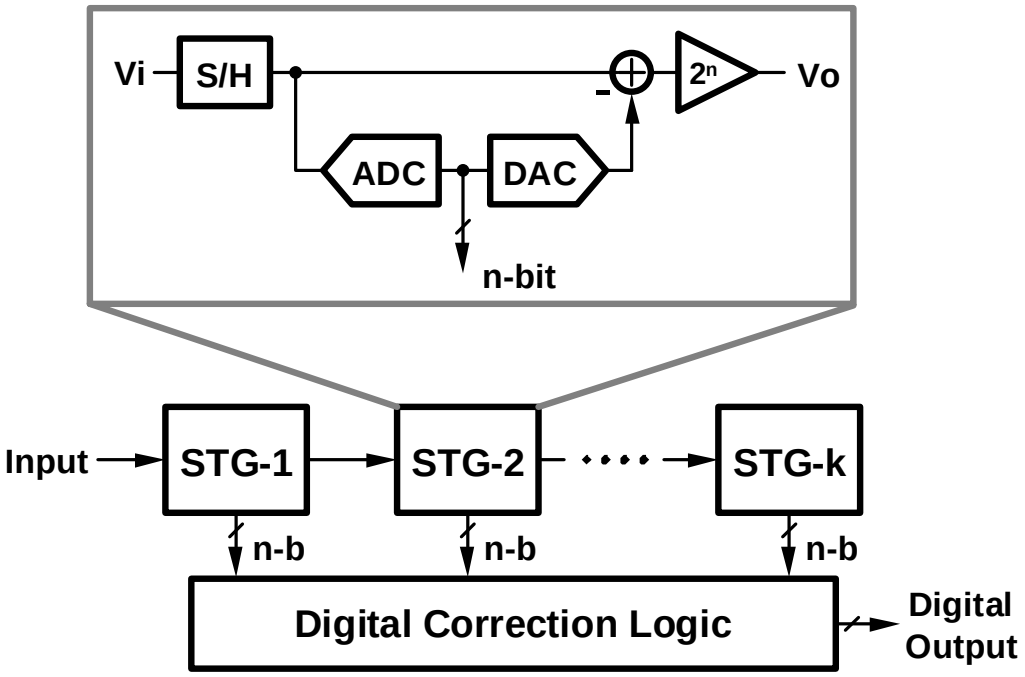


Figure 4.3 Pipelined ADC.

The primary advantage of the architecture is its high throughput rate due to concurrent operation of the stages. Limiting factors of the conversion rate are front-end input sampling and interstage gain amplifier. Compared to the basic full flash ADC, chip area and power dissipation are dramatically reduced. This is because the number of components increases linearly rather than exponentially. However, interstage signal transfer and sub-DAC linearity decide the overall ADC performance. Recently, various correction and calibration techniques are reported to obtain high resolution. To increase the conversion speed, a multi-channel time-interleaved architecture is widely used these days [37]-[38].

Chapter 5.

Low-Voltage Pipelined ADC Design

The *Opamp-Reset Switching Technique* (ORST) topology that does not use clock boosting, bootstrapping, switched-opamp (SO), or threshold voltage scaling is employed in a 1.4V 10-bit 25MSPS pipelined ADC as a low-voltage circuit design example. The detailed low-voltage circuit implementation is described in this Chapter. The prototype ADC was fabricated in a 0.35-μm CMOS process.

5.1 1.5-Bit-per-Stage Architecture

The block diagram of a 10-bit 1.5-bit-per-stage pipelined ADC is shown in Figure 5.1. The ADC consists of 9 cascaded stages with a front-end input sampling circuit. The stages 1 through 8 are identical, each of which is composed of comparators (flash ADC) and a MDAC merging the sub-DAC and the residue amplifier operations. Each stage employs a 3-level DAC, results in the residue transfer function as

$$V_O = \begin{cases} 2V_i - V_{ref} & (V_i > \frac{V_{ref}}{4}) \quad D_{out} = (10)_2 \\ 2V_i & (-\frac{V_{ref}}{4} \le V_i \le \frac{V_{ref}}{4}) \quad D_{out} = (01)_2 \\ 2V_i + V_{ref} & (V_i < -\frac{V_{ref}}{4}) \quad D_{out} = (00)_2 \end{cases} \tag{5.1}$$

Depending on the sub-ADC output (D_{out}), $\pm V_{ref}$ or 0 is subtracted from the input. Figure 5.2 shows the conceptual block diagram of each pipeline stage [26]. The sub-ADC of each stage performs coarse 1.5-bit quantization (3 levels) while the last stage (9^{th} stage) generates true 2-bit output (4 levels).

$$D_{out} = \begin{cases} V_i > \frac{3V_{ref}}{4} & D_{out} = (11)_2 \\ \frac{V_{ref}}{4} < V_i \le \frac{3V_{ref}}{4} & D_{out} = (10)_2 \\ -\frac{V_{ref}}{4} \le V_i \le \frac{V_{ref}}{4} & D_{out} = (01)_2 \\ V_i < -\frac{V_{ref}}{4} & D_{out} = (00)_2 \end{cases} \tag{5.2}$$

The digital correction is done by adding up the 2-bit raw code from each stage with 1-bit overlap. It relaxes the offset requirements of the comparators and the opamps (of the MDACs). In the prototype IC implementation, the proposed ORST is applied to the input sampling circuit as well as the MDACs. A detailed circuit implementation will be described in the following Section.

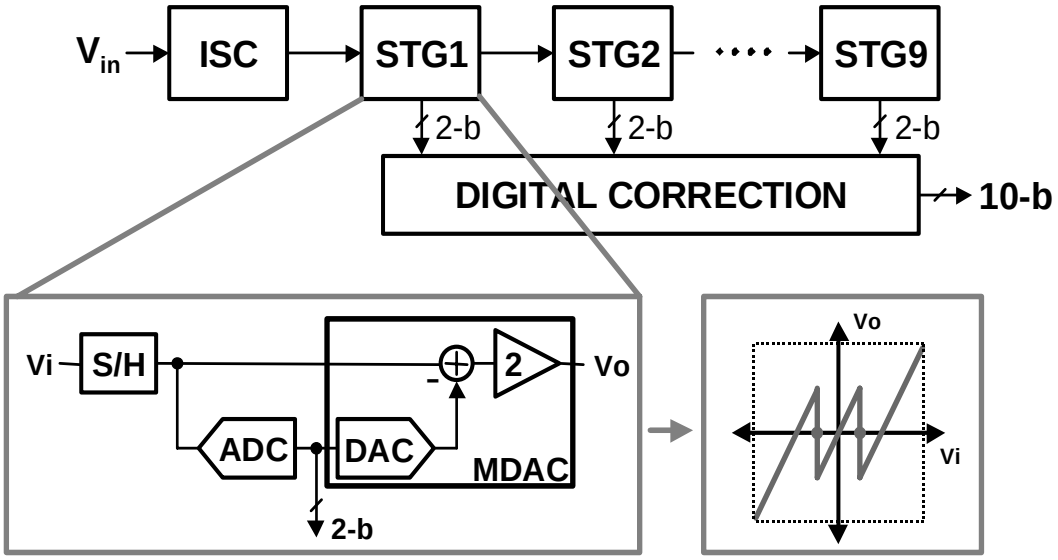


Figure 5.1 Block diagram of a 10-bit 1.5bit/stage pipelined ADC.

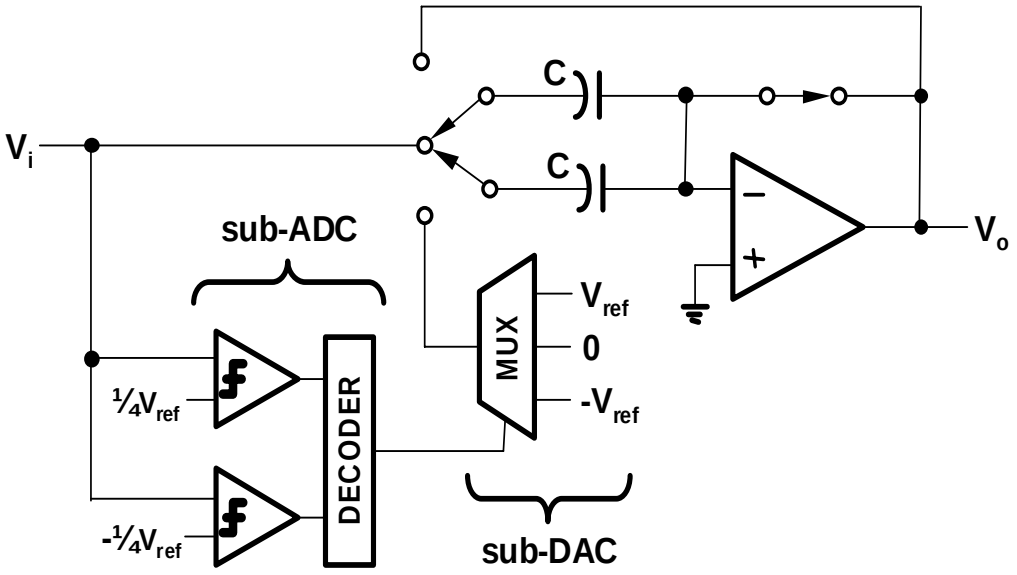


Figure 5.2 Implementation of 1.5-bit pipeline stage.

There are several reasons for choosing 1.5-bit/stage architecture for the low-voltage ADC design. In the MDAC with the ORST, the opamp is in the unity-gain reset mode during one of the clock phases. Therefore, the feedback factors during the amplification phase and the reset phase should be comparable to maintain similar settling dynamics. If the feedback factors were drastically different, the opamp would have to be over-compensated to cover a wide range of loop bandwidths, which would end up being an unnecessary burden on the SC circuit design. The MDACs with a gain of two proved to be a simpler choice in this regard. Another reason for choosing the 1.5-bit/stage architecture was that under very low-voltage and small dynamic range conditions, the digital correction/redundancy range needed to be maximized to relax the comparator and opamp offset accuracy requirements.

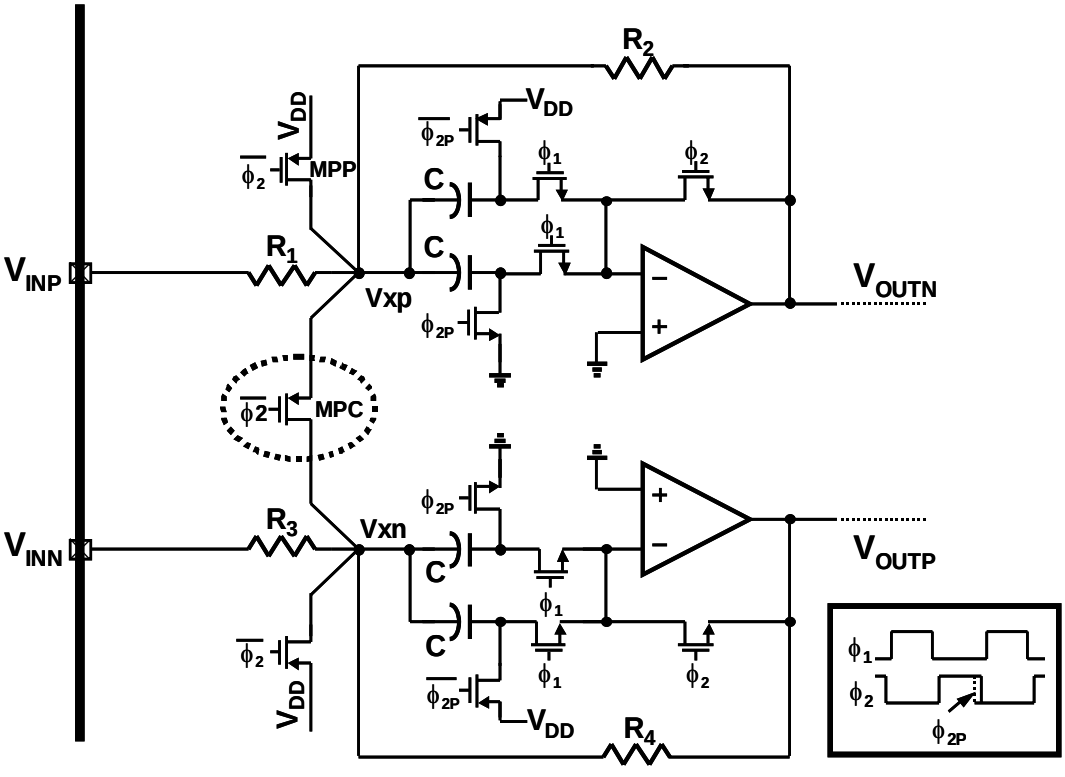


Figure 5.3 Low-voltage input sampling circuit.

5.2 Building Block Implementation

This Section shows the detailed implementation of each building block in the pipelined ADC. Low-voltage issues are discussed with previous works. To emphasize the voltage *potentia*l, the reference voltages are expressed as V_{DD} (=V_{ref}) and *GND* (=-V_{ref}), respectively. In the actual IC implementation, these reference voltages represent the nodes that are connected separately to a set of quiet voltage references.

5.2.1 Input Sampling Circuit

Another major challenge in the low-voltage ADC design is to sample/transfer the input signal fast and accurately from sources external to the IC. One such circuit exists in the context of the switched-opamp technique [27]. Figure 5.3 shows the modified version of the circuit. The modifications include using a pseudo-differential configuration and the ORST. This circuit provides the tracking signal (inverted) of the input to the first stage MDAC during one clock phase and the reset signal during the other phase. The inverting unit gain of the tracking signal is obtained from a one-to-one resistor ratio. During the reset phase (Φ_2), V_{xp} is pulled up to V_{DD} while level-shifting capacitors *C* are precharged to V_{DD} and *GND*. During the amplification phase (Φ_1), V_{xp} becomes $V_{DD}/2$ (=V_{batt}) due to the charge sharing between C_1 and C_2. Assuming that the input common-mode voltage is $V_{DD}/2$, the output common-mode voltage also becomes $V_{DD}/2$ because of the equivalent function of an intermediate virtual ground V_{xp} (V_{xn}).

During the reset phase, the resistance of the PMOS switch MPP is

$$R_{MPP}=\frac{1}{\beta[(V_{SG}-|V_{th}|)-V_{SD}]} \tag{5.3}$$

where $\beta=\mu_p C_{ox}(W/L)$. The body effect is ignored for simplicity. The voltage division between linear R_1 and nonlinear R_{MPP} introduce nonlinear voltage fluctuation at Vxp:

$$V_{xp} = \left(\frac{R_{MPP}}{R_1 + R_{MPP}} \right) V_{INP} + \left(\frac{R_1}{R_1 + R_{MPP}} \right) V_{DD} \tag{5.4}$$

The level-shifting voltage V_{batt} is a function of V_{xp} and V_{OUTN} is a function of V_{batt}. Assuming that the opamps have finite but linear open-loop gain A, those voltages are given by

$$V_{batt} = \frac{V_{xp}(C_1 + C_2) - (C_1 V_{DD} + C_1 GND)}{C_1 + C_2} \tag{5.5}$$

and

$$V_{OUTN} = \left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1} \right) \right)^{-1} \cdot \left(\left(1 + \frac{R_2}{R_1} \right) V_{batt} - \left(\frac{R_2}{R_1} \right) V_{INP} \right) \tag{5.6}$$

Because of nonlinear voltage fluctuation at V_{xp}, output distortion results. This nonlinear behavior will be discussed intensively in the following Chapter.

The operational amplifier used in the input sampling circuit is the most important part to determine the speed and accuracy performance of the converter. The opamp used in is shown in Figure 5.4. It is a differential input and single-ended output two-stage amplifier with Miller compensation. The input stage is a modified folded cascode for low voltage and high dc gain. The second inverting stage consists of M10 and M11 to achieve high signal swing. C_C and R_Z make up the standard Miller-compensation. During output reset phase, the input of the opamp is set to 0.25V, rather than *GND*, around V_{dsat} of device M11. Such that when the opamp is configured as an unity-gain buffer output device M11 will not be out of saturation. The supply should be greater than $V_{dsat5} + V_{th,P} + V_{dsat1} + V_{dsat3}$.

There are several reasons for using PMOS input pair: 1) If NMOS input pair is used, the input voltage is biased around V_{DD} level and most of switches need to be made of PMOS device. This will increase parasitic capacitance and charge injection error at signal nodes. 2) The bandwidth of the opamp is limited by second pole associated with g_m of M11. Second pole needs

to be about three times larger than unity-gain bandwidth to achieve good enough phase margin. Since the first stage input device is PMOS and the second stage input device is NMOS, they can have the same device size. 3) PMOS input transistors can be put into n-well to reduce the body effect and substrate noise. 4) PMOS devices have lower 1/f noise. The opamp in Figure 5.4 has the dc gain of 72dB and unity-gain bandwidth of 180MHz. It is also used in all MDAC blocks as well.

In the transient response, there is a peaking, which degrades the settling behavior. Extensive simulation shows that the peaking is proportional to gate-drain parasitic capacitance of M10. Large signal swing at the output is coupled to the BIAS1 via the parasitic capacitance and attenuated by a capacitance division between C_{gd} and total capacitance at BIAS1 node. In this work, C_b, which is a 100pF MOS capacitor, is used as a decoupling capacitor. This phenomenon is suspected to happen only in a single-ended structure.

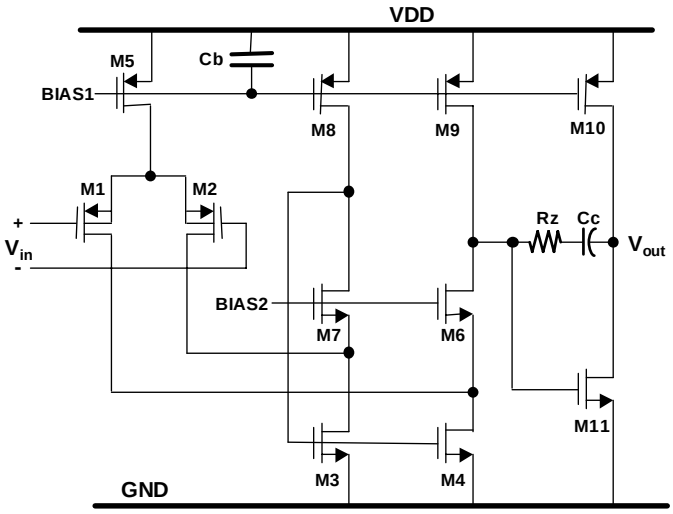


Figure 5.4 Schematic of a low-voltage two-stage Miller-compensated opamp.

5.2.2 MDAC

The simplified schematic of the proposed MDAC is shown in Figure 5.5. A pseudo-differential architecture, which has two single-ended opamps working in parallel, is employed. Fig. 5.6 shows the detailed operations during each of the two clock phases. During the sampling

phase, the opamp is placed in the unity-gain reset configuration while C_S samples the previous stage (sourcing opamp) output. The capacitors C_{M1} and C_{M2} are effectively shorted during this phase. The operation of these capacitors as common-mode feedback (CMFB) will be described in the discussion of the amplification phase that will follow. Due to low-voltage operation, $\pm V_{ref}$ sampling cannot be incorporated into the signal path as with the conventional *capacitor flip-over* architecture [26]. Therefore, extra capacitors (C_R) are added to provide the reference injection. Since all switches are to be connected to either V_{DD} or *GND* level, the desired reference voltage, less than V_{DD}, is generated by a capacitor ratio. The capacitor ratio of 8:1 is used in this design. This effectively provides the references $\pm V_{DD}/4$ for the full-scale signal range that is V_{DD} peak-to-peak differential. During the amplification phase, C_R is connected to either node P or N depending on the sub-ADC decision. The previous/sourcing stage provides the reset level during this phase. If the pseudo-differential architecture is employed without an effective CMFB circuit (C_{M1} and C_{M2} as shown), any common-mode voltage errors entering the cascaded stages would accumulate with multiplication as these errors are multiplied by the same 2x gain of the MDAC. This is because the pseudo-differential configuration inherently does a single-ended operation, resulting in a common-mode gain that is same as the differential gain. Building a traditional CMFB circuit to alleviate this common-mode accumulation problem under such low voltage headroom while using no floating switches is a challenging task. Such CMFB designs result in relatively inefficient realizations, taking up unwanted amount of chip area and power consumption. In this work, we get around the problem of adding a traditional CMFB circuit by introducing a mild amount of positive feedback with C_{M2}. This configuration realizes the required differential gain

$$A_{DIFF} = \frac{C_S}{C_{M1} - C_{M2}} = 2 \tag{5.7}$$

while allowing a common-mode gain

$$A_{CM} = \frac{C_S}{C_{M1} + C_{M2}} = 1 \tag{5.8}$$

Eq. (5.7) and (5.8) came from the assumption that the dc gain of the opamp is infinite. The common-mode errors will now stay unchanged without experiencing the 2x multiplication at each MDAC stage. Thus, the common-mode is controlled and retained throughout the stages without the addition of complex CMFB circuitry.

To achieve the desired resolution, linearity, and SNR, each converting stage should be insensitive to non-ideal effects such as capacitor mismatch, opamp gain and settling error, offset error, charge injection/feedthrough error, thermal noise and so on.

In the pipeline architecture, the accuracy requirement for each stage is different. The first stage has the most strict accuracy requirement that determines the overall performance. For the following stages, it becomes more relaxed because MSBs are already resolved by the previous stages and they need to be only as accurate as the remaining bits. Assuming that the dc gain of the opamp is *A*, for the circuit shown in figure 5.5, the performance is described by the following equations:

$$V_o = G_{DIFF}\left(1 - e^{(-t/\tau)}\right)\left(V_i - 2\frac{C_R}{C_S} D \cdot V_{ref}\right) \tag{5.9}$$

$$G_{DIFF} = \frac{C_S}{C_{M1} - C_{M2} + \dfrac{C_{M1} + C_{M2} + C_R + C_S}{A}} \tag{5.10}$$

$$\tau = \frac{1}{\omega_{CL}} = \frac{1}{\omega_{unity} f} \tag{5.11}$$

$$f = \frac{C_{M1} - C_{M2}}{C_{M1} + C_{M2} + C_R + C_S} \tag{5.12}$$

V_{ref} is set to be V_{DD}, D is the sub-ADC's encoded digital output, which has the value of ±1 and 0. A is the finite dc gain of the opamp, f is a feedback factor, and G_{DIFF} is the differential gain. For a 10-bit resolution, the capacitor matching errors between C_S : (C_{M1}-C_{M2}) and C_S : C_R in the first stage must be better than 0.1%. The unit size capacitor (=C) here is 200fF. The error term exp(-t/τ) in Eq. (5.9) is determined by the settling behavior of the opamp as long as the on-resistance of switches are small enough to be ignored. To achieve 10-bit resolution, the total allowed settling time should be less than 6.9τ. Since 25MHz clock is used for sampling, the output should be settled within 20ns with more than 10-bit accuracy. Feedback factor f in this work is 0.25. These lead to the conclusion that the unity gain bandwidth should be about 200MHz. This value is used to set the bias condition and sizing of the opamp.

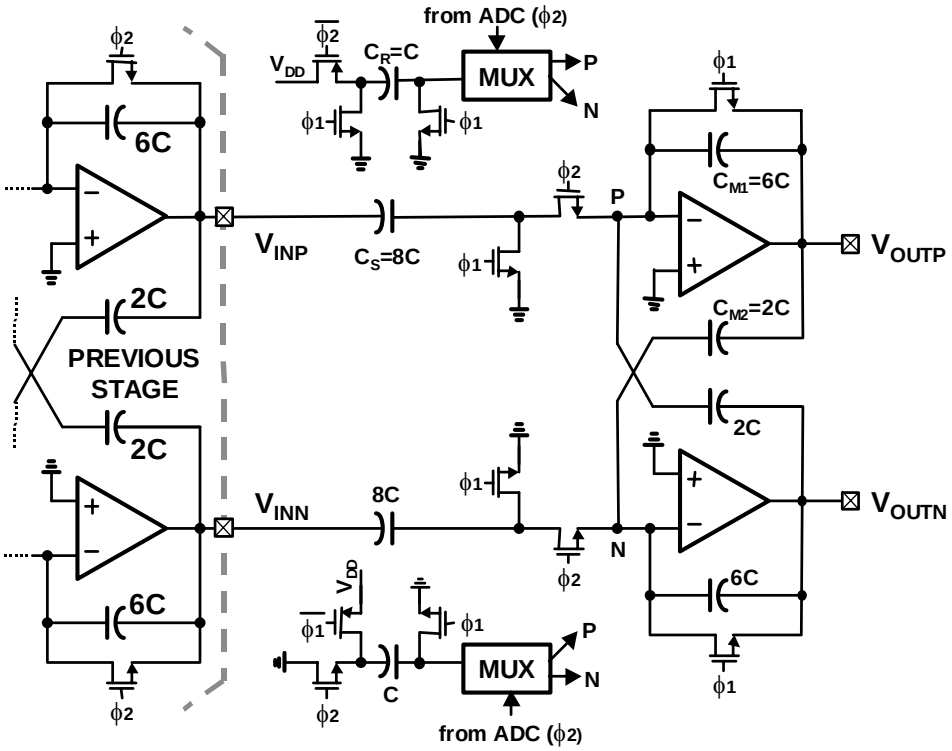
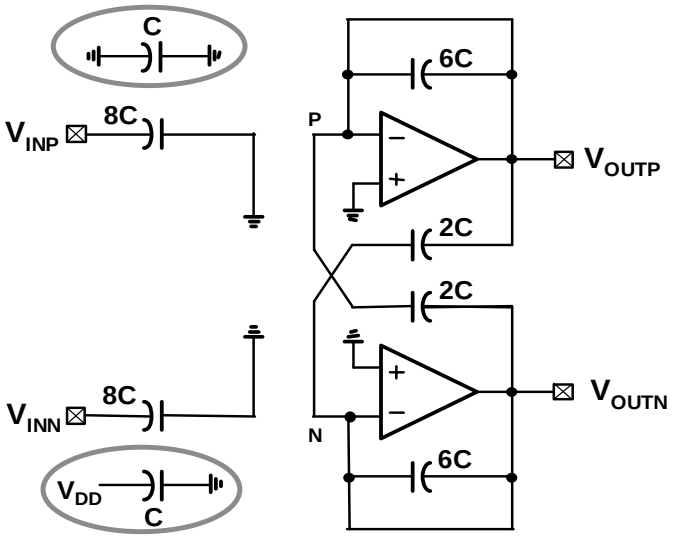
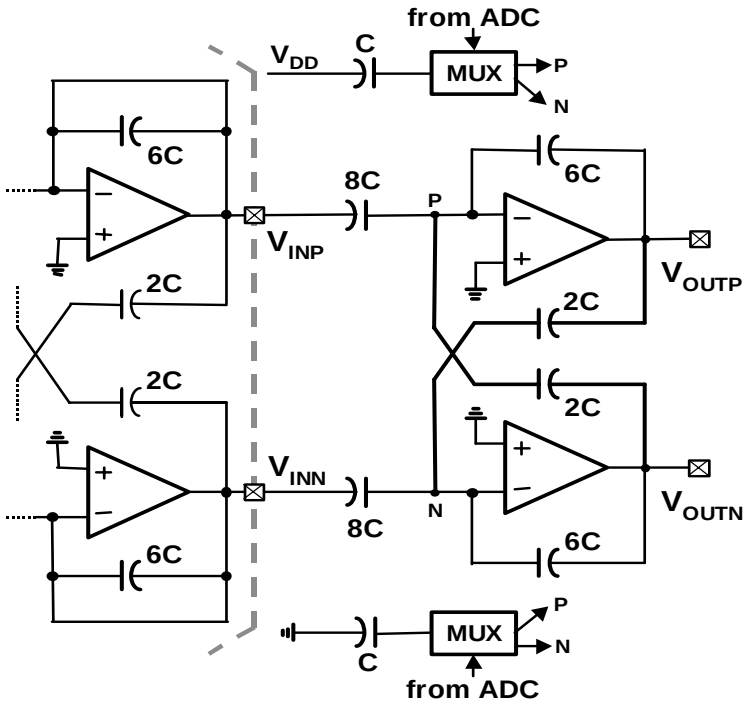


Figure 5.5 Simplified schematic of a low-voltage psuedo-differential MDAC.



(a)



(b)

Figure 5.6 MDAC operations: (a) sampling phase and (b) amplifying phase.

5.2.3 Sub-ADC

The fully differential comparator used in the flash sub-ADCs is shown in Fig. 5.7. In order to avoid using floating switches, the effective $V_{ref}/4$ is provided by a separate capacitor branch C_R similar to the MDAC implementation. The additional capacitor branch C_C effectively provides level shifting and voltage division to ensure that comparator input nodes T_1 and T_2 (gates of NMOS differential-pair) remain equal to or below V_{DD} level in all conditions. The resulting input common-mode voltage is

$$V_{XP} = \frac{R_{MPP}}{R_1 + R_{MPP}}$$

$$= \left(\frac{R_{MPP}}{R_1 + R_{MPP}} \right) V_{INP} + \left(\frac{R_1}{R_1 + R_{MPP}} \right) V_{DD} \tag{5.13}$$

The schematic of the comparator is shown in Figure 5.8. It is composed of a preamplifier with a gain of 10 and a latched-comparator. M4 and M5 in the preamplifier are operating in triode region (as linear resistors) to achieve appropriate dc gain. One important factor in designing a regenerative (positive-feedback) latched comparator, which is composed of M6, M7, and M8, is metastability [53]. When the input signal is small enough, the comparator output strays in mid level rather than generating either high or low level within the allotted time slot. This is a probabilistic function because the difference between the input signal and the reference is a random variable. When the input of the comparator (potential difference between gates of M6 and M7) is V_{XY0}, the time duration to have the output voltage of V_{XY1} can be defined as

$$T = \frac{\tau_o}{A_o - 1} \ln \frac{V_{XY1}}{V_{XY0}} \tag{5.14}$$

The comparator is assumed to have a single pole, a gain $-A_0$, and a time constant τ_0. From Eq. (5.14), T increases with a small input signal. If the circuit has small dc gain or large time constant, it will face the metastability problem.

Assuming that the clock period is $2Tc$, the comparator generates output V_{XY1} from a small input signal within Tc. The input voltage V_{XY0}, which puts comparator into a metastable state, is a random variable. Assuming V_{XY0} has output with uniform distribution between $-V_{XY1}$ and V_{XY1}, the probability of a metastable event is

$$P(T>T_c) = \exp\frac{-(A_o-1)T_c}{\tau_o} \tag{5.15}$$

For the comparator to be free from metastable state, a careful design to give a small regeneration time constant $\tau_o/(A_o-1)$ is very important.

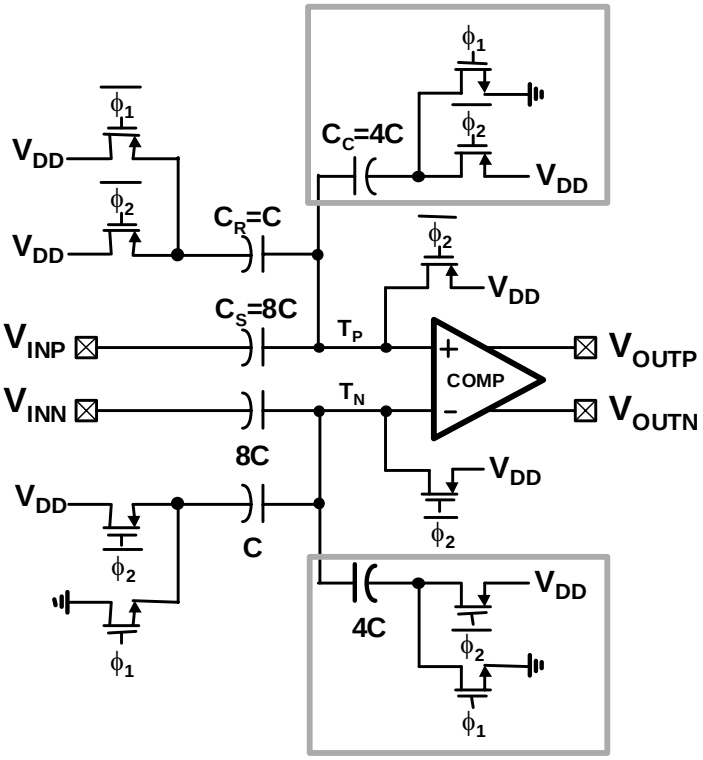


Figure 5.7 Low-voltage comparator with input common-mode level shifting.

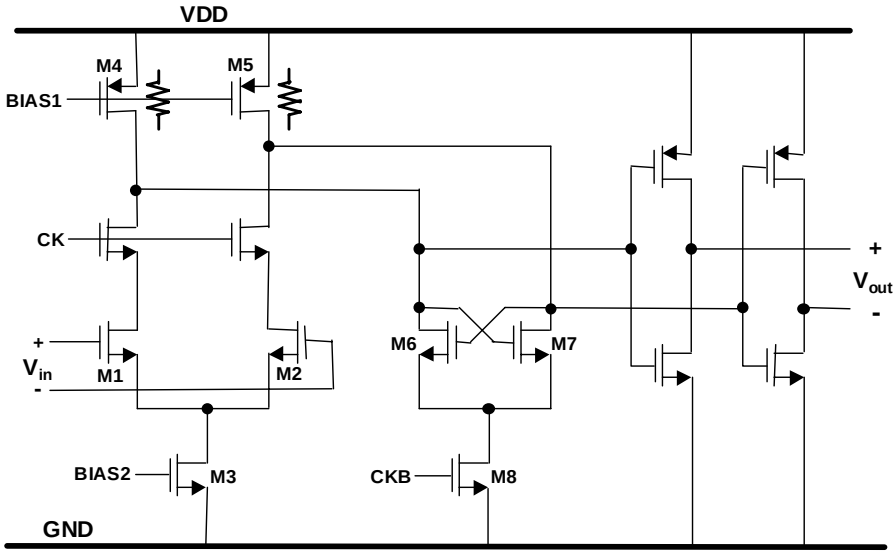


Figure 5.8 Pre-amplifier and latch in comparator.

5.3 Measurement Results

A prototype ADC, incorporating the circuit details described in the previous sections, was implemented in a 0.35-μm CMOS technology where PMOS and NMOS thresholds are -0.9V and 0.7V, respectively. The die photograph is shown in Figure 5.9. The active die area is 1.6 x 1.4 mm^2. All analog building blocks including opamps and capacitors are concentrated at the center part of the chip while the comparators and digital blocks are along the perimeter. All measurements were obtained with a 1.4V single power supply.

The prototype was first characterized with a code density test for differential nonlinearity (DNL) and integral nonlinearity (INL) as shown in Figure 5.10. The resulting code density histogram was obtained for a 25MSPS sampling rate with a full-scale 140kHz sinusoidal input. A total of 2^{15} samples were collected (same for the dynamic measurements). Peak DNL and INL errors are 0.9LSB and 3.3LSB, respectively. Large INL jumps can be seen at + and – $V_{ref}/4$ which are suspected to be coming from poorly matched capacitors at the first stage MDAC. This poor

matching characteristic can also be found in the dynamic measurements of Figure 5.11. This measurement was obtained with a 1MHz input signal. The spurious-free dynamic range (SFDR) with respect to the full-scale input remains relatively fixed despite the different input signal level. This also implies that the front-end input sampling circuit performs well above this SFDR. Figure 5.12 shows that the peak SNR and signal-to-noise and distortion ratio (SNDR) are 55dB and 48dB, respectively. The total power consumption (analog and digital), excluding the digital output pad drivers, is 21mW. The ADC operates at a maximum speed of 32MSPS and a minimum supply voltage of 1.3V. Table 5.1 summarizes the measured performance of the ADC.

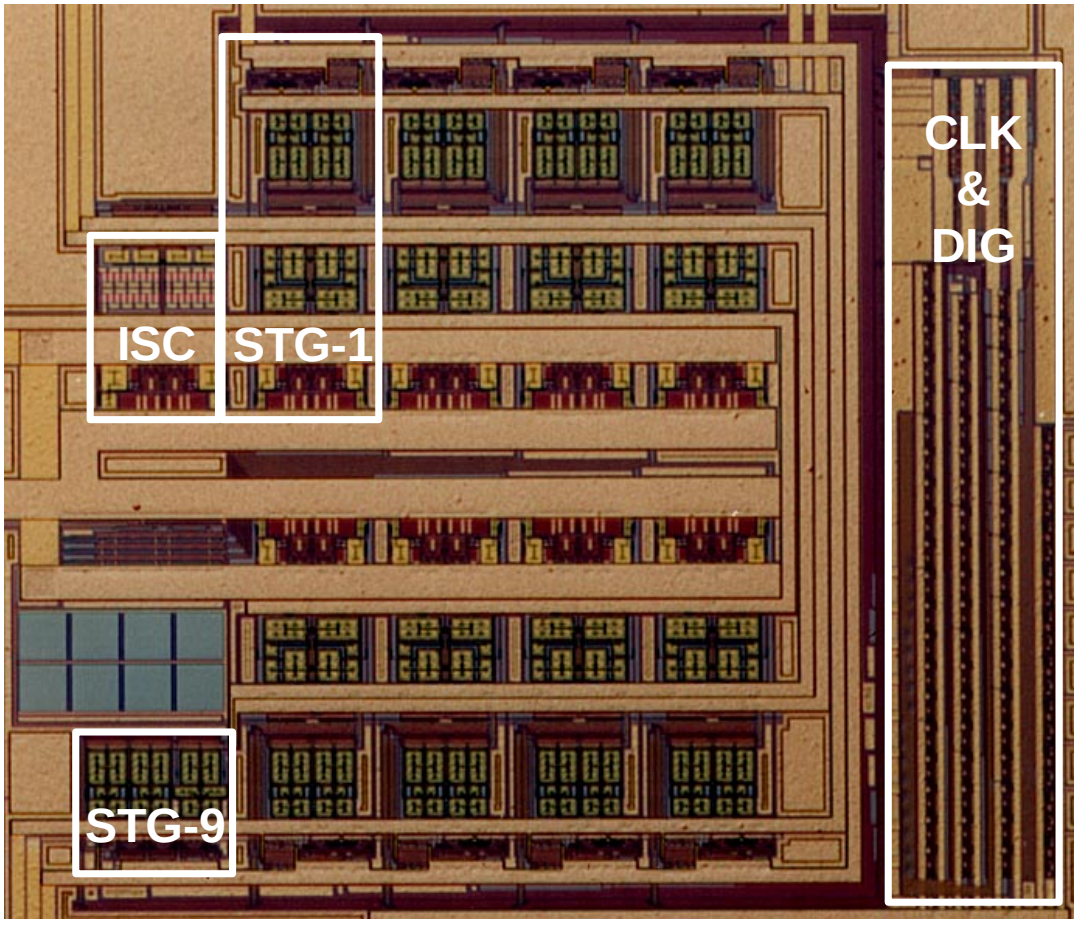


Figure 5.9 Die photograph of the prototype pipelined ADC.

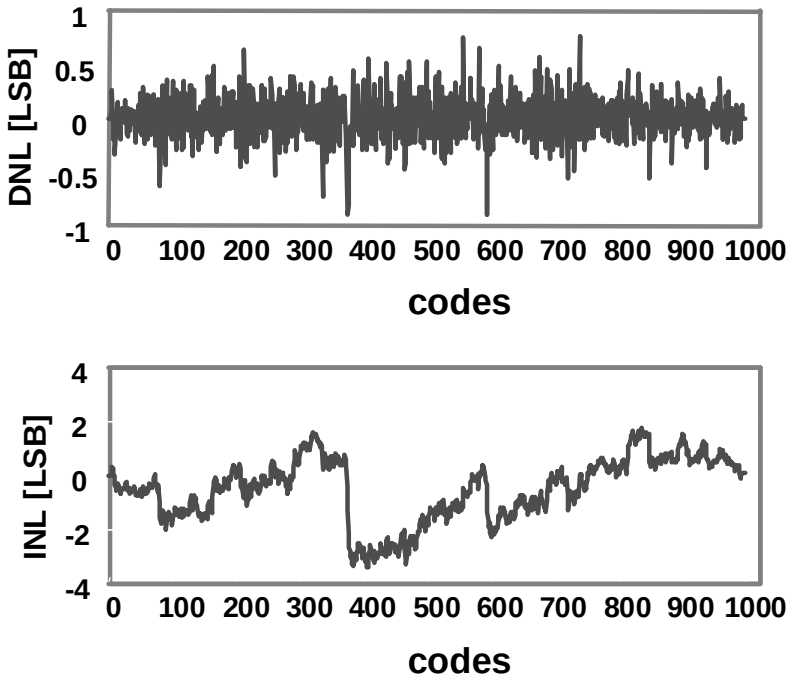


Figure 5.10 DNL and INL.

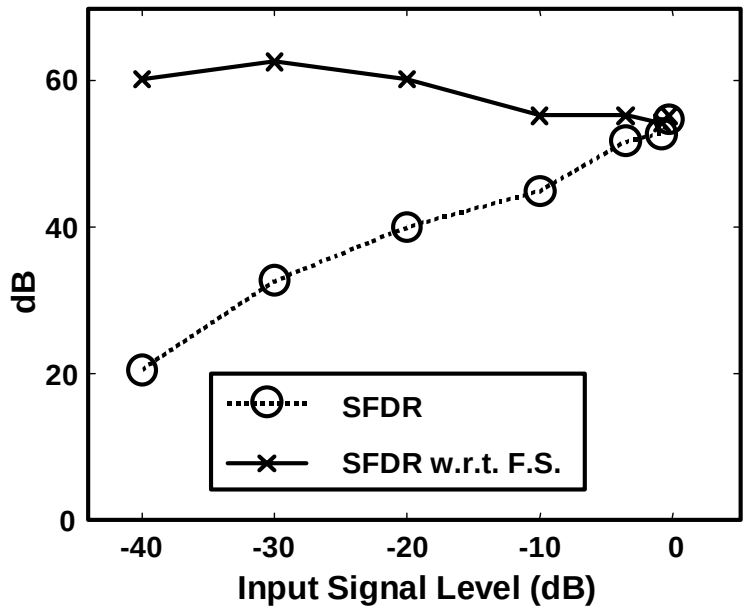


Figure 5.11 SFDR vs. input signal level.

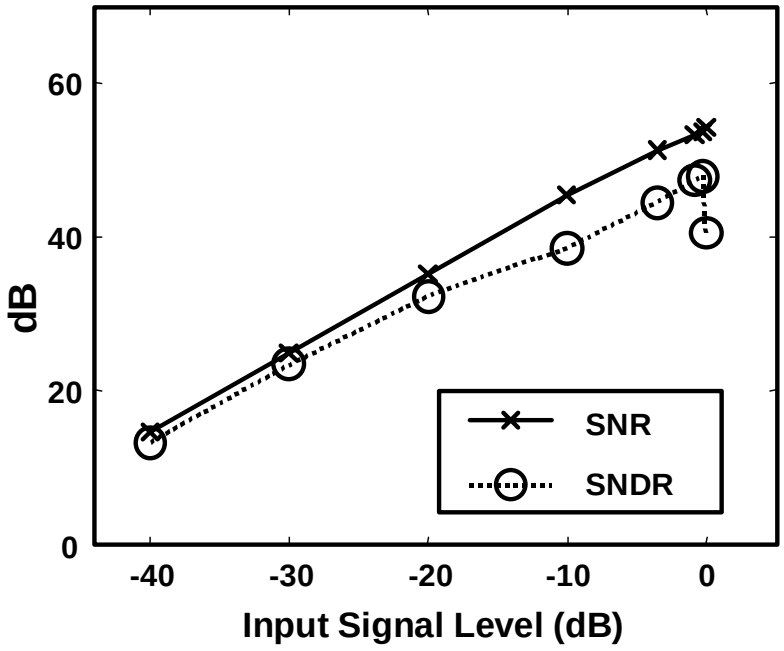


Figure 5.12 Dynamic performance vs. input signal level.

Technology	**0.35-μm CMOS**
Resolution	**10-bit**
Active die area	**1.6 x 1.4 mm^2**
Supply voltage	**1.4V (min. 1.3V)**
Conversion rate	**25MSPS (max. 32MSPS)**
Power consumption	**21mW**
DNL / INL	**0.9LSB / 3.3LSB**
SNR / SNDR / SFDR	**55dB / 48dB / 55dB**

Table 5.1 Performance summary of the pipelined ADC.

Chapter 6.

A 0.9V Calibrated Two-Stage Algorithmic ADC

6.1 Introduction

The increasing demand for high-resolution ADCs has stimulated many innovative design solutions to overcome the finite accuracy set by analog building blocks. Self-calibration techniques have been developed to fulfill the requirements in modern systems such as wireless and wired communication, imaging, and medical instrumentation. In general, ADC calibration techniques can be categorized into three parts: in analog-domain (including circuit level linearity enhancement techniques) [40]-[48], in digital-domain [4]-[10], and physical trimming of internal capacitors [49]-[51]. Analog-domain techniques usually require additional circuitry such as opamps and calibration digital-to-analog converters (DACs). Sometimes they need extra clock phases to do the job. All these imply slow conversion speed and increased power consumption.

In recent years, digital calibration techniques have been widely used. In this Chapter, a radix-based digital calibration technique for multi-stage ADC is described. Two ADC structures based on MDAC are compared to show the basic calibration theory [10]. By making both input and reference signal go through the same signal path, all non-ideal factors within each converting

stage are merged into a single equivalent term. Since the term represents the radix for the stage, the ADC output can be calibrated by a simple radix calculation. The equivalent radix of each stage can be extracted by measuring major-carry errors and calculated mathematically using incremental update algorithm. A two-stage algorithmic ADC is designed as an example and the calibration is employed at the supply voltage of 0.9V. The measurement showed that the technique compensates for capacitor mismatch and finite opamp dc gain error. A highly linear input sampling circuit is also discussed in this Chapter.

6.2 Single-Bit per Stage ADC Architecture

Figure 6.1 shows the data conversion sequence of a single-bit per stage architecture. Depending on the polarity of the analog input signal, the digital output becomes 1 or 0. Then either upper or lower half of the reference range is amplified by a factor of 2 with the analog input signal. An MADC with a “capacitor flip-over topology”, as shown in Figure 6.2, has been widely used [26]. After the input is first sampled on the bottom plates of both sampling capacitors, one of the capacitor flips over to the output and the other one is connected to either + or – V_{ref}. The DAC control signal will be coming from 1-bit sub-ADC, which basically consists of a comparator. The comparator compares the analog input signal with differential 0V for polarity check. One of the most important advantages of a single-bit architecture over other ones is its simple structure.

In the following Sections, the detailed calibration description and circuit implementation will be discussed.

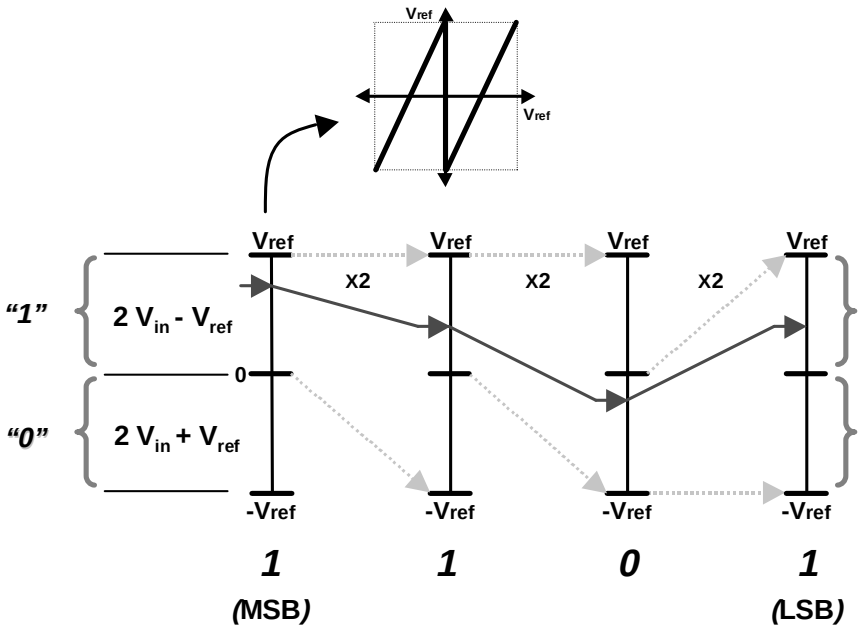


Figure 6.1 Data conversion of a single-bit/stage architecture.

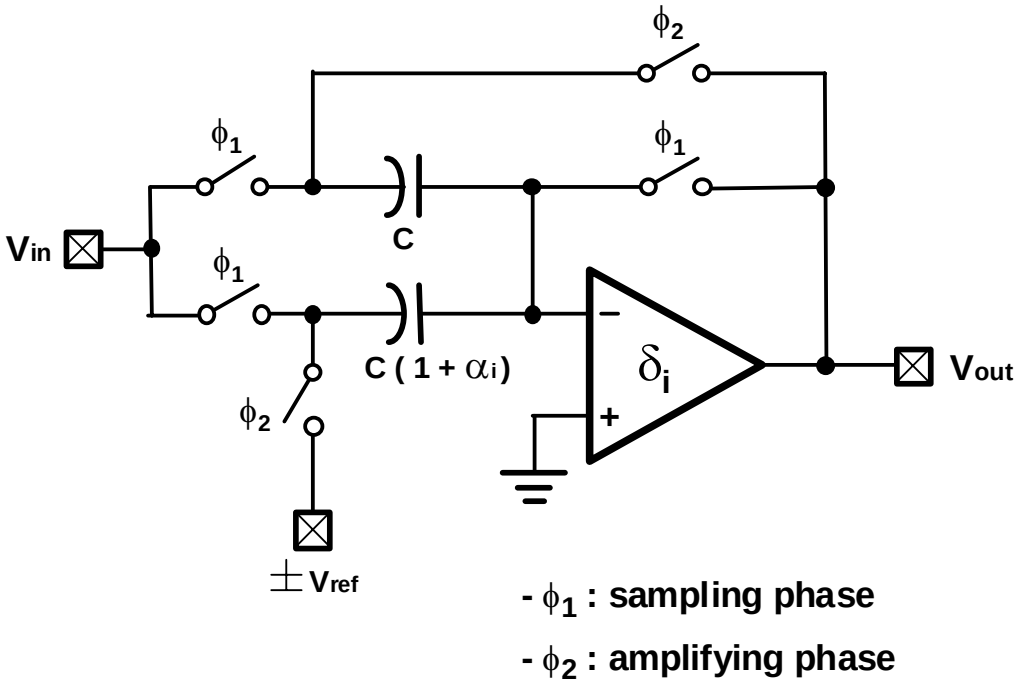


Figure 6.2 MDAC with "capacitor flip-over" architecture.

6.3 Calibration for Multi-Stage ADC

6.3.1 Radix-Based Digital Calibration in a single-bit structure

MDAC in Figure 6.2 has three important static errors, which are capacitor mismatch, finite opamp dc gain, and offset error. They are denoted as α_i, δ_i, and o_i, respectively, in Figure 6.4. Unlike capacitor mismatch and finite dc gain error, constant offset does not affect ADC linearity in most applications. However, once the offset is big enough to push the transfer curve of a conversion stage out of the reference range, the analog input information will be partly lost. The lost information, namely missing decision level, is not reconstructible even after calibration process. To ensure no missing decision level in a single-bit-stage architecture is to make interstage gain less than two. In this way, although there is a shift in the transfer function, all the information will be transferred and reconstructed by the remaining stages before the reference range clamps it. This is so called digital redundancy/correction, which relaxes offset requirement of comparators and opamps. In this Section, all offset terms are assumed to be zero and radix-2 is used for simple illustration of calibration algorithm.

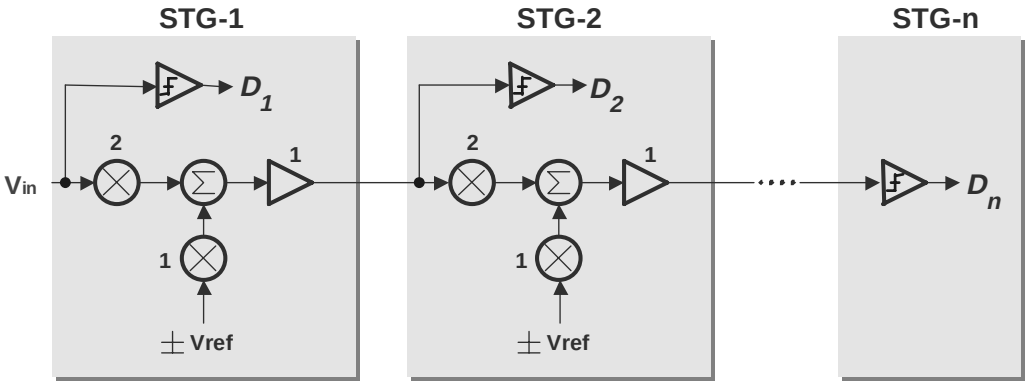


Figure 6.3 Block diagram of a multi-stage ADC with error sources.

Assuming that all capacitors are matched perfectly and the opamp has an infinite open-loop gain, the corresponding ideal operation can be depicted as Figure 6.3. The reconstructed ADC output D_{out} (quantized analog output) can be calculated as follows:

$$D_{out} = \sum_{k=0}^{n-1} D_{n-k}(2)^k \tag{6.1}$$

This provides perfectly linear transfer function. However, in the presence of all error terms, Eq. (6.1) is no longer a linear function. Assuming for simplicity that the opamp has finite but linear open-loop gain A, the i^{th} stage's residue output is:

$$V_{out} = (2+\alpha_i)(1+\delta_i)\cdot\left(V_{in} + D\cdot\frac{(1+\alpha_i)}{(2+\alpha_i)}V_{ref}\right) \tag{6.2}$$

where $\delta_i = -(2+\alpha_i)/(1+\alpha_i+A)$ and $D = \pm 1$. Figure 6.4 shows the corresponding block diagram including all non-ideal sources.

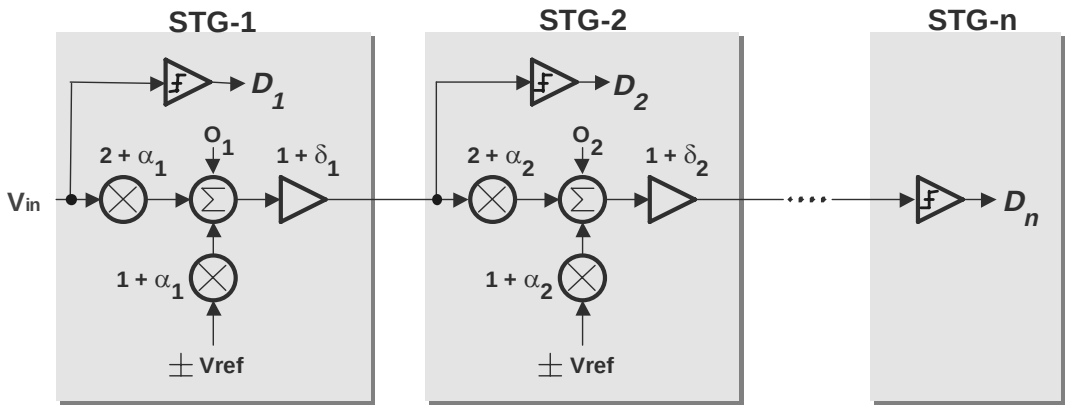


Figure 6.4 Block diagram of a multi-stage ADC with error sources.

For a special case, as in a single-stage algorithmic ADC, where $\alpha_i = \alpha$ and $\delta_i = \delta$, the residue voltage can be rewritten as:

$$V_{out} = (2+\alpha)(1+\delta)\cdot(V_{in} + D\cdot V_r) \tag{6.3}$$

where $V_r = (1+\alpha)/(1+2\alpha)\cdot V_{ref}$. Here V_r is a newly defined reference level and not a linearity error. As a result, only one equivalent error term $ra = (2+\alpha)(1+\delta)$, an interstage gain error, exists. This represents an equivalent radix for the stage. The output of the ADC can now be calibrated with a simple radix calculation [9]:

$$D_{out} = \sum_{k=0}^{n-1} D_{n-k}(ra)^k \tag{6.4}$$

However in a multi-stage case, the residue in each MDAC includes two errors as shown in Eq. (6.2), which are

interstage gain error, $(2+\alpha_i)(1+\delta_i)$, and reference level mismatch between stages, $(1+\alpha_i)/(2+\alpha_i)$. Since input and reference are amplified with different coefficients, interstage gain error alone can no longer represent the radix for the stage. For the ADC to be calibrated in the form of Eq. (6.4), both input and reference should have the same multiplying factor. Calibration of two alternative architectures is discussed in the following.

6.3.2 Calibration of Capacitor Flip-Over MDAC

First one is based on Figure 6.4. Some equivalent transformations are made to the ADC. The procedure of reconfiguration is illustrated in Figure 6.5. If we change V_{ref} to $V_{ref}/2$ and adjust the gain factor of reference voltage correspondingly, we get the diagram of Figure 6.5 (b). Then we merge the gain factor of the reference voltage into the input and output parts to have the form in Figure 6.5 (c). Finally, input and output of each stage is redefined as shown in Figure 6.5 (d). In this way, the residue voltage in i^{th} stage can be rewritten as:

$$V_{out} = 2(1+\alpha_i)(1+\delta_i)\cdot\frac{(2+\alpha_{i+1})}{2(1+\alpha_{i+1})}\left(V_{in}' + D\cdot\frac{V_{ref}}{2}\right) \tag{6.5}$$

where $V_{in}' = \frac{(2+\alpha_i)}{2(1+\alpha_i)}\cdot V_{in}$ which is a newly defined input signal. The resulting equivalent radix is

$$ra_i = 2(1+\alpha_i)(1+\delta_i)\cdot\frac{(2+\alpha_{i+1})}{2(1+\alpha_{i+1})} \tag{6.6}$$

Since both input and reference have the same multiplying factor, the calibrated ADC output can be obtained as:

$$D_{out} = D_n + D_{n-1}(ra_{n-1}) + D_{n-2}(ra_{n-1})(ra_{n-2}) + \ldots + D_1\prod_{k=1}^{n-1} ra_k \tag{6.7}$$

One issue in this reconfiguration is that the comparator in sub-ADC still sees the original input V_{in} (before reconfiguration) to generate the digital output. Therefore, signal dependent offset is added to the comparator. In general, this is not a problem because the added offset is strictly coming from internal capacitor mismatch, which is usually small enough to be compensated by digital redundancy between stages.

6.3.3 Half-Reference MDAC

The other method is based on the MDAC structure illustrated in Figure 6.6. As mentioned above, to have a set of single error term per stage, both input and reference should see the identical error term. Instead of one of the sampling capacitors being flipped over to the output, dedicated feedback and sampling capacitors are used. After input is sampled onto the sampling capacitor while the opamp is being reset, + or – V_{ref}/2 is sampled to the very same capacitor. Therefore, reference voltage is directly subtracted from the input before it is multiplied such that it can take the same signal path as input. The residue voltage can be described as:

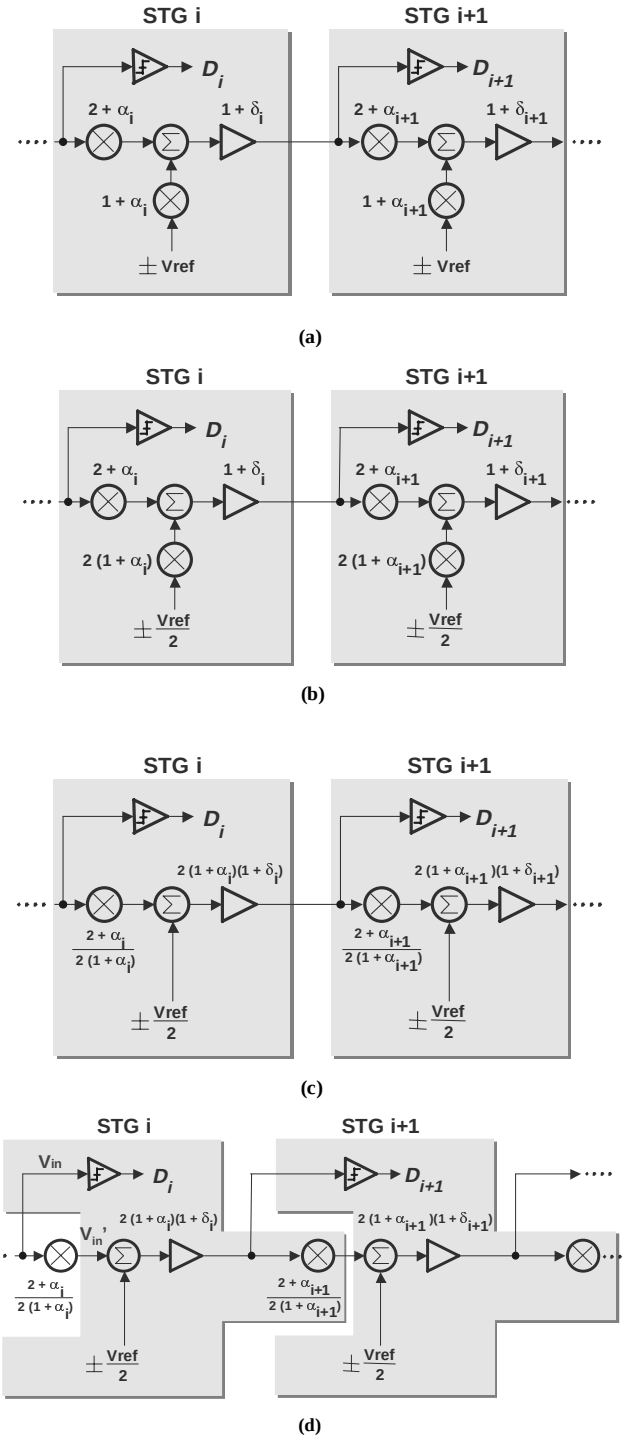


Figure 6.5 Equivalent transformation of the ADC.

$$V_{out} = ra_i \left(V_{in} + D \cdot \frac{V_{ref}}{2} \right) \tag{6.8}$$

where $ra_i = (2+\alpha_i)(1+\delta_i)$. In this way, the digital output can also be calibrated by Eq. (6.7). The block diagram of this operation can be depicted as Figure 6.7.

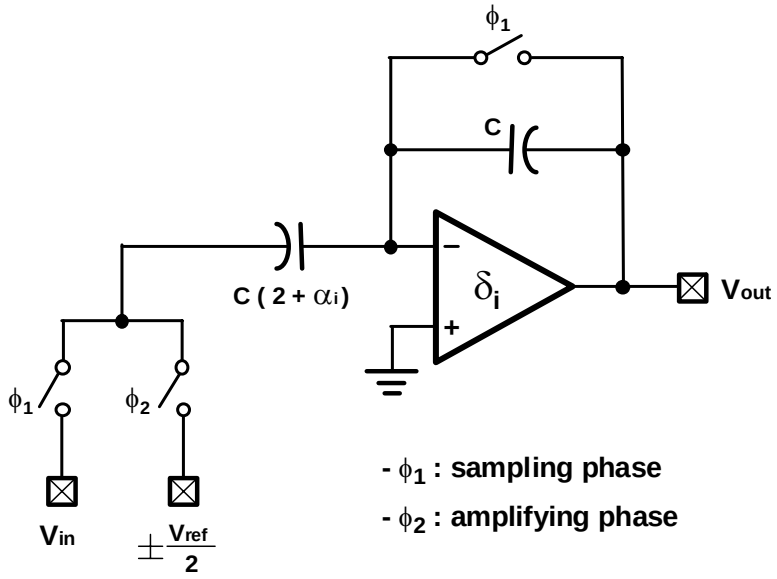


Figure 6.6 “Half-reference” MDAC architecture.

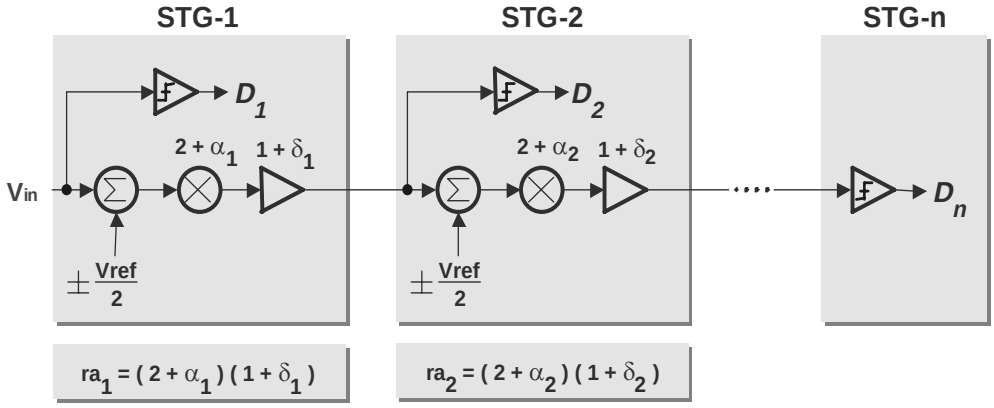
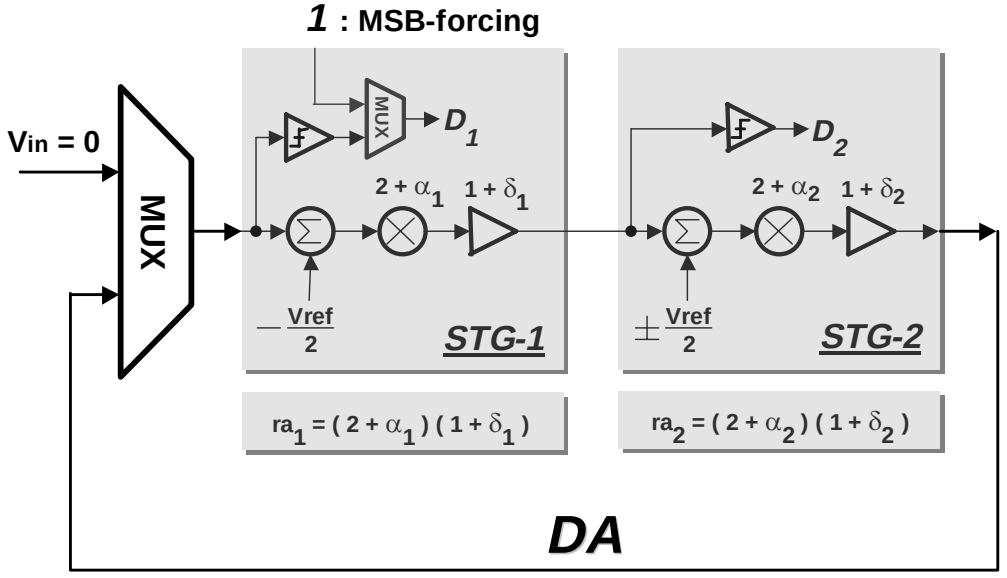


Figure 6.7 Block diagram of a proposed multi-stage ADC using “Half-reference” MDAC.



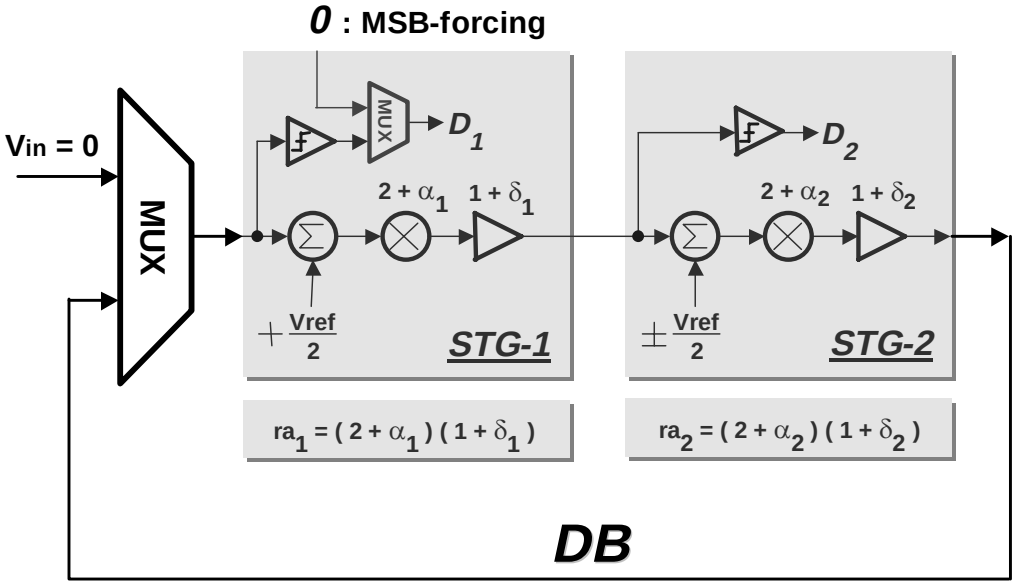


Figure 6.8 Conceptual block diagram of ra_1 iteration.

6.3.4 Radix Iteration

In this calibration, all error terms should be measured accurately. The accuracy of the measurement decides the overall ADC resolution. The primary difficulty is that the exact radix for each stage cannot be known precisely in advance. Therefore, estimated initial value will be used to start iterative calculation. Between the two configuration described in the previous section, the latter architecture (Figure 6.7) is used in this Section to show the detailed calibration steps. The former one will be calibrated exactly the same way. A 20-bit two-stage algorithmic ADC is chosen representing a multi-stage ADC for behavioral simulation as shown in Figure 6.8. The ADC generates 20-bit digital output after 10 cyclic conversions. The ADC output can be reconstructed by

$$\begin{aligned} D_{out} = \underbrace{D_{20}}_{LSB} + D_{19}(ra_1) + D_{18}(ra_1)(ra_2) + D_{17}(ra_1)^2(ra_2) \\ + D_{16}(ra_1)^2(ra_2)^2 + \ldots + \underbrace{D_1}_{MSB}(ra_1)^{10}(ra_2)^9 \end{aligned} \tag{6.9}$$

where ra_1 and ra_2 are equivalent radices for STG-1 and STG-2, respectively. The measurement procedure starts by monitoring the major carry transition. The biggest discontinuities occur at the points where the MSBs (we are referring to the first two bits, which result from this two-stage algorithmic ADC structure) change from zero to one. These discontinuities are referred to as the major-carry jump (*mcarry*). The *mcarry* can be extracted by injecting digital bits to the MSB-stage. For example, under ideal condition, if '1' is forced to the MSB-stage with zero analog input then the residue results in $-V_{ref}$ and the resulting ADC output would be 1000…00. When '0' is forced with the same condition, the residue would be V_{ref} and the ADC output would be 0111…11. The difference between the two digital words is 1 code, which is 1-LSB in ideal radix-2 system. However, as shown in Figure 6.9, the difference between the radix estimate and the actual value of the equivalent radix causes *mcarry* to be different from 1-LSB. The difference is coming from the

combination of the first and second stage's radix estimation errors. By using the 1-LSB as the desirable value of all major-carry jumps, the each estimated radix correction can be made by incremental update algorithm:

$$ra_i[n+1] = ra_i[n] - \Delta \cdot (mcarry[n] - 1\text{LSB}) \tag{6.10}$$

where n is the iteration index and Δ is update step size. While one radix is updated, the other one is fixed to the previous value. They are updated alternatively until iterating to final values. For non-radix-2 operation (with all error terms), the detailed calibration procedure will be described in the following.

First step is to measure ra_1 while the estimate ra_2 holds the fixed initial value. As shown in Figure 6.8, MSB of '1' is forced to STG-1 and the analog input is set to zero. The resulting residue can be shown as:

$$V_A = -ra_1 \cdot \frac{V_{ref}}{2} \tag{6.11}$$

The ADC itself then digitizes V_A during the remaining conversion cycles to have a 20-bit digital word, *DA*. Next, MSB of '0' is forced to STG-1 to obtain the residue of

$$V_B = ra_1 \cdot \frac{V_{ref}}{2} \tag{6.12}$$

which is also digitized to have *DB*. Notice that V_A and V_B define the new upper and lower reference level of STG-2. The *mcarry* can now be calculated as follows:

$$mcarry = D_{out}(DA) - D_{out}(DB) \tag{6.13}$$

With the extracted *mcarry*, ra_1 is updated using Eq. (6.10) and stored in the memory for ra_2 measurement.

The ra_2 measurement is done in a same manner as ra_1. The only difference is that during bit-forcing to STG-2 with zero analog input, digital output of STG-1 (MSB) can be either '1' or '0'. This implies that ra_2 measurement is done in 19-bit level by monitoring either upper or lower

second-major-carry jump ($mcarry_2$) in Figure 6.9. The resulting residues from STG-2 during the bit-forcing sequence also redefine the full input range of STG-1. After ra_2 is updated by Eq. (6.10), it is stored in the memory to go back to the calculation/update of ra_1. Since the overall ADC range is composed of a combination of two radices, they are updated alternatively based on one another's latest values until the overall transfer function is fully linear. The update/iteration loop is purely mathematical after generating four digital words. Although a two-stage algorithmic ADC was used for simplicity, this calibration sequence can be extended to ADCs with any number of stages.

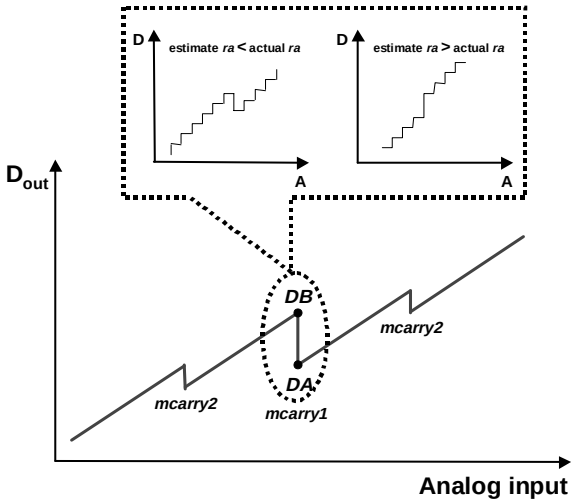


Figure 6.9 Nonlinear ADC transfer curve.

6.3.5 Low-Voltage Calibration with Bit-Lookahead Scheme

In low-voltage analog circuit design, especially in switched-capacitor circuit design, sampling (floating) switches are no longer available as mentioned in the previous Chapter. Therefore, Figure 6.6 cannot be used as it is. Figure 6.10 shows the low-voltage version of Figure 6.6 with all floating switches being eliminated. During sampling phase (Φ_1), both $V_{ref}/2$ and analog input signals are sampled on the top and bottom plates of the sampling capacitor, respectively.

During amplification phase (Φ_1), top plate of the capacitor is connected to the virtual ground of the opamp to generate residue voltage exactly same as Eq. (6.8) while the bottom plate is being reset by the sourcing amplifier from the previous stage (ORST).

In conventional pipelined ADCs, sub-ADC's bit decision is made half clock period later than the input signal sampling, which implies that the input and +/- $V_{ref}/2$ cannot be sampled during the same clock phase. However, sampling both signals at the same time is the key operation in the radix-based calibration. Therefore, the low-voltage structure requires a bit-lookahead configuration to move the comparator decision one clock ahead. This is shown in Figure 6.11. Instead of comparators deciding polarity of the present stage input, the ADC looks ahead to the next stage signal polarity by shifting the reference points of the comparator by + and – $V_{ref}/2$ [52]. This will result in two digital outputs in each stage. The valid data between the two is selected by the previous stage's digital output. For example, if D1=1 then D2-1 is the valid digital output for COMP-2 (if D1=0 then D2-2 will be the valid one). At the same time, D2-1 also controls the reference sampling of the second stage MDAC (MDAC-2) while input is being sampled.

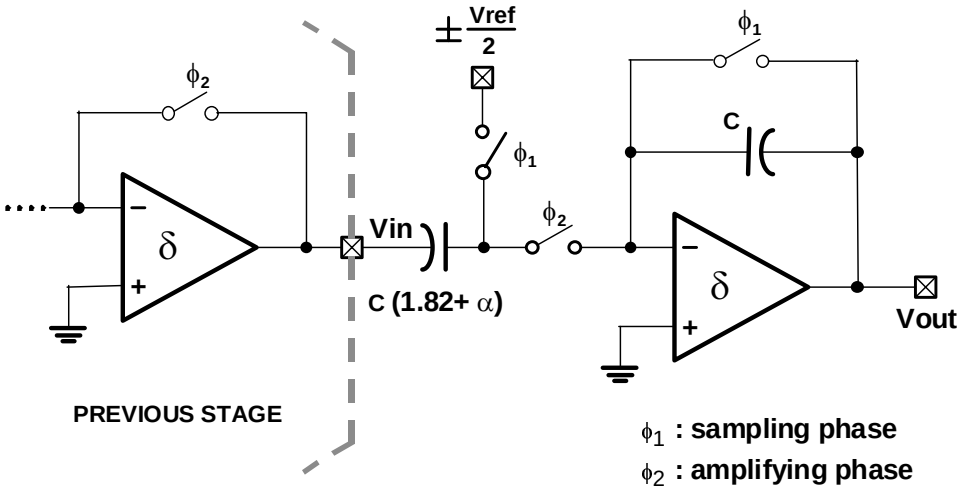


Figure 6.10 Low-voltage MDAC.

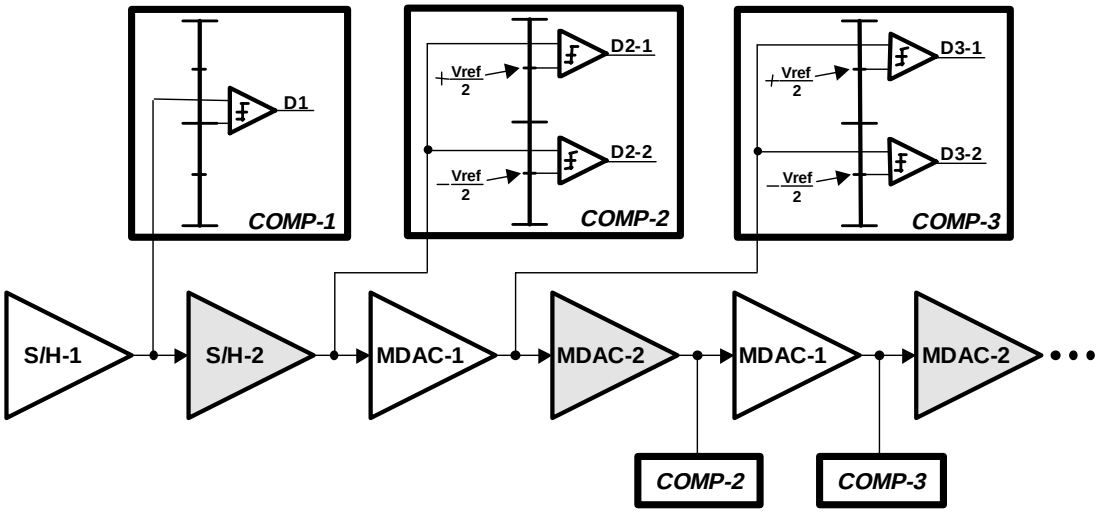


Figure 6.11 Bit-lookahead scheme.

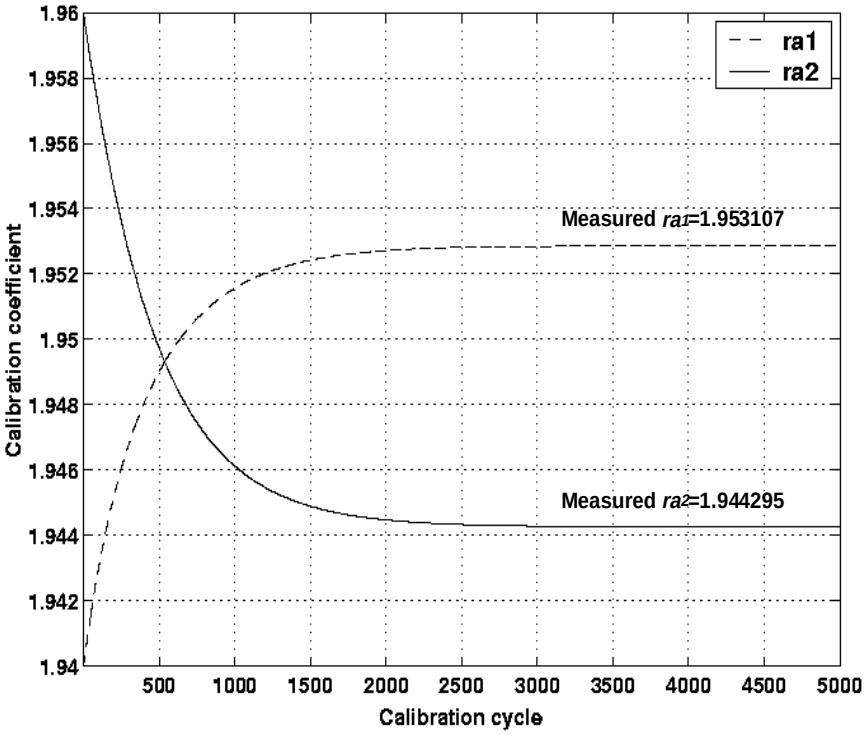
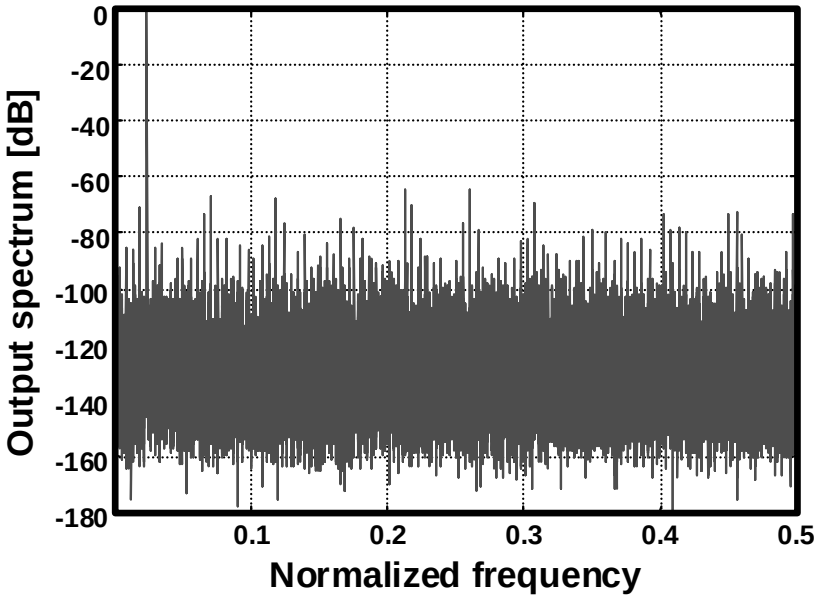


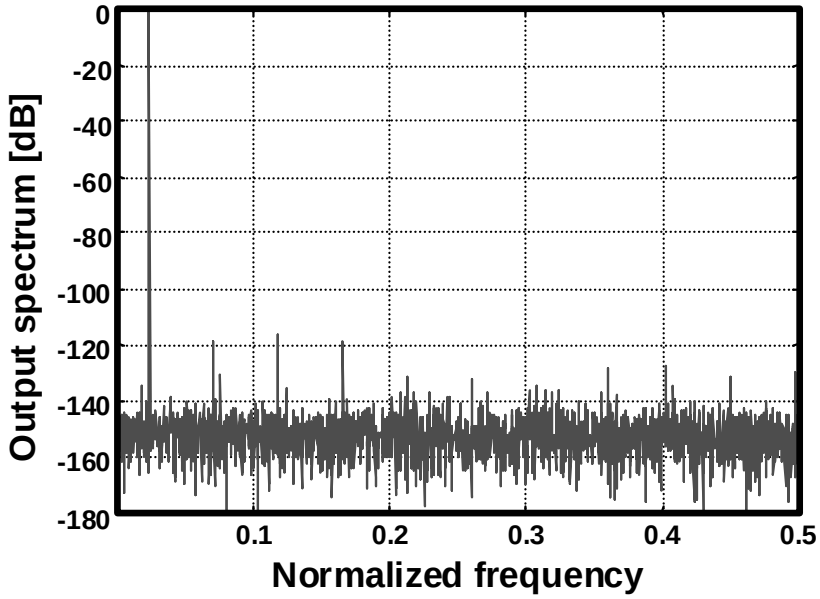
Figure 6.12 Radices iteration for the two-stage algorithmic ADC.

6.3.6 Behavioral Simulation

Figure 6.12 shows a behavioral model simulation based on Figure 6.8 illustrating the iteration of ra_1 and ra_2. Actual values for ra_1 and ra_2 are 1.953131 and 1.944248, respectively. The final iteratively reached values are ra_1=1.9531**07** and ra_2=1.9442**95**. The update step size Δ should be smaller than 1-LSB step size of the ADC. In this simulation, 2^{-24} is used. Figure 6.13 shows the FFT plots with 0.1% device mismatch and opamp dc gain of 1000. The resulting SNDR shows 58dB before calibration and 112dB after calibration. Compared to the SNDR of an ideal 20-bit ADC (with radix-1.95), which is 117dB, the calibrated one is lowered by about several dB. There is couple of reasons for that. One reason is that ra_2 is iterated using 19-bit digital words (not 20-bit). Second, digital truncation errors occur during the calculation of *mcarry*. In theory, one simple way to recover the decreased dynamic range is to increase the resolution of the ADC for the calibration mode and reduce radix update step size (Δ) more during iteration. It has been verified that this results in achieving almost ideal accuracy of the overall ADC. In IC realization, however, component nonlinearities and thermal noise would limit the overall resolution. The detailed circuit implementation of this two-stage algorithmic ADC will be discussed in the following Section. In addition, low-voltage calibration will also be covered.



(a)



(b)

Figure 6.13 FFT plots of (a) before and (b) after calibration of a half-reference architecture.

6.4 Building Block Implementation

Figure 6.14 shows the block diagram of the proposed two-stage algorithmic ADC. It consists of input sampling circuit and two conversion stages. Each stage has an MDAC and a comparator providing a single-bit. The ADC generates 12-bit digital output after 7 clock cycles. Therefore, the operating internal clock has to be running six times faster than the sampling rate. The difference from a 1.5-bit per stage architecture is that to achieve digital redundancy between stages an interstage gain of less than 2 (1.82 in this work) has to be used rather than overlapping bits with shift registers and adders. This keeps the transfer curve in each stage within V_{ref} boundary despite of capacitor mismatch and offset errors. This section will cover the detailed implementation of each individual circuit block.

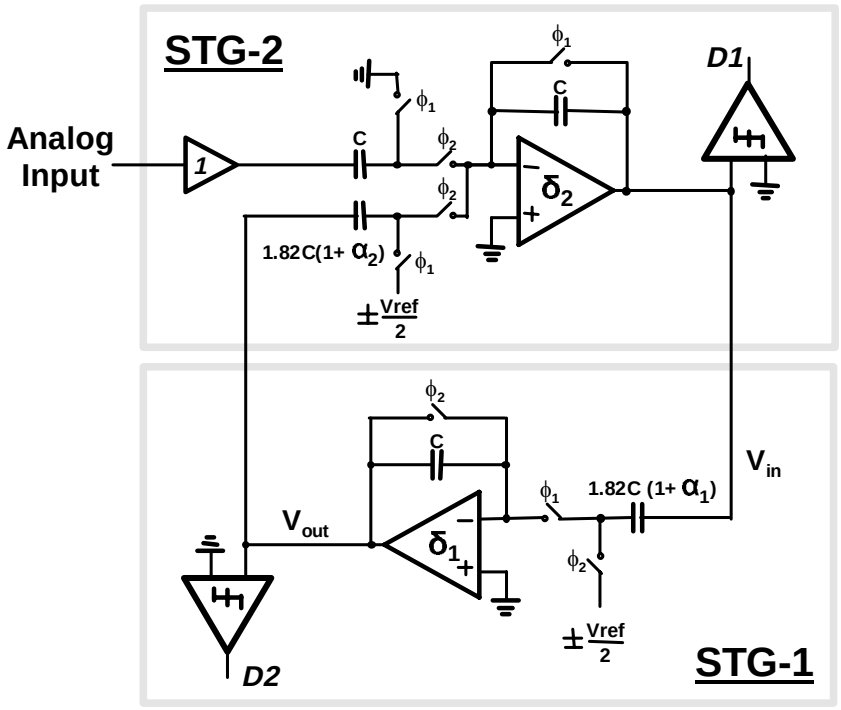


Figure 6.14 Block diagram of the low-voltage two-stage algorithmic ADC.

6.4.1 Input Sampling Circuit

The proposed highly linear input sampling circuit is illustrated in Figure 6.15. In the new low-voltage sampling circuit, three design techniques are proposed to minimize this nonlinearity problem. They are depicted in shaded areas. During Φ_2, the capacitor C_{c1}, which was precharged to V_{DD} during the previous clock phase, is connected between the gate of MPP and V_{xp}, so that the gate voltage can track the variation of V_{xp}. This makes R_{MPP} constant:

$$R_{MPP} = \frac{1}{\beta\left(V_{DD} - |V_{th}|\right)} \tag{6.14}$$

Note that V_{xp} is slightly lower than V_{DD} during Φ_2, and X may go below GND, which can cause a latch-up condition. Careful design requires proper sizing of C_{C1} with respect to $2C$. We have used C_{C1}=4pF and C_1=C_2=2pF in this design. To cancel the remaining distortion at the output, V_{xp} and X are sampled to two level shifting capacitors C_1 and C_2, respectively, instead of sampling V_{DD} and GND. In doing so, the nonlinear fluctuation at V_{xp} is cancelled during the tracking operation:

$$\begin{aligned} V_{batt} &= \frac{V_{xp}\left(C_1 + C_2\right) - \left(C_1 V_{DD} + C_1\left(V_{xp} - V_{DD}\right)\right)}{C_1 + C_2} \\ &= \frac{C_2 V_{DD}}{C_1 + C_2} \end{aligned} \tag{6.15}$$

The output is no longer a function of V_{xp} or R_{MPP}, but a linear function of V_{INP} only:

$$V_{OUTN} = \left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)\right)^{-1} \cdot \left(\left(1 + \frac{R_2}{R_1}\right)\left(\frac{C_2 V_{DD}}{C_1 + C_2}\right) - \left(\frac{R_2}{R_1}\right)V_{INP}\right) \tag{6.16}$$

Because the device/elements will never match perfectly in the circuit implementation, incorporating both techniques will minimize distortion. Another straightforward way to improve the linearity of R_{MPP} is to increase the device size, so that the fluctuation at V_{xp} is as small as possible. However, this increases the chip area. In the proposed circuit, we have incorporated a differential resetting switch MPC. The switch can be made half the size of MPP and MPN, and

will achieve the same result as doubling the sizes of MPP and MPN. Using MPC also helps to suppress even harmonics that are due to device mismatches in the two pseudo-differential signal paths. This is because MPC provides a differentially stable V_{DD} reference level to both V_{xp} and V_{xn} during the reset phase.

Figure 6.16 shows FFT plots of the conventional (Figure 5.3 without MPC) and the proposed (Figure 6.15) circuits with 1% random mismatches in resistors, capacitors, and MOS switches. Modeled opamps with finite gain-bandwidth are used for simulation. The conventional circuit shows a total harmonic distortion (THD) of -40dB while the proposed circuit shows -100dB. There is little variation of THD when the input signal is swept over the entire Nyquist bandwidth.

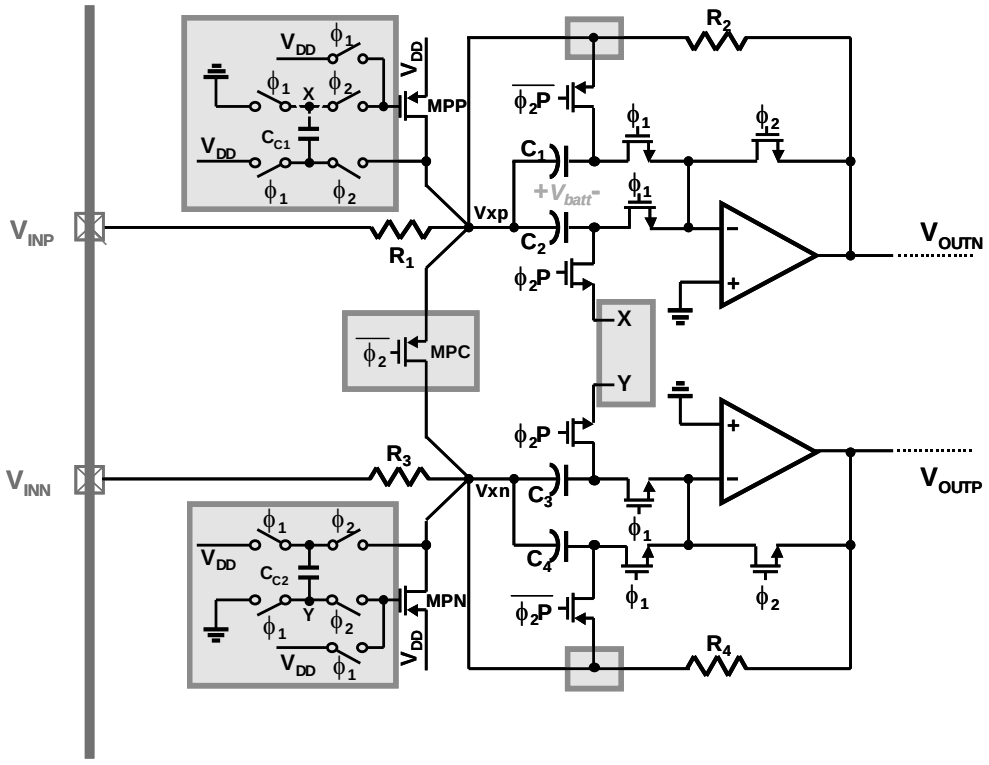
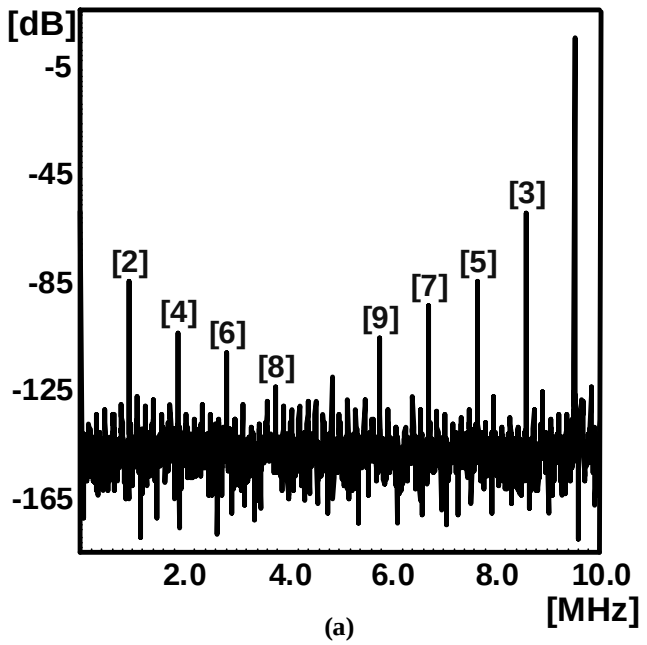
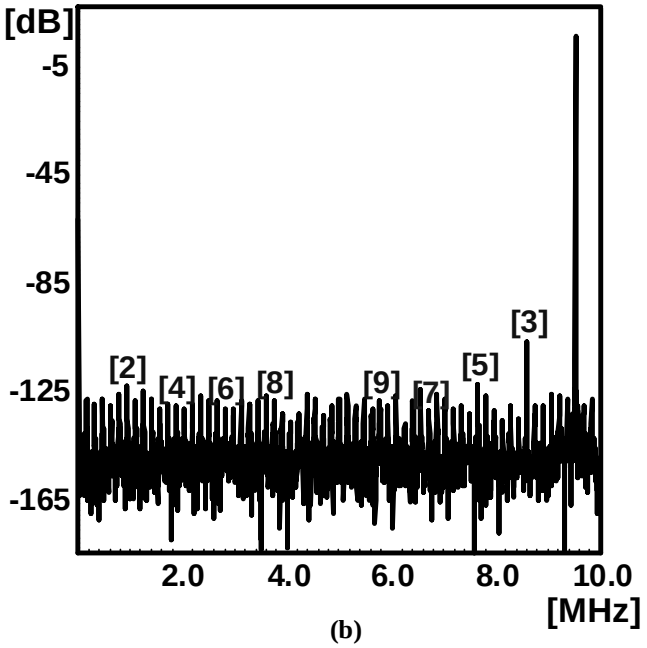


Figure 6.15 Proposed input sampling circuit with improved linearity.



(a)



(b)

Figure 6.16 FFT simulation results of (a) conventional and (b) proposed circuit.

6.4.2 MDAC

The full schematic of the low-voltage MDAC is depicted in Figure 6.17. It employs the ORST in the pseudo-differential architecture. With a differential analog input range of 1V peak-to-peak, $V_{ref}/2$ implies ±0.125V single-ended swing from $V_{DD}/2$ (=0.5V), which makes reference sampling difficult due to switch overdrive problem. In this design, the reference swing center is shifted down to $V_{ref}/4$, which equals to 0.125V. Therefore, $V_{ref}/2$ can be realized by differential sampling between 0.25V and *GND*. To avoid the input signal common-mode error accumulation problem, cross-coupled feedback capacitors are also used as in the previous pipelined ADC design. Therefore, the differential gain of $C_S/(C_{M1}-C_{M2})$=1.82 can be achieved while the common-mode gain is kept to $C_S/(C_{M1}+C_{M2})$=1. The virtual ground of the opamp is also set to $V_{ref}/4$ as well to further suppress reference common-mode accumulation error.

To ensure no missing decision level in a 1-bit-per-stage ADC architecture, interstage gain is usually made less than 2 for digital redundancy between stages. This relaxes the offset requirement of opamps and comparators. On the other hand, reducing the gain results in shrinking the ADC dynamic range. To avoid large reduction of the interstage gain, we chose to sufficiently cancel the offsets at the circuit level. In this design, the pseudo-differential offset cancellation technique is used. As shown in Figure 6.18, offset level is sampled onto the storing capacitor (C_{off}) during the sampling phase. During the amplification phase, actual offset voltage and the precharged value are cancelled out. This sets the V_x node to ground potential. The technique is made possible because one node of the virtual ground pair is always available in the pseudo-differential configuration.

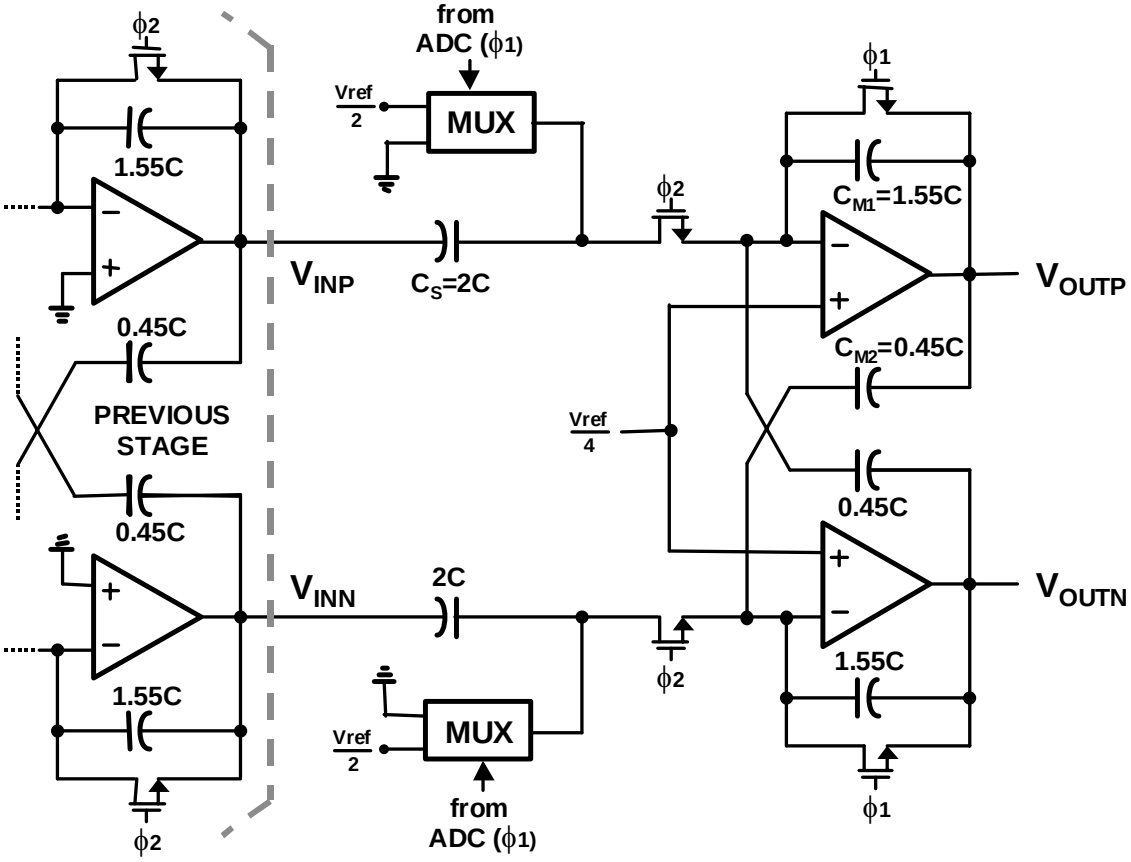


Figure 6.17 Simplified schematic of the MDAC.

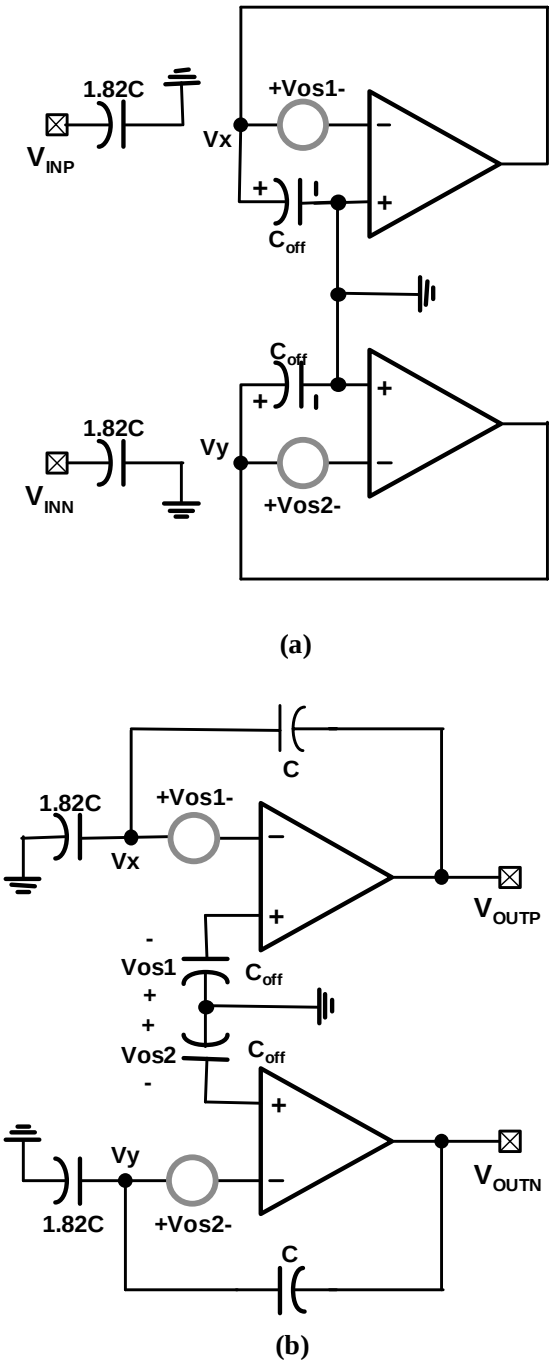


Figure 6.18 Pseudo-differential offset cancellation: (a) offset sampling and (b) offset cancellation.

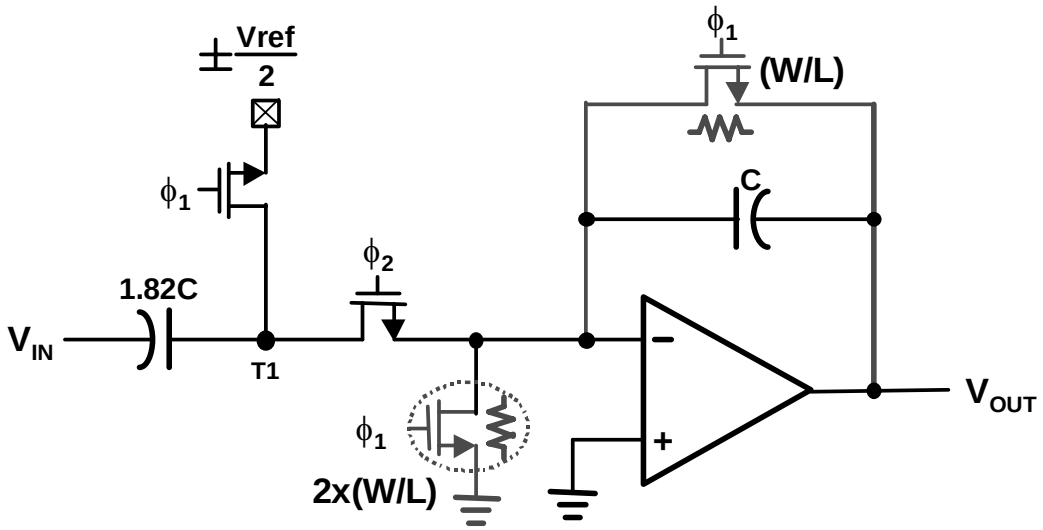


Figure 6.19 Feedback factor control.

When using the ORST in MDAC, there is a feedback factor difference between sampling/reset and amplification mode. This is because the opamp has to be placed in the unity-gain feedback configuration during the sampling/reset phase. If the difference is drastic, the opamp would have to be over-compensated to cover a wide range of loop bandwidths. This would end up being an unnecessary burden on the switched-capacitor circuit design. As shown in Figure 6.19, an additional switch that provides a resistance between virtual ground and *GND* during the sampling phase is employed. It is made half the size of the feedback switch. With this switch, the reset mode feedback factor has the similar value to that of amplification mode (feedback factor of 1/3), which assures good phase margin and settling dynamics.

6.4.3 Comparator

The sub-ADC is composed of a preamplifier and a latched-comparator. Comparators compare input with + and – $V_{ref}/2$ for the bit-lookahead decision. The one of the most critical parts

in comparator design is minimizing the input offset. Otherwise, the ADC will lose dynamic range. There are various offset cancellation methods and the most common approaches among them are based on input offset storage (IOS) and output offset storage (OOS) [34]. IOS is often called auto-zeroing technique, which stores the offset voltage at the input sampling capacitor by unity-gain feedback configuration. However, ISO is not suitable in low-voltage design because the floating switch transferring offset from output to input is no longer available. In this design, OOS is used to bypass the floating switch problem.

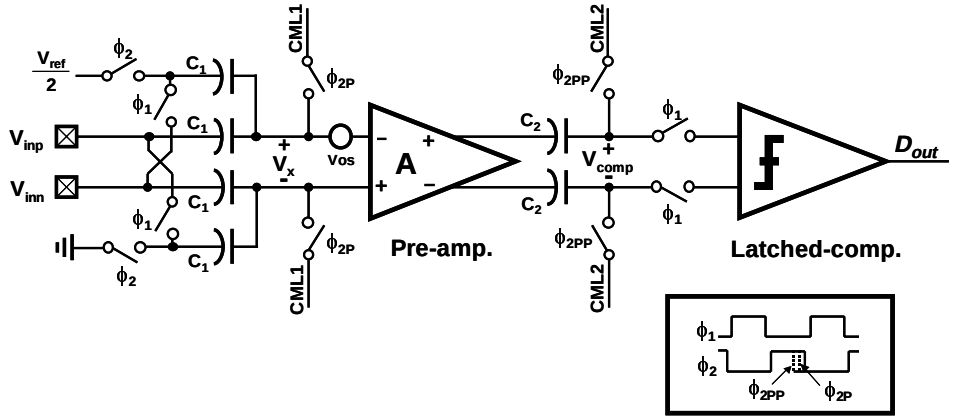


Figure 6.20 Simplified full schematic of the comparator.

Figure 6.20 shows the simplified schematic of the comparator. The detailed operation is shown in Figure 6.21. During sampling phase (Φ_2), offset of the sourcing amplifier (V_{osa}) is cancelled out initially by cross-coupled sampling. Therefore, effectively zero voltage is charged to C_1. Additional offset due to opamp-reset switching is negligible. The offset of the preamplifier (V_{os}) is amplified by itself and sampled onto C_2. During comparison phase (Φ_1), reference voltage is subtracted by analog input with V_{os} to form V_x in Eq. (6.18) and then amplified by the preamplifier. When the voltage is sampled onto C_2, V_{os} is cancelled out and V_{comp} is a function of V_{in} and $V_{ref}/2$ only.

$$V_i = V_{inp} - V_{inn} \tag{6.17}$$

$$V_X = V_i - \frac{V_{ref}}{2} - V_{os} \tag{6.18}$$

$$\begin{aligned} V_{comp} &= A\left(V_i - \frac{V_{ref}}{2} - V_{os} \right) + \left(AV_{os} \right) \\ &= A\left(V_i - \frac{V_{ref}}{2} \right) \end{aligned} \tag{6.19}$$

where A is the open-loop gain of preamplifier. One important thing that should be considered on deciding the preamplifier gain is that if it is too small, the offset of the latched-comparator starts to affect on the transfer curve. If the gain is too large, AV_{os} goes out of the signal range and lose the offset information. In this design, the gain is set to be about 8. C_1 and C_2 are sized 200fF.

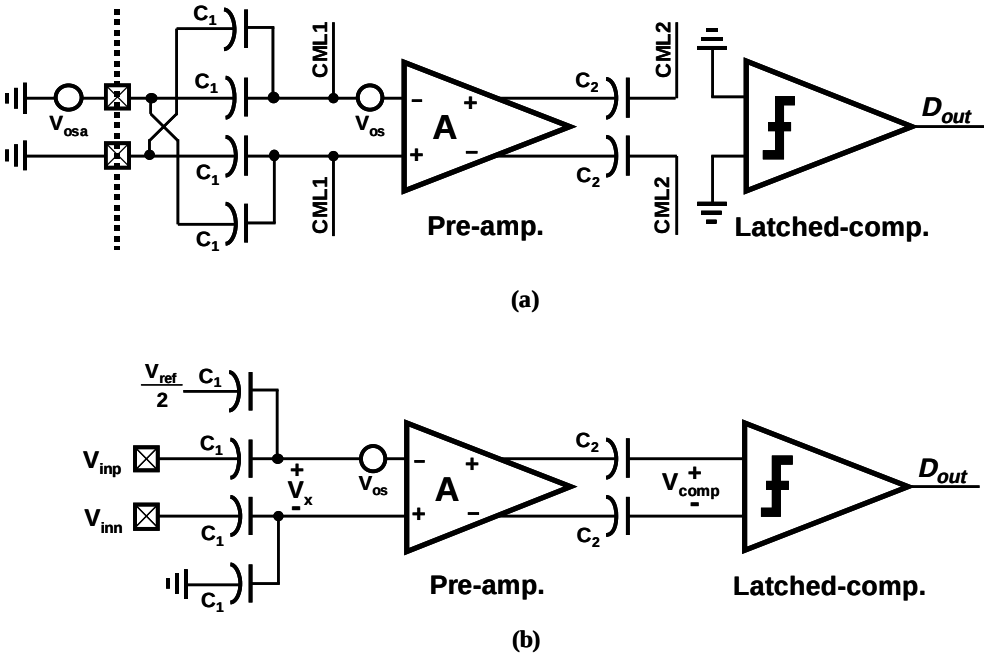


Figure 6.21 OOS of the comparator: (a) sampling phase and (b) comparison phase.

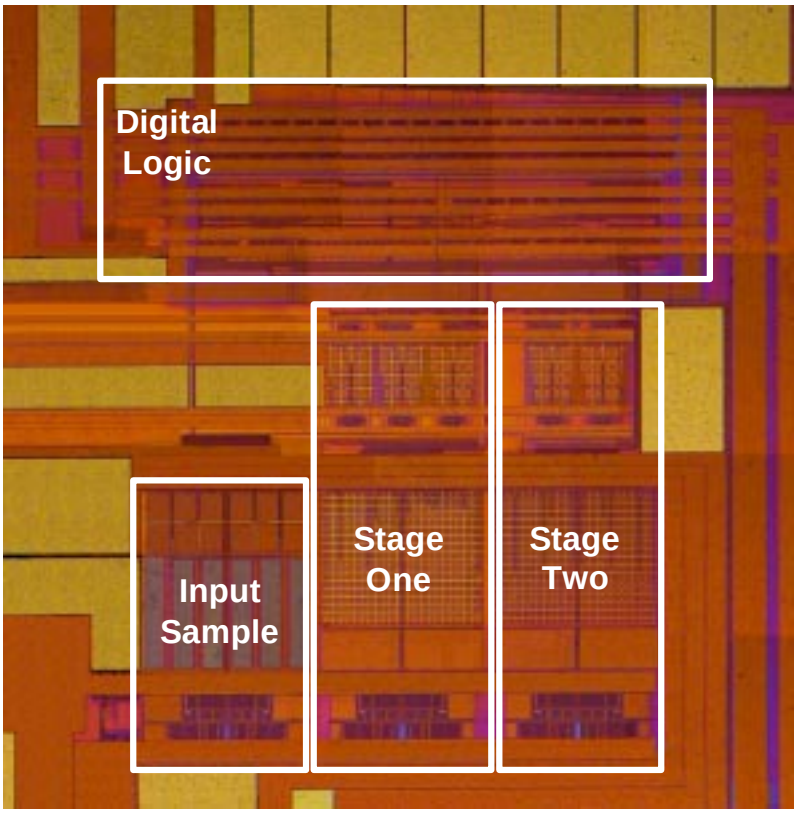


Figure 6.22 Die photograph of the prototype ADC.

6.5 Measurement Results

The chip photograph of the prototype is shown in Figure 6.22. Its active die size is 1.2mm x 1.2mm. The input sampling circuit is laid out in the lower left part and two converting stages are located side by side to minimize the signal crossing. Resolved bits are sent to digital blocks, which are placed upper part of the chip with timing circuit. All clock signals are coming from that part. The chip was implemented in a 0.18-μm CMOS process. Threshold voltages for both NMOS and PMOS are 0.45V. The prototype ADC was characterized with SNDR and SFDR measurements based on an FFT test, and DNL and INL measurements based on a code-density test. Under normal conditions, the power supply voltage is 0.9V and the reference range is $0.9V_{p\text{-}p}$.

Chips are also characterized with higher supply conditions. In each case, reference range is also adjusted to have the same number as the supply voltage. Due to reduced radix and digital truncation error, the prototype was tested in 10-bit (binary) level although the ADC output is obtained in 12-bit (sub-radix) word. The digital calibration was done by MATLAB code externally.

Before actual static and dynamic measurements, precise radix measurement of each stage should be done in advance with procedure described in Section 6.2. Figure 6.23 shows the radix iteration steps with initial value of 1.82. The update step size of 2^{-14} was used for iteration. The final values change under different supply, conversion speed, and bias condition due to varying settling behavior and dc gain variation of the opamp. All measured results in the following were obtained after radix measurement/iterations based on each test condition.

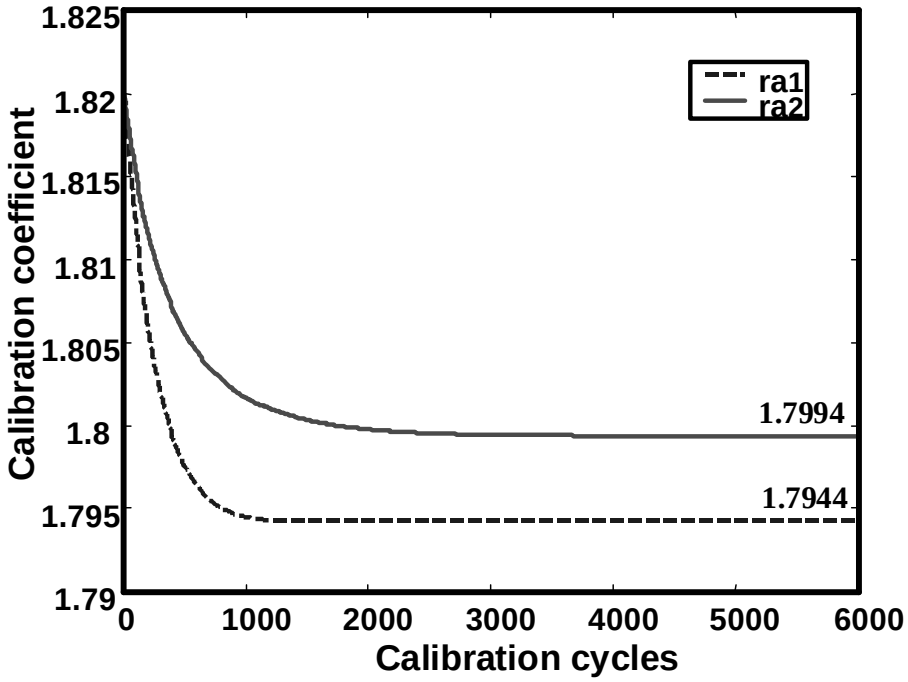


Figure 6.23 Convergence of radix iterations (measured).

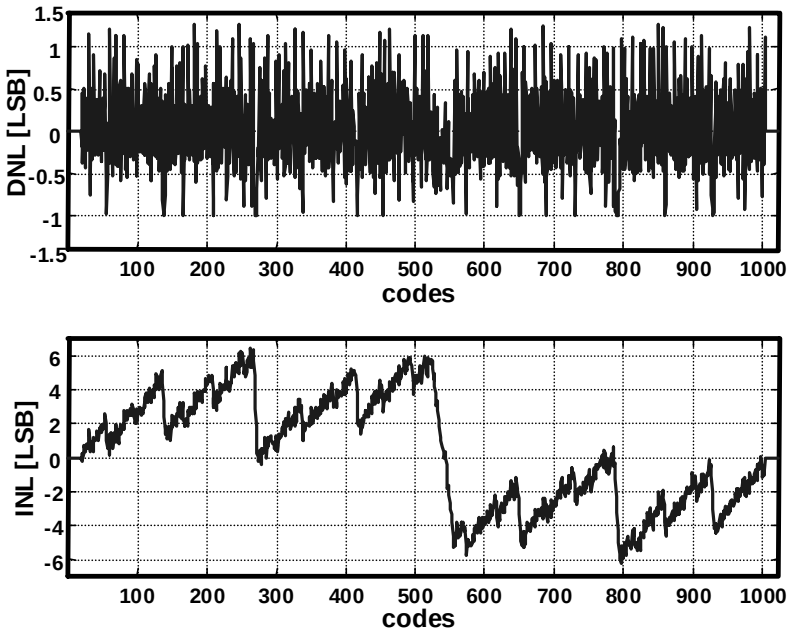


Figure 6.24 DNL and INL before calibration at 0.9V with fs=1MSPS.

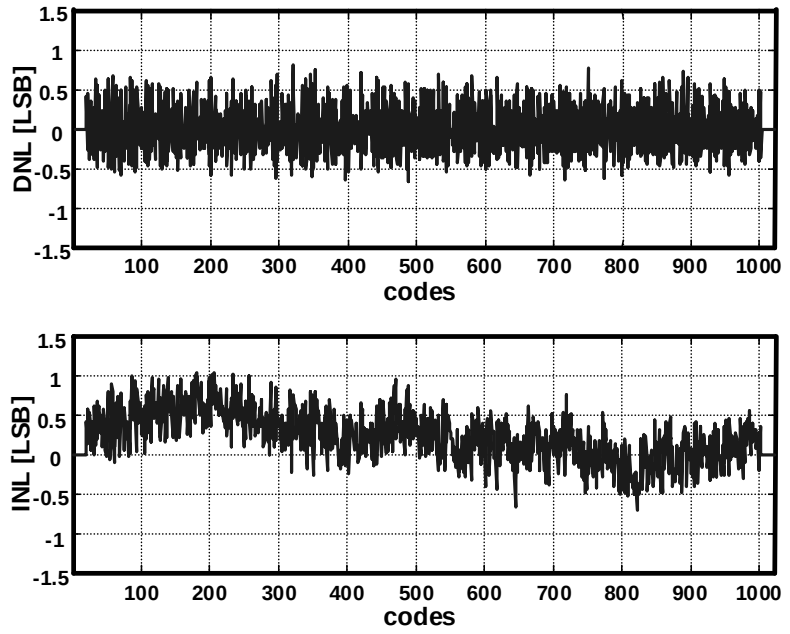


Figure 6.25 DNL and INL after calibration at 0.9V with fs=1MSPS.

6.5.1 Static Performance Measurement

The code density measurements are done in 10-bit level. Total of 2^{16} samples was collected with sampling rate of 1MSPS and input signal of 15Hz. Typical DNL and INL plots are shown in Figure 6.24 and Figure 6.25 for "before calibration" and "after calibration", respectively. Before calibration shows that peak DNL and INL errors are 1.4/-1LSB and 6.3/-6.2LSB, respectively. DNL of –1LSB implies missing codes, which result in huge INL error jumps at major transition codes. After calibration, DNL and INL errors improved to 0.8/-0.65LSB and 1.05/-0.7LSB, respectively. There is no missing code and most of the major carry jumps are removed in INL plot.

6.5.2 Dynamic Performance Measurement

In this FFT test, 2^{13} sample are used for SNDR and SFDR. Figure 6.26 shows output spectrum at 0.9V supply. Full-scale input sine wave of 50kHz with sampling rate of 1MSPS were used. Before calibration, SFDR of 47dB and SNDR of 40dB were obtained. After calibration, all harmonics are reduced below –75dB and SNDR improved to 55dB. It can be concluded that SNDR is dominated by noise level rather than harmonic distortion after calibration. Figure 6.27 shows the dynamic measurement results with different supply voltage conditions at the same dc bias current. It demonstrates that the SFDR goes above 80dB at 1.2V supply condition. This is because the opamp has more headroom for signal swing with higher supply results in less signal distortion. In this measurement setup, the peak-to-peak differential input range was set equal to supply level. Figure 6.28 shows the dynamic performance versus different input signal frequencies. The ADC performs consistently up to Nyquist rate. This also implies that the input sampling circuit also works above 80dB-linearity level independent of input signal frequency. Dynamic performance versus clock rate is also shown in Figure 6.29. The ADC performs up to 1.5MSPS while retaining consistent performance. Finally, the ADC is pushed up to the maximum

operating speed by increasing bias current externally. Figure 6.30 shows that at 0.9V supply, sampling rate can go up to 2MSPS with power consumption of 32mW. At 1.2V supply, it can go as high as 3.5MSPS with power consumption of 45mW. Operating speed of the ADC does not go higher than those values although bias currents are further increased. It is because bias voltages in opamps start to saturate after certain potential and degrades circuit performance. Performance of the calibrated ADC is summarized in Table 6.1.

Technology	**0.18-µm CMOS**
Resolution	**10.4 binary bits (12 bits of 1.82 radix)**
Active die area	**1.2 x 1.2 mm^2**
Supply voltage	**0.9V**
Conversion rate	**1MSPS (clock=7MHz)**
Power consumption	**9mW**
DNL	**1.4LSB / 0.8LSB**
INL	**6.3LSB / 1.05LSB**
SNDR	**40dB / 55dB (after cal.)**
SFDR	**47dB / 75dB (after cal.)**

Table 6.1 Performance summary of the pipelined ADC.

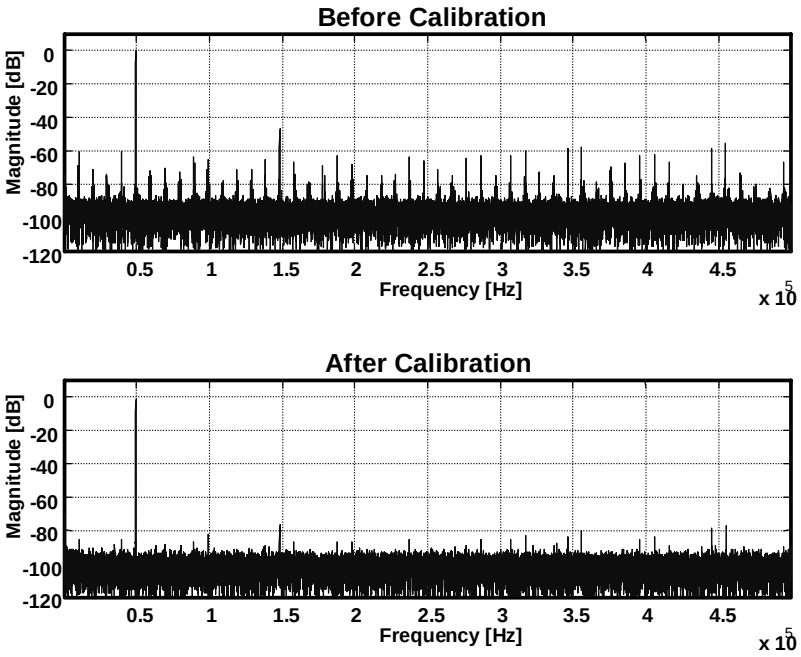


Figure 6.26 Output spectrum at 0.9V with fin=50kHz and fs=1MSPS.

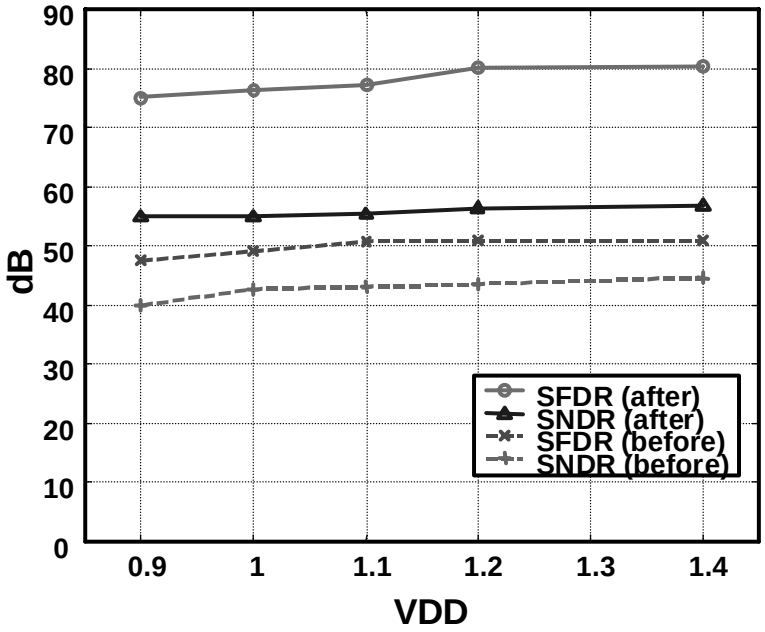


Figure 6.27 Dynamic performance vs. supply voltage with fin=50kHz and fs=1MSPS.

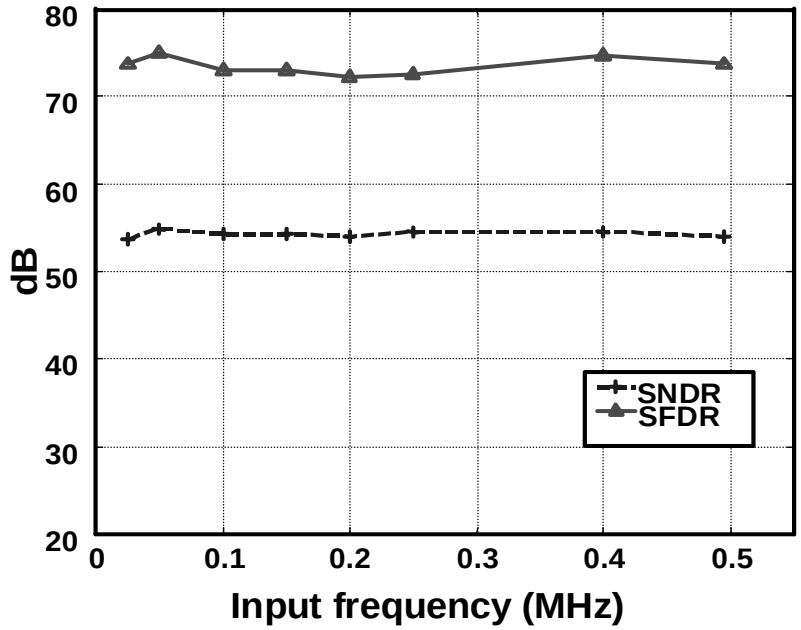


Figure 6.28 Dynamic performance vs. fin at 0.9V with fs=1MSPS.

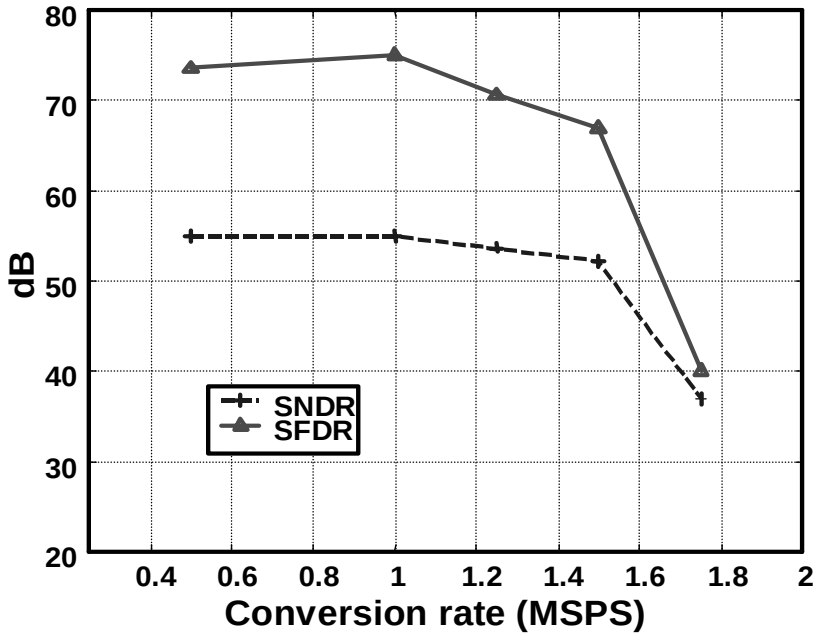


Figure 5.29 Dynamic performance vs. fs at 0.9V with fin=50kHz.

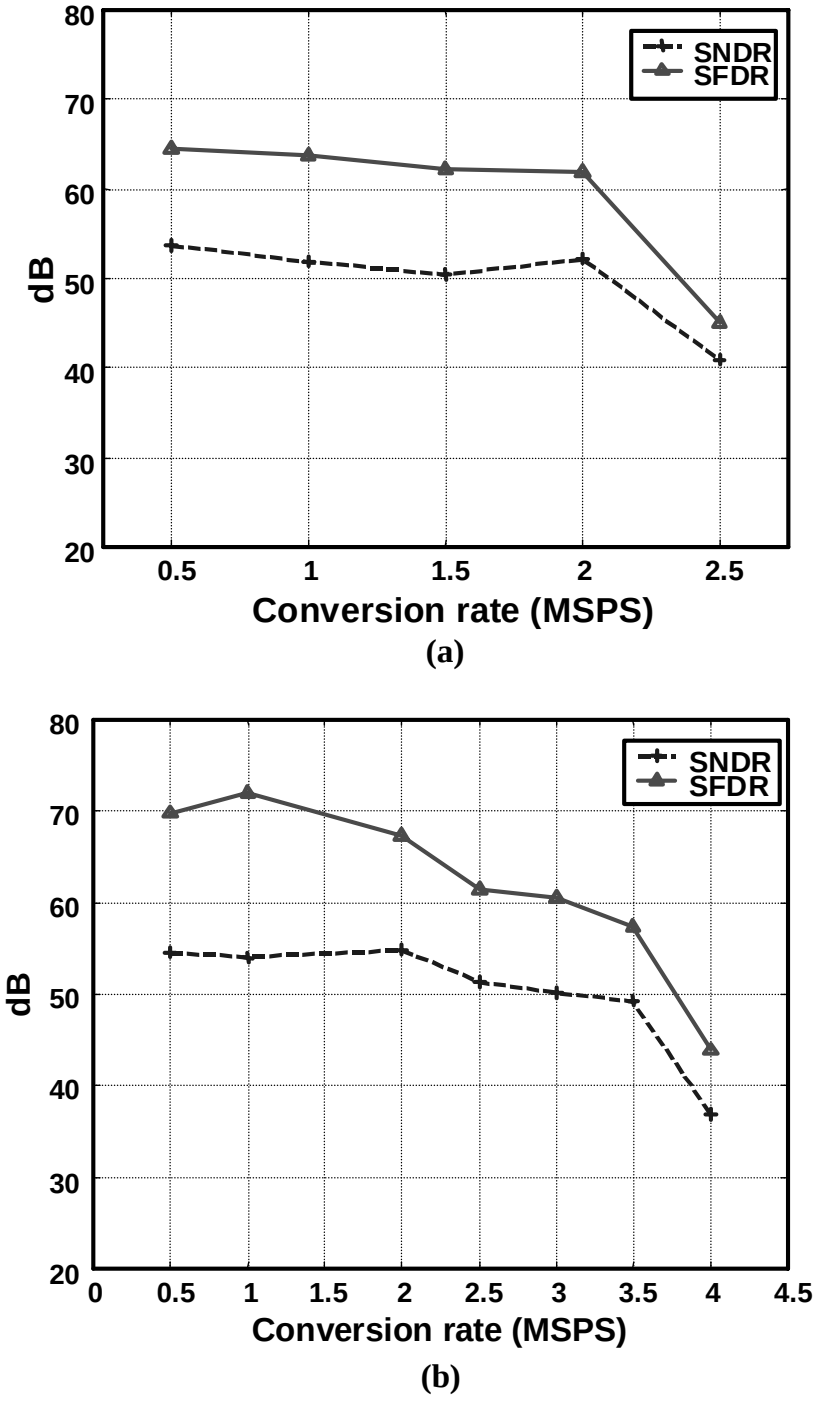


Figure 6.30 Dynamic performances under fast condition bias (a) at 0.9V supply and (b) at 1.2V supply.

Chapter 7.

Conclusions

This thesis started with a review of the device and design issues coming from recent device scaling. To overcome the low-voltage circuit design obstacles, an *Opamp-Reset Switching Technique* (ORST) has been used. The ORST does not use boosting/bootstrapping, switched-opamp, and threshold scaling techniques. It can also be free from any device reliability issues. It has been applied to several ADC designs. They are a 10-bit 25MSPS pipelined ADC and a digitally calibrated two-stage algorithmic ADC. The proposed technique is expected to be applicable to other high resolution and ultra low-voltage designs.

The pipelined ADC was fabricated in a 0.35-μm CMOS with PMOS threshold voltage of -0.9V. It employs pseudo-differential architecture. To overcome the common-mode accumulation problem, cross-coupled positive feedback capacitors were used. In this way, the common-mode level can be controlled without using any CMFB circuitry. The ADC operates at a supply voltage as low as 1.4V with a total power consumption of 21mW. The measurement results demonstrate 55dB SNR, 55dB SFDR, and 48dB SNDR.

A two-stage algorithmic ADC was also designed to verify the new radix-based digital self-calibration technique. The calibration scheme used equivalent radix architecture, major-carry measurements, and mathematical update/iteration loop. The main advantage of the technique is that it accounts for all nonlinear factors of all converting stages, such that the calibrated output will not be limited by component inaccuracy. The calibration was adapted to the low supply

condition by using bit-lookahead and offset cancellation technique. An accurate input sampling circuit was designed at the front-end to provide highly linear input signal to the ADC. The prototype was fabricated in a 0.18μm CMOS technology. The calibrated ADC demonstrates 75dB SFDR at 0.9V and 80dB SFDR at 1.2V. The total power consumption is 9mW with a clock frequency of 7MHz (1MSPS).

Although both IC measurement results showed successful realization of low-voltage analog circuits, still several issues remain to be improved in the future:

1) In spite of using cross-coupled feedback capacitors to control common-mode levels, there still exists a common-mode drift caused by capacitor mismatches, opamp offset, and charge injection. This can be initially improved by careful layout. However, a closed-loop low-voltage CMFB circuit would be the desirable solution.

2) In a deep-submicron process, turning *off* the device is sometimes as difficult as turning it *on* because of sub-threshold conduction. The leakage current is already a big burden in VLSI circuit design due to large stand-by power consumption. In analog SC circuits, this limits the resolution whose operation is based on charge conservation. A circuit-level solution is necessary for reliable low-voltage operation.

3) The radix-based calibration technique corrects capacitor mismatches, finite opamp dc gain error, and signal-independent charge injection error. However, opamp nonlinearity due to open-loop gain variation with output signal swing cannot be corrected by the calibration. It can often be improved by reducing the output swing range, which results in losing the dynamic range. In the pipelined ADC design, either adjusting the reference range in each stage or calibrating the segmented output signal range would be the straightforward solution. Finally, although the calibration is employed in the single-bit-per-stage architecture, it can be extended to the multi-bit architecture in the future.

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