Low-Voltage Switched-Capacitor Circuits

by

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To my parents.

LOW-VOLTAGE SWITCHED-CAPACITOR CIRCUITS

1. INTRODUCTION

One of the key limitations of state-of-the-art fine-linewidth CMOS technologies is the restricted power-supply voltage, limited by the low junction-breakdown voltage of the process and by the thin gate oxide, prone to voltage stress and breakdown. Also, in some applications, the available external power source may limit the supply voltage; for example, this source may be a 1.2 V battery, with an end-of-life voltage of only 0.9 V.

In analog and mixed analog-digital circuits, the circuit technique most often used for analog signal processing is based on switched-capacitor (SC) stages. They can be utilized in many applications, such as data conversion (both in Nyquist-rate and oversampled $\Delta\Sigma$ ADCs), analog filters, sensor interfaces, etc.

SC circuits use MOS switches, op-amps, and capacitors as components. In A/D converter applications, comparators are also needed. For supply voltages below about 1.5 V, the design of these components becomes quite challenging. While op-amps and comparators can be designed for supply voltages as low as 0.9 V by skillful designers [1], there are fundamental limitations on the operation of switches when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages. To illustrate the difficulty, Figure 1.1 shows a conventional SC integrator, which is the basic building block of most SC circuits. In this stage, the switches S2 - S4 can operate at a fixed low (analog ground) voltage, and hence can be turned on and off even if single-channel switches are used. However, the switches S1 and S5 operate at signal voltages which may swing from rail to rail. Hence, if the signal voltage is about half-way between the rail voltages, and $V_{Tn}+|V_{Tp}| > V_{dd}$, it may not be possible to turn the switch on, even if a CMOS transmission gate is used to realize it.

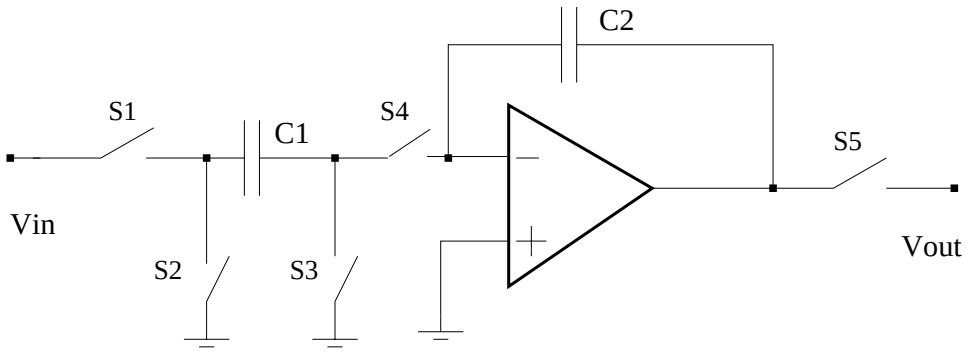


FIGURE 1.1: Conventional SC integrator

In the past, two approaches have been commonly used to bypass this problem. One used internal voltage boosting (typically, doubling) to obtain high-swing clock signals [2]. Figure 1.2 shows two kinds of clock boosting schemes.

The Dickson charge pump (Dickson CPC) shown in Figure 1.2a, was widely used to generate an on-chip voltage higher than V_{DD}. However in the low-voltage environment, the CPCs voltage pumping gain (the voltage increase per pumping stage) is degraded drastically. This limitation is overcome by the charge pump circuit(NCPC) shown in Figure 1.2b [11].

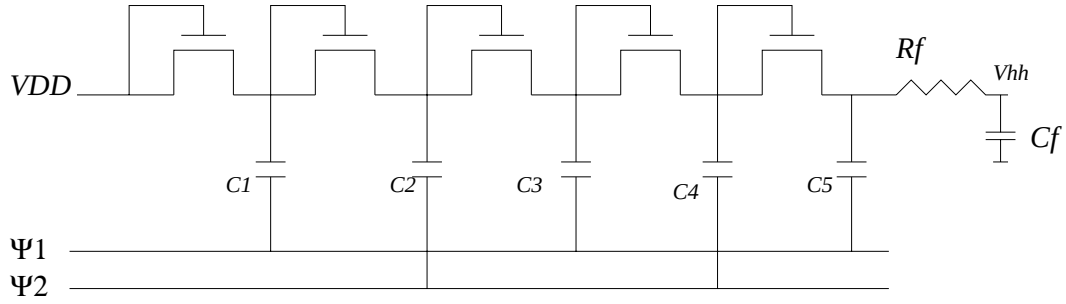
This approach is useful if the supply voltage is restricted by the source, as in the case of battery-operated devices, or by the junction breakdown only. However, it cannot be used if the gate oxide deterioration limits the permissible supply voltage.

The other alternative was the use of switched op-amps [3]. In this method the operational amplifier is turned off during reset phase. Meanwhile the sampling capacitor is discharged by shorting the opamp output to ground by means of an additional switch. This approach also suffers from some shortcomings. Specifically, the transients introduced by the required power-up/power-down of the op-amp slow down the operation, increase the required settling time, and thus reduce the speed of the circuit.

1.1. Design Objective

In our project, we are working on a third approach to realize low-voltage SC circuits. It is based on the use of a different integrator architecture, illustrated schematically in Figure 1.3a, which

(a) Dickson Charge Pumping Circuit



(b) New Charge Pumping Circuit

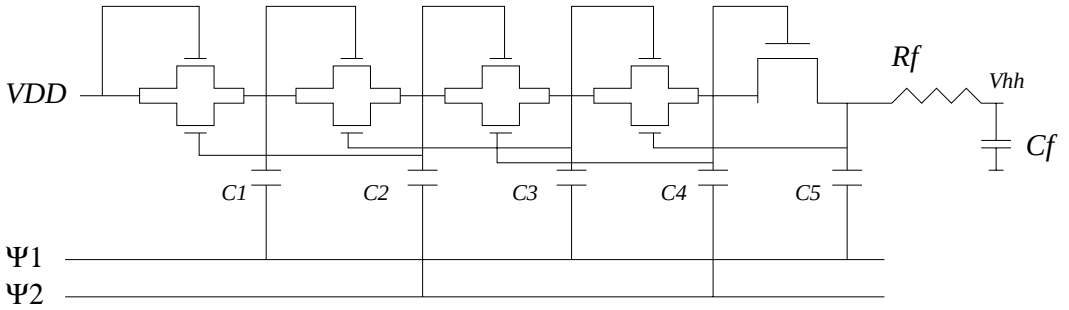


FIGURE 1.2: Charge pump circuits (clock boosting)

shows two cascaded integrators.

The clock phases are shown in Figure 1.3b. Note that the four switches S1-S4 needed for the conventional integrator stage of Figure 1.1 are replaced by the two grounded switches S_A and S_B in this circuit. This architecture was suggested earlier by Maloberti [4] for reducing the offset and 1/f noise in SC filters.

A straightforward implementation of the stage of Figure 1.3a would introduce practical problems due to forward-biased p-n junctions in the S_B switch. The objective of this dissertation is to investigate the possible solutions for this problem.

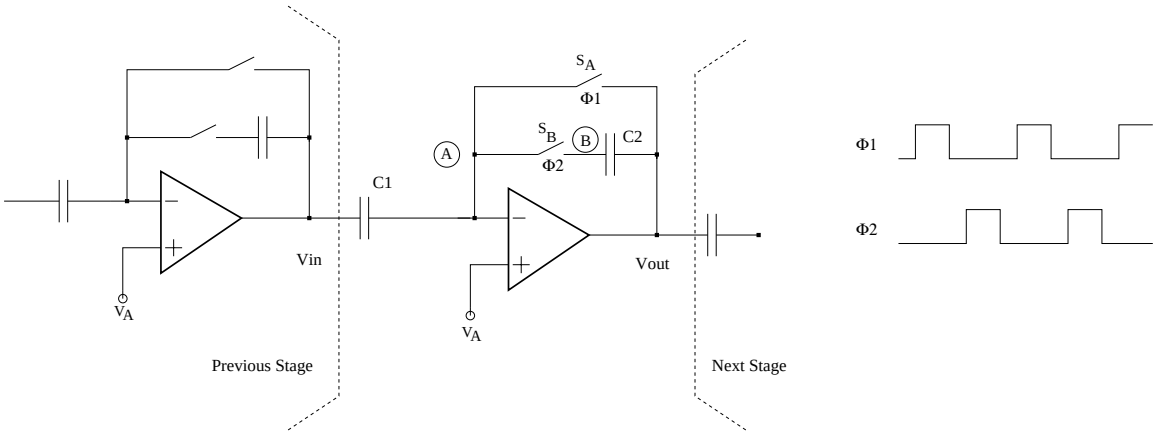


FIGURE 1.3: (a) Low-voltage SC integrator (b) Clock phases

1.2. Thesis Organization

The operation of the circuit, and the practical problem mentioned above, will be described in Section 2. Several solutions will be discussed in Sections 2.1., 2.2. and 2.3.. The application of the improved integrator stage in SC filters will be described in Section 3, and its application in $\Delta\Sigma$ ADCs will be discussed in Section 4. However, the concentration is on the integrators discussed in Sections 2.1. and 2.2.. In Section 5 the low-voltage operational amplifier and comparator used in the proposed $\Delta\Sigma$ ADCs will be described.

2. THE OPERATION AND IMPLEMENTATION OF THE LOW-VOLTAGE INTEGRATOR

Consider Figure 1.3. Let switch S_A be closed only during the period when clock phase $\Phi 1$ is high, and S_B only when $\Phi 2$ is high (Figure 1.3b). The output of the integrator $v_{out}(n-1/2)$ will be at the virtual-ground voltage V_A when $\Phi 1$ = 1. During this time, C2 is open-circuited by S_B. When $\Phi 2$ rises, C2 is reconnected and receives a charge $C1[v_{in}(n) - v_{in}(n-1/2)]$, resulting in an output voltage:

$$v_{out}(n) = v_{out}(n-1) - \frac{C_1}{C_2}[v_{in}(n) - v_{in}(n-1/2)] \tag{2.1}$$

which is the appropriate equation for an inverting delay-free integrator.

Notice that v_{in} is the output voltage of the preceding stage, which has the same architecture. Hence, if the preceding stage has the same switching sequence as the one analyzed, then $v_{in}(n-1/2) = V_A$, while $v_{in}(n)$ is the output signal voltage of the preceding stage. If the S_A switch of the previous stage is closed during $\Phi 2 = 1$, and its S_B is closed during $\Phi 1 = 1$, then the output voltage of the cascade is inverted and delayed.

Note that (at the cost of two additional switches) the right-hand terminal of C1 can be disconnected from the virtual ground and grounded during the $\Phi 1 = 1$ period. Note also that most discussions in this report refer to single-ended circuit realizations. In reality, the implementations planned will be mostly fully differential (or at least pseudo-differential [5]) structures, to achieve better noise immunity.

As mentioned in the Introduction, the obvious realization of the circuit of Figure 1.3 leads to some practical difficulties. Assume that the analog ground voltage is $V_A = V_{ss} = 0$, i.e., that the input common-mode voltage is true ground, as may be the case if the op-amps have PMOS input devices. Then the conventional realization of the circuit calls for NMOS switches for both S_A and S_B, since NMOS devices are easy to turn on when they operate at ground bias. Assume also that the output voltage at the end of a $\Phi 2 = 1$ period approaches V_{dd}. Then, at the beginning of the next $\Phi 1 = 1$ phase, V_{out} is pulled down to ground by S_A, and the floating node B (between S_B and C2) is pulled down to about $-V_{dd}$ by C2. Since node B is connected to the n+ source diffusion of

S_B, the source-to-substrate junction of S_B will be forward biased, and C2 will lose charge to the substrate.

In what follows, several techniques for avoiding the forward-biased junction problem will be described.

2.1. Integrator Realization Using a PMOS Switch and Level-Shifted Clock

A possible solution [20] to the junction leakage problem is illustrated in Figure 2.1.

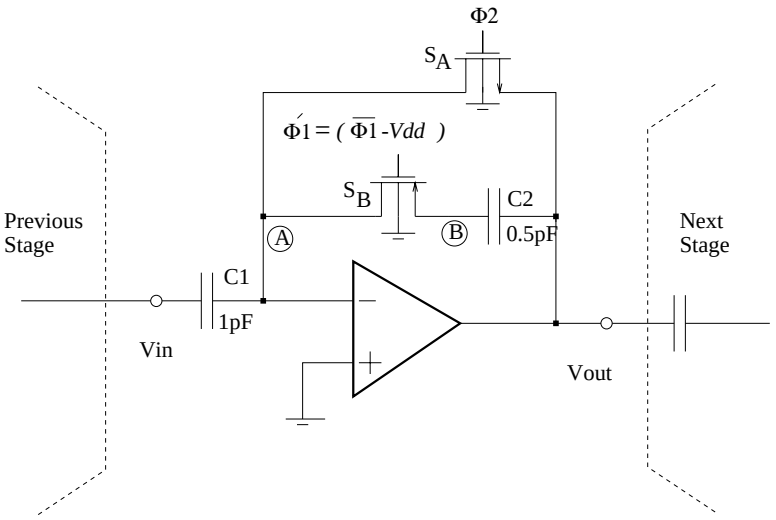


FIGURE 2.1: Low-voltage integrator with MOS switches

As before, it uses an NMOS implementation for S_A, but now a PMOS device is used as S_B. The physical details of S_B in an n-well process are shown in Figure 2.2. Clearly, now the voltage drop from 0 to $-V_{dd}$ at node B will reverse bias, not forward bias, the source-to-well junction. Hence, the charge loss from C2 is avoided.

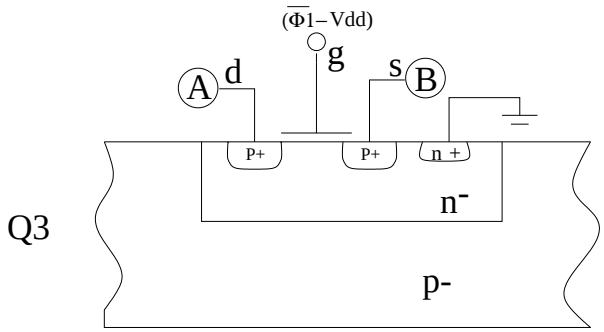


FIGURE 2.2: The realization of the PMOS switch S_B

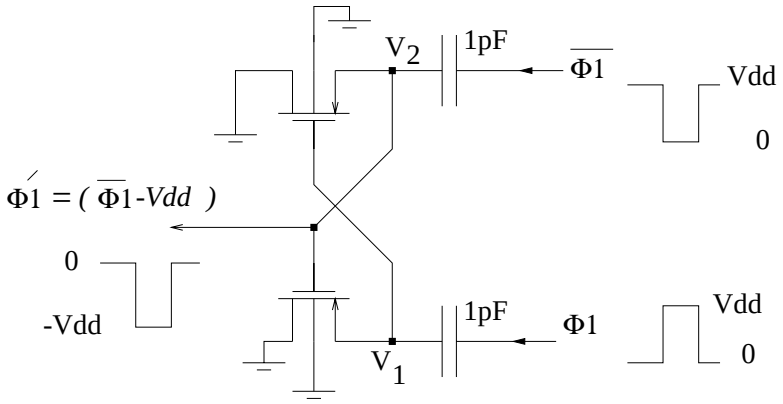


FIGURE 2.3: Level-shifted clock generator

The remaining problem is that the grounded PMOS switch device requires a negative clock voltage for conduction. This can be done by changing the clock signal variation limits. A level-shifting circuit which can be realized is shown Figure 2.3.

It is a variant of the widely-used Nakagome clock-booster stage [6]. It provides a clock signal varying between 0 and $-V_{dd}$. Analysis of this clock-shifting scheme shows that the first samples of voltages V1 and V2 after power-up will be positive, leading to charge pumping into the well from the sources of the PMOS switches (Figure 2.2). This should not be a problem as long as the well is adequately grounded. After the third or fourth clock periods, the samples of V1 and V2 become negative, and the charge pumping stops. Note that in this clock shifting scheme the voltages applied across gate-source and gate-drain are not going beyond low-voltage technology limits, and that's an advantage to the clock-boosting method.

As an illustration of the integrator operation, Figure 2.4 shows the simulated input, clock,

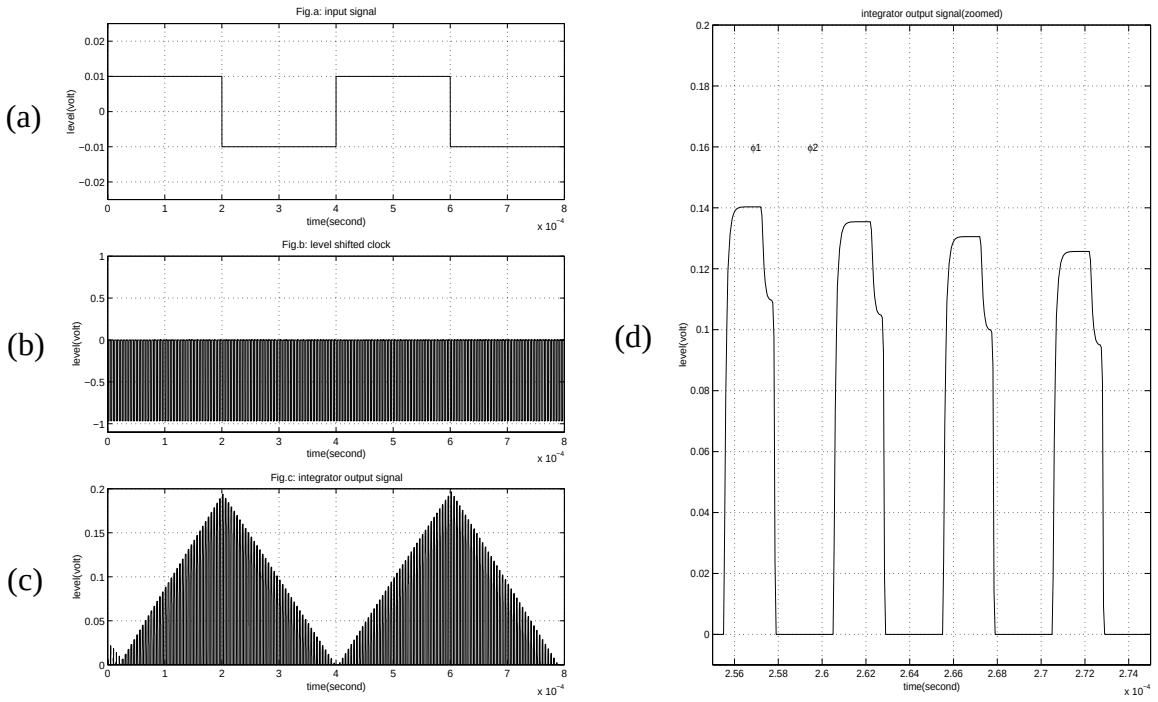


FIGURE 2.4: Simulated voltages in the integrator of Figure 2.1: (a) input; (b) clock; (c) output voltage; (d) output voltage on an expanded time scale

and output voltages of the circuits of Figures 2.1 and 2.3, under the following test conditions: C1 = 1 pF, C2 = 0.5 pF and V_{dd} = 1 V.

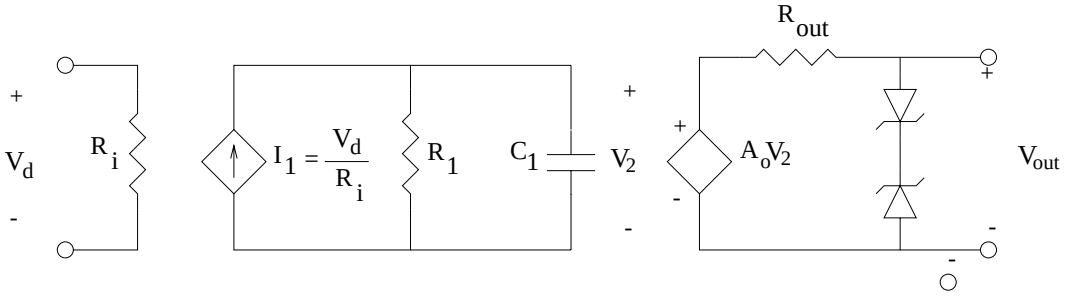


FIGURE 2.5: Op-amp macromodel used in the simulation of Figure 2.4

The input voltage was a 2.5-kHz, 20-mV p-p square wave, and the clock frequency was 200 kHz. A simple macromodel, shown in Figure 2.5, was used for the op-amp. The model component values are as follows:

$$\mathrm{R_i} = 20\ \mathrm{M\Omega}\ ,\ \mathrm{R_1} = 10\ \mathrm{K\Omega}\ ,\ \mathrm{C_1} = 0.15\ \mu\mathrm{F},\ \mathrm{R_{out}} = 1\ \mathrm{K\Omega}\ ,\ \mathrm{A_0} = 10000$$

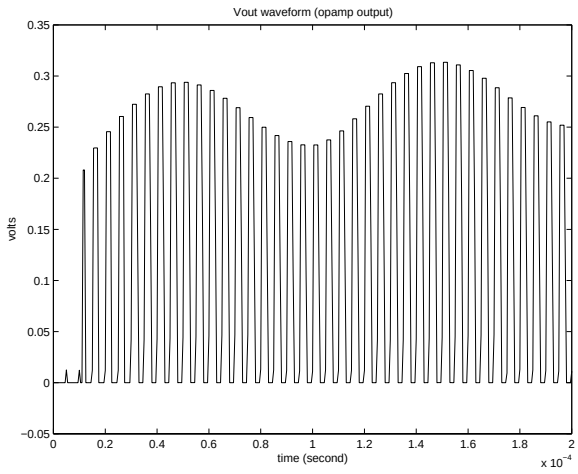


FIGURE 2.6: Simulated waveforms for a sine-wave input signal

These correspond to a dc gain of 80 dB and a unity-gain bandwidth of about 2 MHz. The models used for the switches were realistic Level 13 HSPICE ones.

Figure 2.6 shows the simulated waveforms for a 10-kHz, 20-mV p-p sine-wave input signal, under the same conditions. The illustrated waveform includes the power-up transient around t = 0.

2.2. Integrator Realization Using a Floating Voltage Supply

An alternative realization of the low-voltage switched-capacitor integrator circuits, which also avoids charge leakage, is shown in Figure 2.7.

This circuit can be implemented using only NMOS switches, since when S_A closes the output voltage rises to the reset voltage V_{dd} (rather than drop to 0 as in the previous realization), and hence the voltage at node B cannot fall below 0 V. Thus, the source-to-substrate junction of S_B remains reverse-biased under all conditions. A more detailed circuit diagram, showing also the implementation of the floating V_{dd} source in the form of the switched capacitor C3, is illustrated in Figure 2.8.

In this circuit the combination of $m16$, $m11$ and $C3$ provide a floating voltage source in order to have an output voltage equal to V_{dd}. Notice that in practical single supply circuits, $C3$ should be charged to $V_{dd} - V_{offset}$, where V_{offset} is the difference voltage between $V_{out}(max)$ and opamp virtual ground voltage.

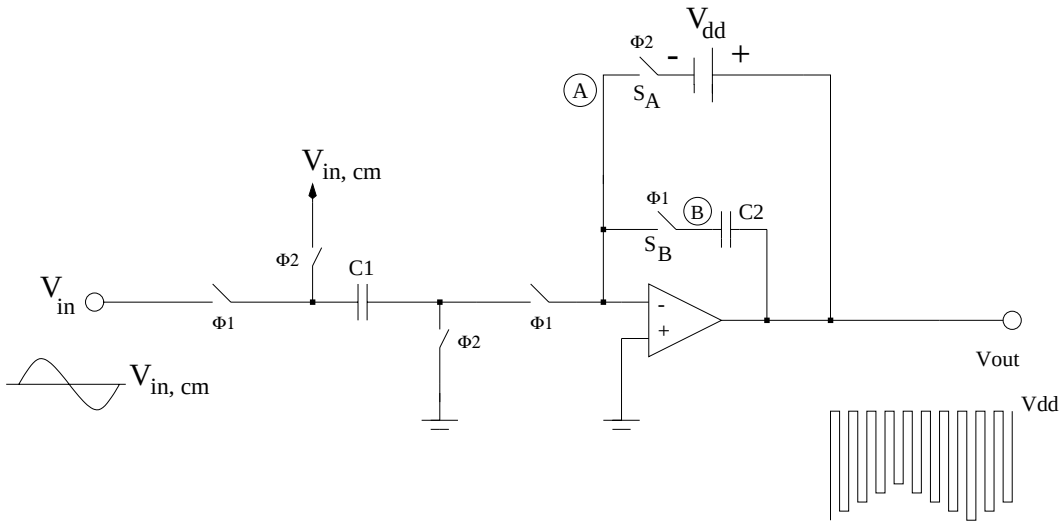


FIGURE 2.7: Low-voltage integrator using a floating bias supply

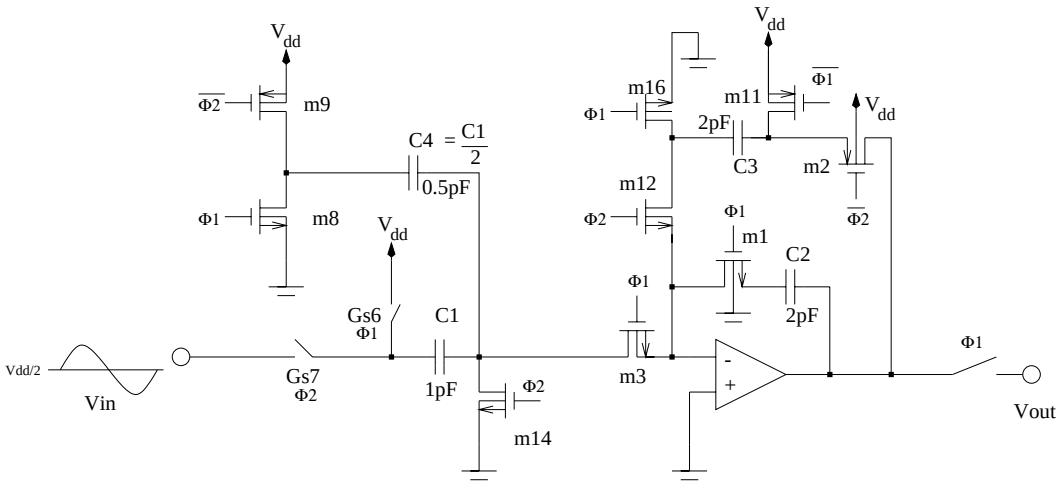


FIGURE 2.8: A possible implementation of the floating-supply integrator ($z^{-1/2}$ delay)

In the circuit shown in Figure 2.8, the dc bias of the input signal is assumed to be $V_{dd}/2$, and hence a compensating branch, realized by the SC branch containing C4, is needed to prevent the output from ramping down due to the accumulation of this input bias. Figure 2.9 shows more details of operation of this DC shifting circuit.

During the $\Phi 1$ phase, $C4$ is discharged while $C1$ is charged to V_{dd} due to its connection between opamp virtual ground and the previous SC output which should be V_{dd} during this phase. During $\Phi 2$ the amount of charge pulled from opamp virtual ground will be:

$$Q = q1 + q2 = (\frac{V_{dd}}{2} - V_{in})C_1 \tag{2.2}$$

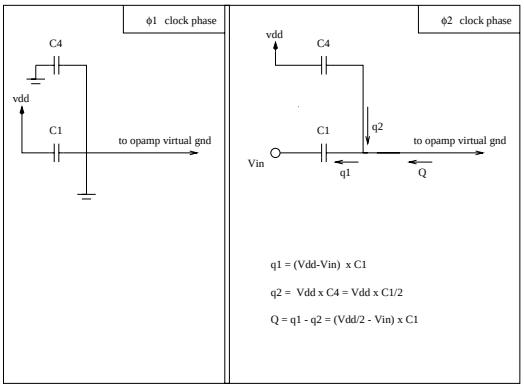


FIGURE 2.9: DC shifting circuit

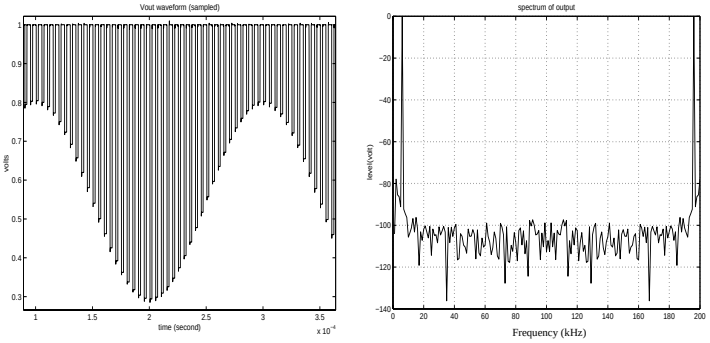


FIGURE 2.10: Simulated output in the time- and frequency-domain for the floating-supply integrator

Which imposes a DC shift equal to $V_{dd}/2$ appropriate for single supply usage. Without switch m3, C1 will loose charge through C3 during reset phase($\Phi 2$). That will cause a change in output voltage which is signal dependent, producing harmonic distortion.

This integrator induces a half-clock cycle delay ($z^{-1/2}$). By changing the clock scheme, a delay-free integrator can also be realized.

Figure 2.10 shows the simulated time- and frequency-domain representations of the output voltage of the integrator stage of Figure 2.8 for a 5-kHz, 0.2-V p-p sine-wave input voltage, under the following conditions. The capacitances were C1 = 1 pF and C2 = 2 pF, and V_{dd} was 1-V. The op-amp model was as shown in Figure 2.5, and the switch models used were HSPICE Level 13.

2.3. Integrator Realization Using Master/Slave Integrators

Yet another technique for avoiding charge leakage in the low-voltage integrator of Figure 1.3 is to use an extra op-amp stage (slave integrator) for storing the charge during the rest phase when the integrating capacitor is floating [7].

Figure 2.11a shows the schematic diagram of the circuit; Figure 2.11b illustrates the clock phases needed.

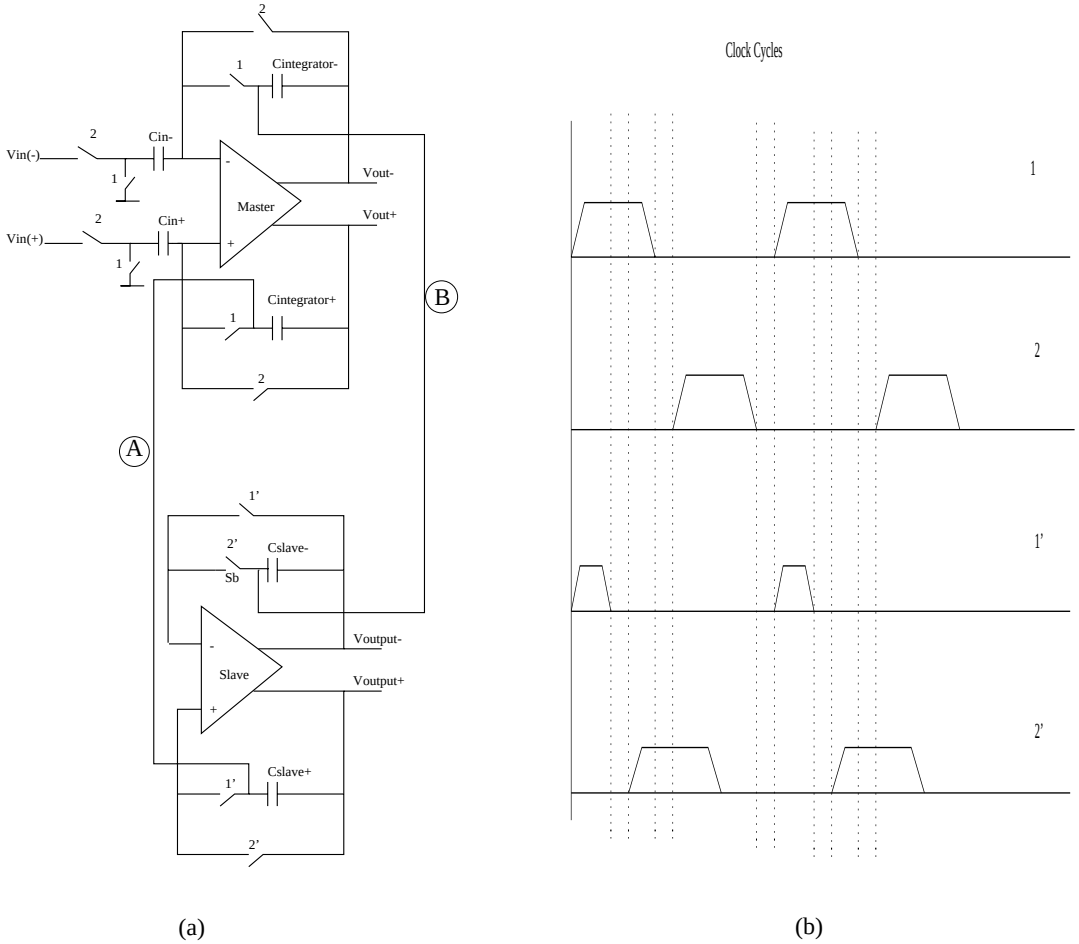


FIGURE 2.11: Master/slave integrator scheme

When Φ2 and Φ2’ rise, the signal charge stored in the master storage element $C_{\text{integrator}}$ is transferred into the slave storage capacitor C_{slave}; when clock phases Φ1 and Φ1’ rise, the charge is returned into $C_{\text{integrator}}$. The sensitive nodes A and B are kept at or near the analog ground, and charge leakage is thereby prevented.

This stage can use single-channel (NMOS) switches everywhere, since all switches operate at analog ground potential. A drawback of the master-slave structure is the need for the second integrator stage. However, it is possible to operate the structure in a double-sampling mode, in which both integrators receive input charges in alternating clock periods. For such a "ping-pong" circuit, the sampling rate can be doubled without increasing the op-amp bandwidth.

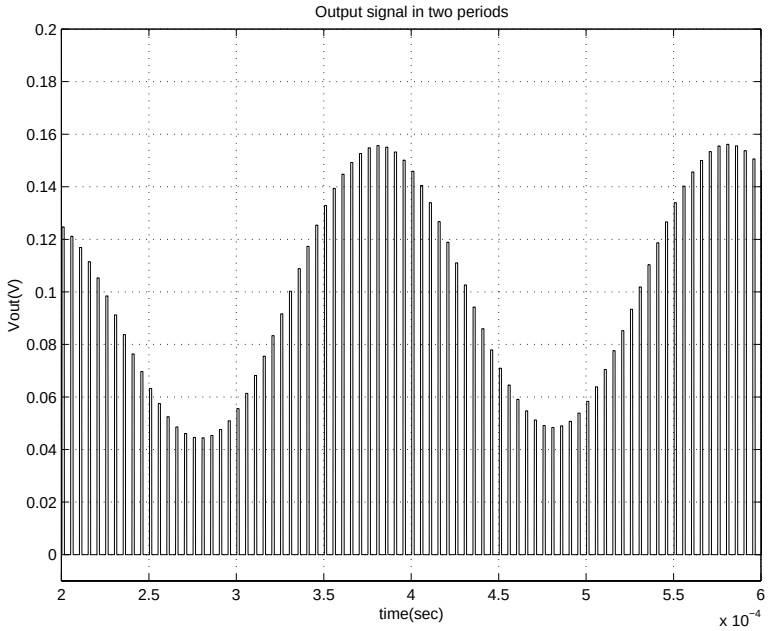


FIGURE 2.12: Output voltage for a sine-wave input signal

The performance of this integrator was simulated using HSPICE. A macro model similar to that of Figure 2.5 was used for the op-amp, corresponding to a dc gain of 80 dB and a unity-gain frequency of 100 MHz. All capacitors were chosen as 2 pF. The switches were simulated by the Level 13 model in HSPICE. Their dimensions were $\mathrm{L} = 0.6\ \mu\mathrm{m}$ and $\mathrm{W} = 10\ \mu\mathrm{m}$. The sampling frequency was 200 kHz. A 20-mV p-p 5-kHz sine wave was used as input signal. Figure 2.12 shows the output voltage over two periods; Figure 2.13 illustrates its spectrum. The low harmonic distortion verifies the absence of charge leakage. Figure 2.14 shows the output voltages for various constant input voltages, and the error as compared to the ideal response. Clearly, the performance is close to the ideal one.

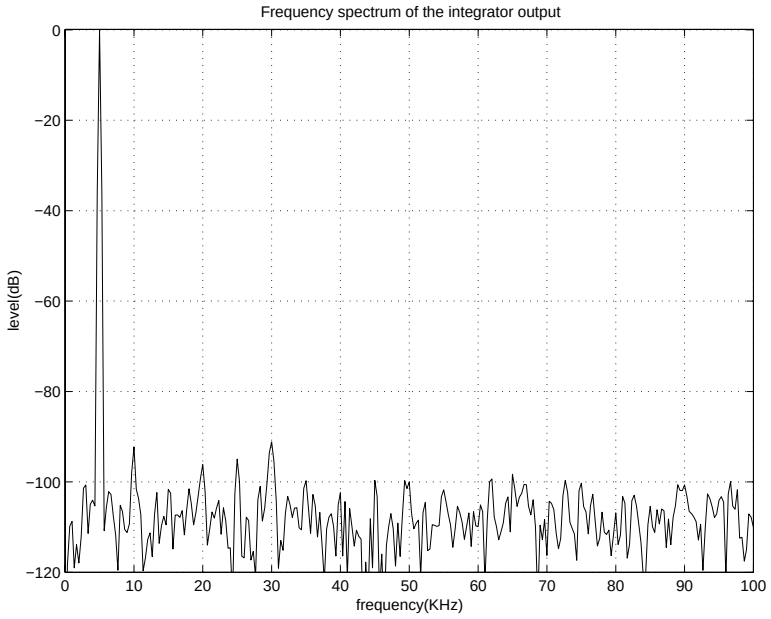


FIGURE 2.13: Output spectrum

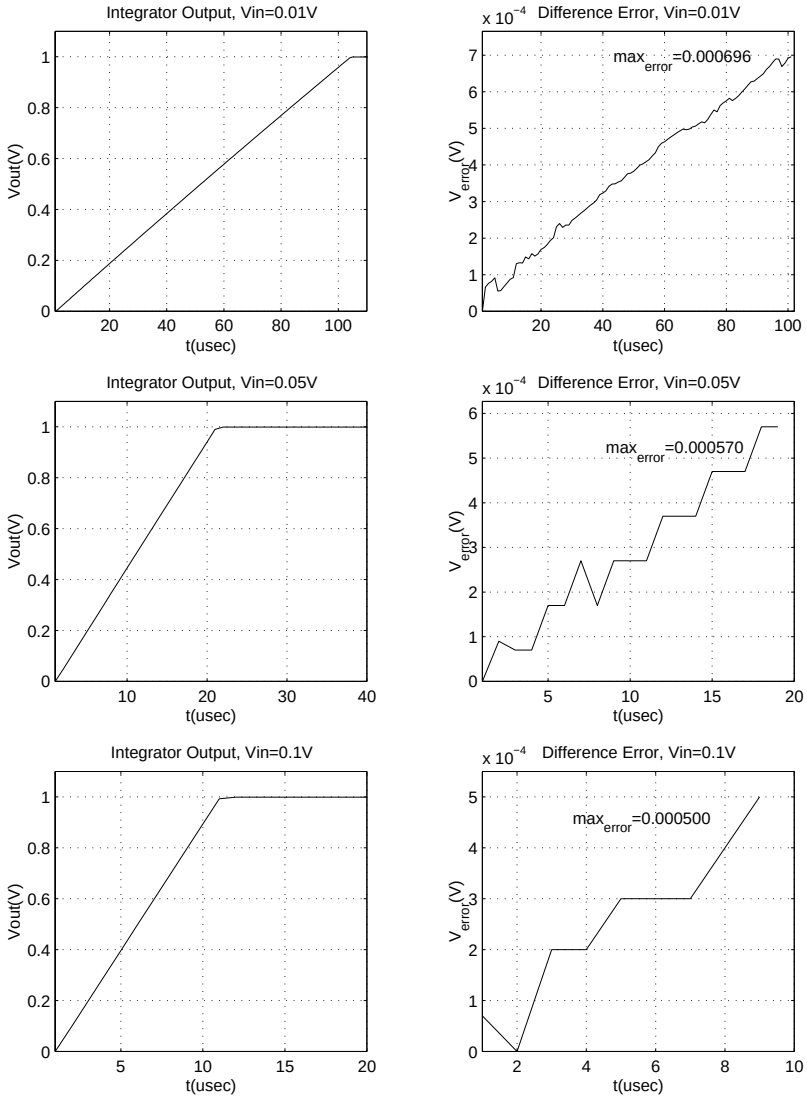


FIGURE 2.14: Output waveforms and errors for various dc input signals

3. LOW-VOLTAGE SC FILTER STAGES

Presently, the most popular approach for realizing different filter structures in switched capacitor designs are bilinear and biquad filters. A switched-capacitor filter works based on different capacitive signal flows. They have been widely discussed in many books. The main objective of this section is to exploit the methods discussed in previous sections to design very low-voltage SC bilinear and biquad filters.

3.1. Low-Voltage Bilinear Filter Stages

A general first-order switched-capacitor filter is shown in Figure 3.1. Here the switched-capacitors $C1$ and $C6$ behave as resistors, while the un-switched capacitors, $C5$ and $C2$ perform as capacitive elements.

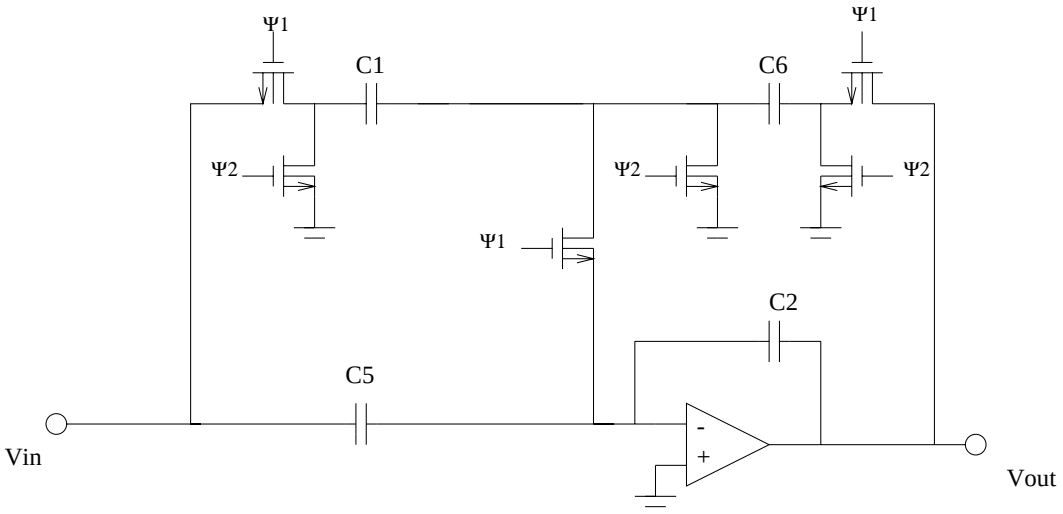


FIGURE 3.1: A traditional bilinear switched-capacitor filter

The transfer function of this filter is:

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{(\frac{C1+C5}{C2})z - \frac{C5}{C2}}{(1+\frac{C6}{C2})z - 1} \tag{3.1}$$

The low-voltage integrator circuit shown in Figure 2.8 can be readily modified and combined to obtain a switched-capacitor filter having the same low-frequency behavior.

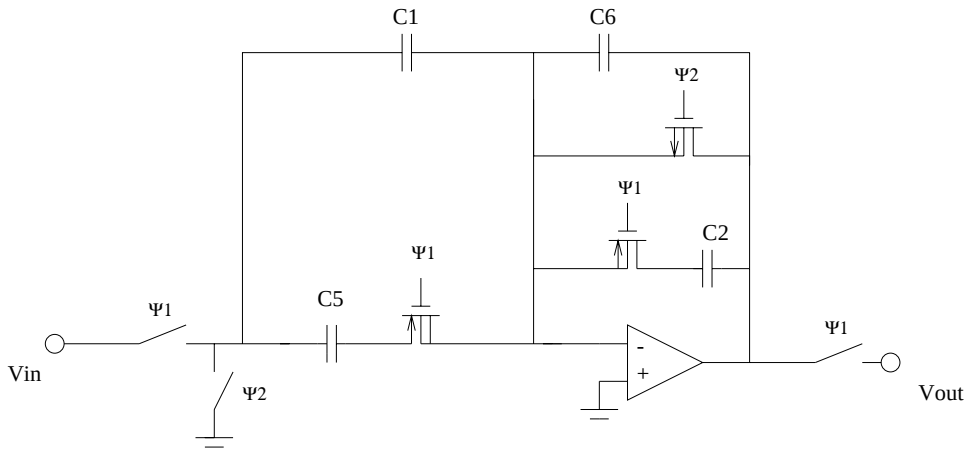


FIGURE 3.2: Bilinear SC filter section using the low-voltage integrator of Figure 2.1

Figure 3.2 shows a bilinear switched-capacitor filter using the low-voltage scheme shown in Figure 2.1. Notice that all capacitors shown in Figure 3.1 are substituted with their counterparts in Figure 2.8. Here the capacitors $C1$ and $C6$ are discharged during $\Phi 2$ and charged during $\Phi 1$, performing as resistive elements of the bilinear filter. $C5$ and $C2$ are being charged during $\Phi 1$ and will not loose their charge during $\Phi 2$, realizing the capacitive elements. For simplicity the DC shifting circuit is not shown in the scheme, however we can use the same technique discussed earlier to compensate for DC-bias applied to the integrator input.

It is also possible to realize a bilinear switched-capacitor circuit using the floating-supply low-voltage scheme (see Figure 2.8). As an illustration Figure 3.3 shows a bilinear section realizing the above transfer function. The floating supply part consists of $m2$, $m16$, $m11$ and $C3$, prividing a $V_{dd} - V_{sat}$ bias voltage between opamp output and input, during reset phase ($\Phi 2$). The combination of $m9$, $m8$ and $C4$ is used as a compensation circuit for DC-offset at input and output of the SC-filter, when a single power supply is applied. Assuming input and output signals have $V_{dd}/2$ offset voltages, C4 will be determined as:

$$\mathrm{C4} = \frac{\mathrm{C1} + \mathrm{C6}}{2} \tag{3.2}$$

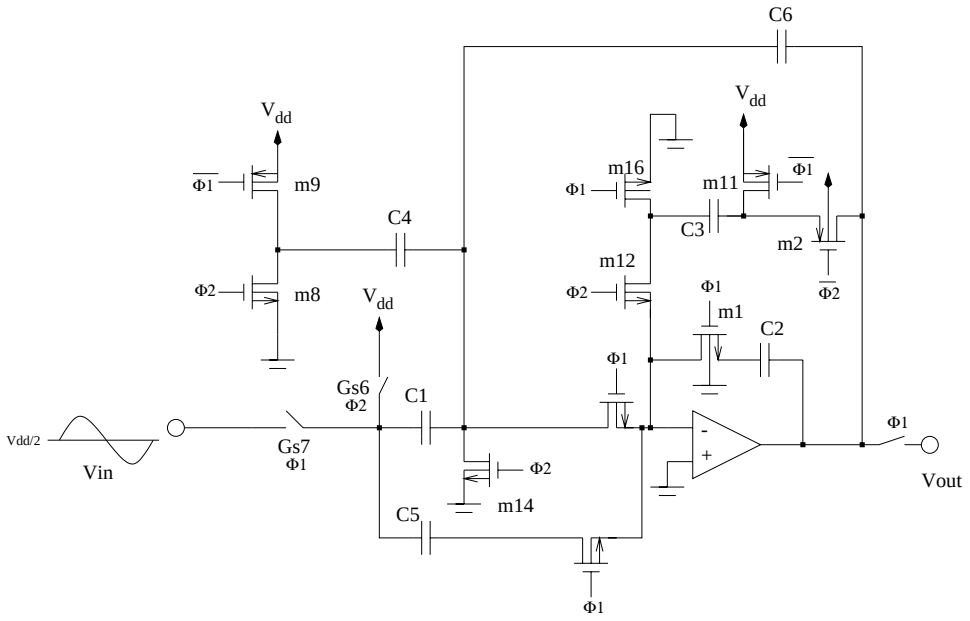


FIGURE 3.3: Bilinear SC filter section using the low-voltage integrator of Figure 2.8

3.2. Biquad Low-Voltage SC Filters

Similar to the first-order case, biquad low-voltage SC filters can be realized using the low-voltage schemes described earlier.

A direct-form continuous-time biquad filter structure should realize a transfer function

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_0}{S^2 + (\frac{\omega_0}{Q})s + \omega_0^2} \tag{3.3}$$

A switched-capacitor biquad based on this continuous-time transfer function, is shown in Figure 3.4 [19].

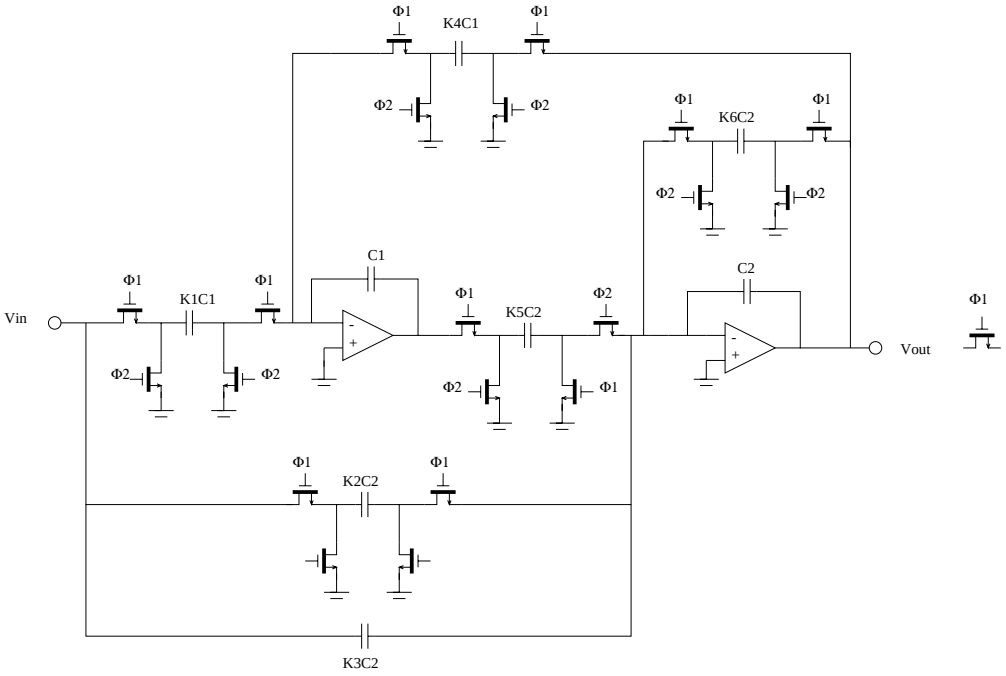


FIGURE 3.4: A low-Q switched-capacitor biquad filter (without switch sharing)

Using the signal flow graph for this circuit, the transfer function, $H(z)$ is:

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{(K_2 + K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + k_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1} \tag{3.4}$$

which follows the biquad filter transfer functions.

Matching the coefficients of this transfer function to a discrete form given by

$$H(z) = -\frac{a_2 z^2 + a_1 z^1 + a_0}{z^2 + b_1 z^1 + b_0} \tag{3.5}$$

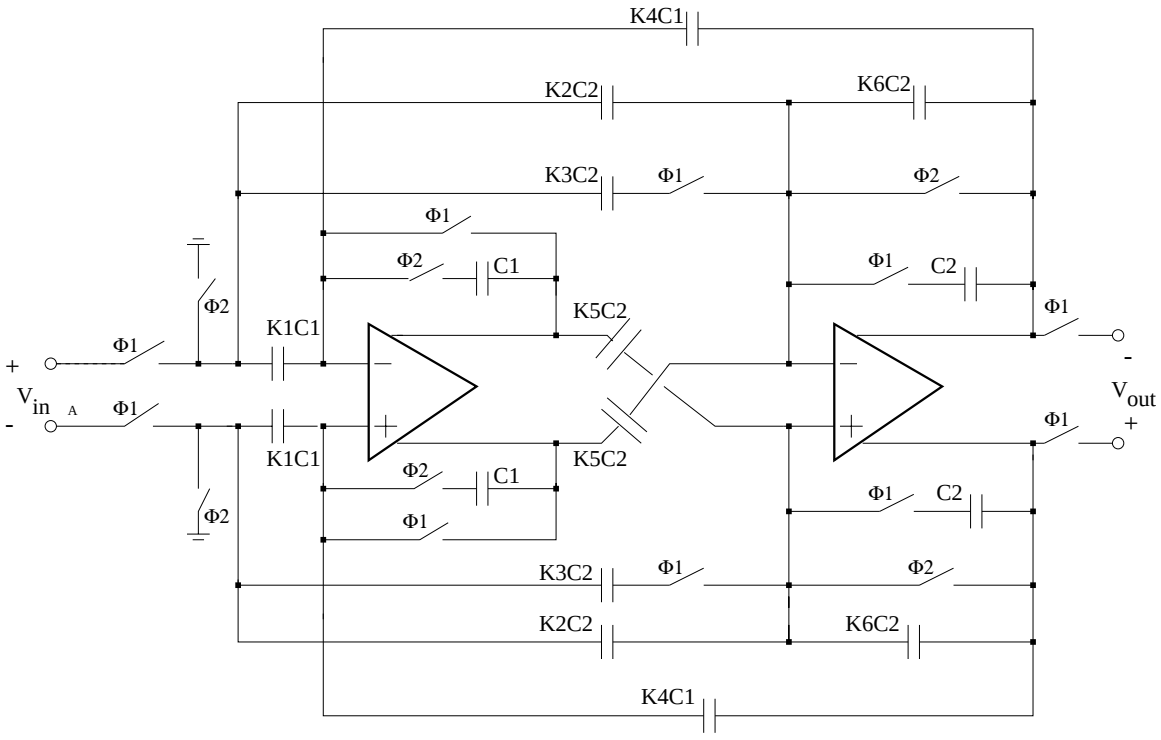


FIGURE 3.5: SC biquad using the low-voltage integrator of Figure 2.1 (differential)

yields to the following equations:

$$K_3 = a_0 \tag{3.6}$$

$$K_2 = a_2 - a_0 \tag{3.7}$$

$$K_1 K_5 = a_0 + a_1 + a_2 \tag{3.8}$$

$$K_6 = b_2 - 1 \tag{3.9}$$

$$K_4 K_5 = b_1 + b_2 + 1 \tag{3.10}$$

Using a fully differential configuration of the scheme shown in Figure 2.1 and based on the mentioned biquad structure, we can realize the low-voltage switched-capacitor biquad shown in Figure 3.5.

Here the switched in series with $C1$ and $C2$ are P-channel transistors, while the other switches are N-channel type.

The operation of this circuit was compared to an ideal biquad filter through SWITCAP simulator. The transfer function was

$$H(z) = -\frac{z^2 - 1.3672z^1 + 1}{z^2 - 1.69z^{-1} + .7566} \tag{3.11}$$

giving the values for the K's as:

$$K_1 = 1.1365 \tag{3.12}$$

$$K_2 = K_6 = 0 \tag{3.13}$$

$$K_3 = 1 \tag{3.14}$$

$$K_4 = K_5 = 0.5568 \tag{3.15}$$

Figure 3.6 shows both analyzed and simulated normalized results of this filter with a clock frequency of 200 kHz, and having ideal switches. The simulation proves the scheme's validity. Notice to the notch in the simulation result, placed at the same location as the ideal one but with a lower attenuation, which is due to the opamp finite-gain. In this example the opamp has a gain of 100 dB.

It is also possible to use the low-voltage integrators in SC ladder filters [4]. Note that in this case the series-connected switches and capacitors should be interchanged for low-voltage implementation.

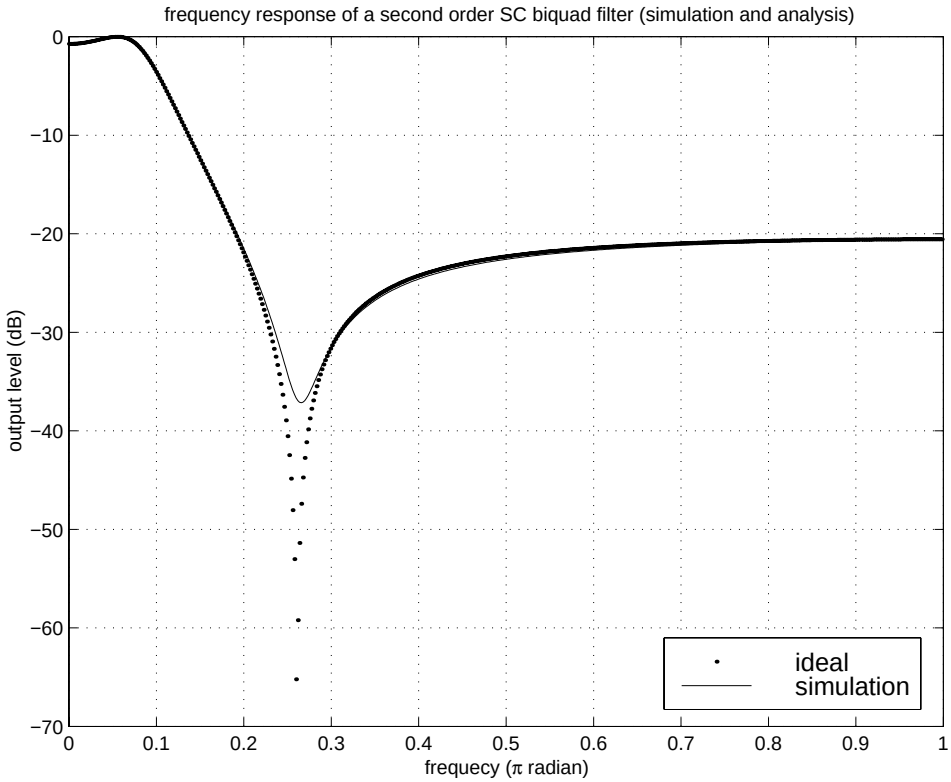


FIGURE 3.6: SC biquad filter simulation and analysis results

4. A LOW-VOLTAGE $\Delta\Sigma$ A/D CONVERTER

Analog-to-digital converters provide the cornerstone for a variety of modern circuits. In recent years the art of ADC design has been drawn to the use of switched-capacitor delta-sigma modulators. This technique is widely adopted in moderate-speed and high-performance applications. A $\Delta\Sigma$ modulator contains opamps, switches and comparators. In a very low-voltage environment, the operation of these blocks becomes problematic. In 1998, Peluso *et. al.* proposed the application of switched-opamp(SO) in a 900-mV 3^{rd}-order $\Delta\Sigma$ modulator design [1]. The pros and cons of this method were briefly discussed in the introduction.

In the following sections we show the implementation of two different second-order $\Delta\Sigma$ modulators, using the proposed low-voltage integrator schemes, clock-shifting and floating supply methods (Section 2).

4.1. Design Principles of $\Delta\Sigma$ Modulators

A linearized model of a second-order $\Delta\Sigma$ modulator block diagram using half phase delay integrators ($z^{-1/2}$) is shown in Figure 4.1 [1].

It is worth mentioning that this DSM block is structurally a little different from the traditional $\Delta\Sigma$ ADCs [9] . The use of half phase-delay integrators instead of full-phase or delay-free ones, will save on number of components in the realized circuit. However by using delay components in the digital domain, a DSM block in the traditional structure is also realizable.

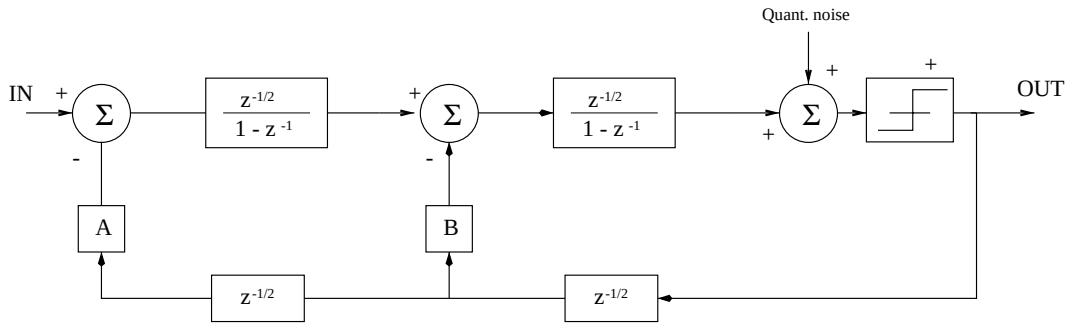


FIGURE 4.1: A second-order $\Delta\Sigma$ modulator block diagram(using half-clock delay elements)

For this DSM, the transfer function from the signal input to the output is in the form of:

$$H_S(z) = \frac{OUT}{IN} = \frac{z^{-1}}{1-(2-B)z^{-1}+(1-B+A)z^{-2}} \tag{4.1}$$

and the transfer function from the quantization noise to the output is:

$$H_N(z) = \frac{OUT}{Quant.Noise} = \frac{(1-z^{-1})^2}{1-(2-B)z^{-1}+(1-B+A)z^{-2}} \tag{4.2}$$

By choosing

$$A = 1 \quad , \quad B = 2, \tag{4.3}$$

a signal loop-gain of 1 will be determined, while the quantization noise will be shaped by a second-order filter characteristic defined as:

$$H_N(z) = (1-z^{-1})^2 \tag{4.4}$$

4.2. Signal Scaling

Using ideal integrators, a MATLAB simulation of the $\Delta\Sigma$ modulator in Figure 4.1 shows a signal swing of 5V p-p, which is not applicable in low-voltage designs. A solution to this problem is the use of signal scaling in order to decrease the voltage swing at the quantizer and integrator output terminals. A scaled version of the architecture of Figure 4.1 is shown in Figure 4.2.

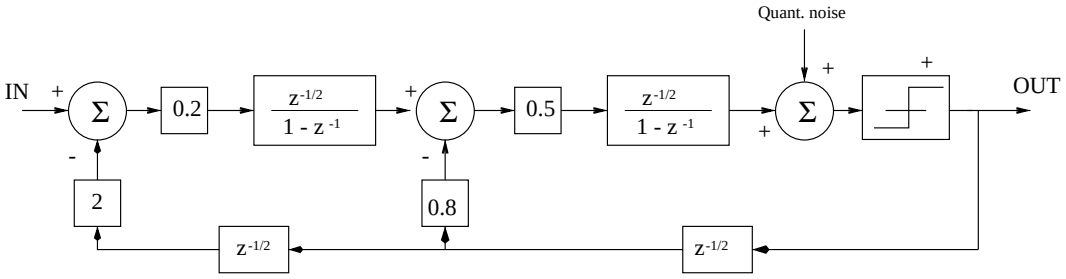


FIGURE 4.2: Low-voltage $\Delta\Sigma$ A/D converter block diagram

Since this circuit has to work with a single power supply voltage, a DC-offset voltage is defined for all input and output signals, for which the integrators should be compensated. It is done by adding DC-bias circuits to the integrators inputs (Section 2). The modified $\Delta\Sigma$ ADC block has the same noise and signal transfer functions to the one shown in Figure 4.1.

Using ideal elements, Figure 4.3a shows the signal waveforms at the first and second integrators outputs. Figure 4.3b shows the delta-sigma loop output spectrum. Here, MATLAB was used as simulator.

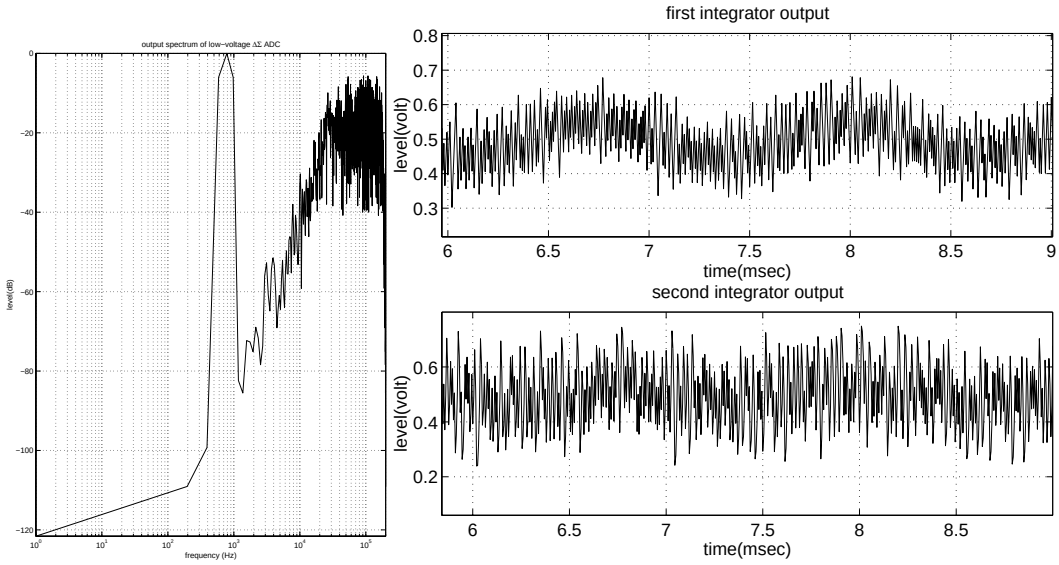


FIGURE 4.3: a: $\Delta\Sigma$ output spectrum b: integrator output waveforms

MATLAB simulation shows that using the above parameters yields integrator output swings to be in the range of low-voltage op-amp characteristics. Here, the power supply voltage is assumed to be 1 volt. In this scheme the comparator low and high levels are defined as zero and V_{dd} respectively.

4.3. Circuit Realization of a Low-Voltage $\Delta\Sigma$ A/D Converter

Using the low-voltage schemes presented in section 2, we can realize the DSM block described above. In this section, two such realizations will be presented.

4.3.1. Low-Voltage DSM using P-Channel Scheme

Following the idea given in the DSM block diagram shown in Figure 4.2, and using the clock-shifted integrator described in Section 2.1., it is possible to design a low-voltage second-order $\Delta\Sigma$ modulator. A complete circuit realization of a differential $\Delta\Sigma$ A/D converter, is shown in Figure 4.5. The utilization of a fully-differential configuration provides superior noise immunity and adds 3 dB to the dynamic range. Notice to the DC level-shifting circuits which were added to the inputs of both integrators in order to limit the output signal swings in the range of 0 to V_{dd}, suitable for single-supply operation. The clock scheme shown in Figure 4.4 describes the timing of the operation.

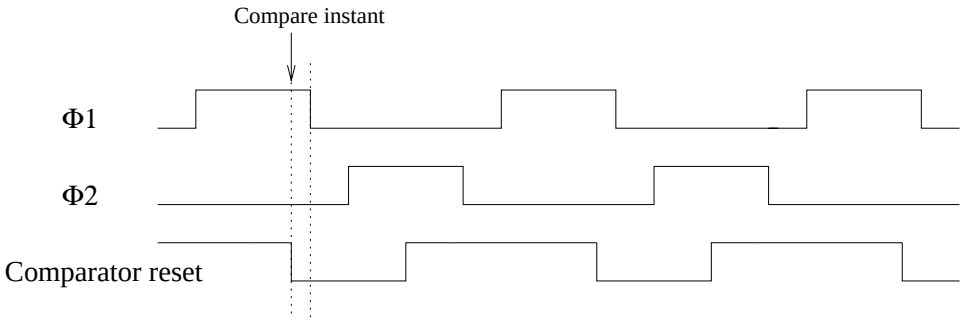


FIGURE 4.4: Clock phases used in $\Delta\Sigma$ ADC shown in Figure 4.5

Each integrator produces a half clock phase delay. The comparator incorporated with its input biasing circuit, including S15, S16, S17 and C23, generates another $z^{-1/2}$ delay. A half clock cycle delay is also generated by the edge-triggered SR flip-flop U1, which is clocked by $\Phi 2$.

To verify the operation of the circuit, it was simulated using MATLAB under the following

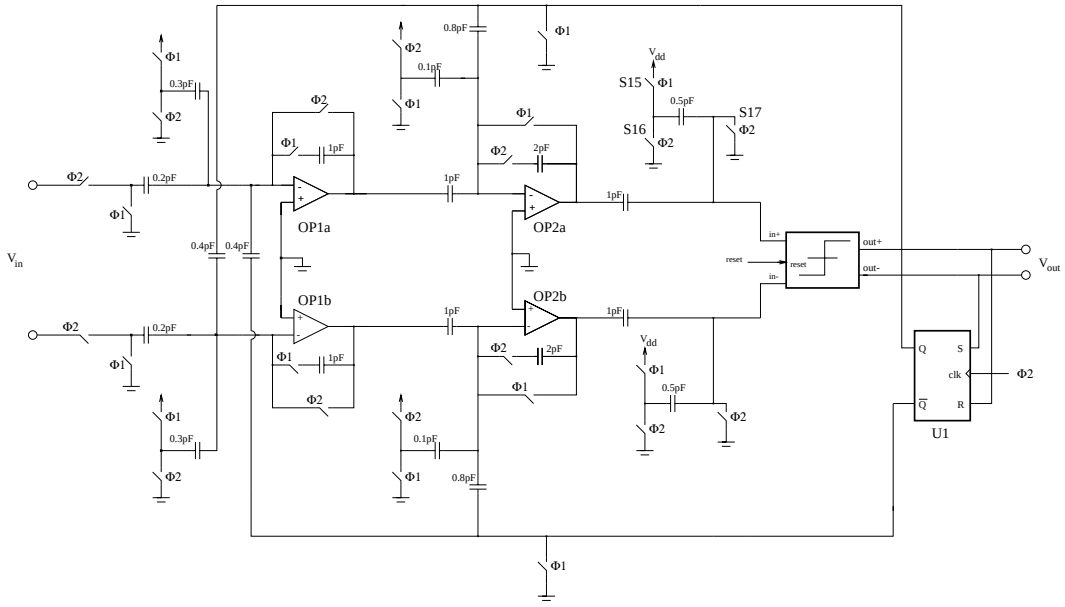


FIGURE 4.5: 1-V power supply $\Delta\Sigma$ ADC (p-channel scheme)

conditions: sampling frequency f_s = 200 kHz and a sine-wave input signal with $f_i = 781.25$ Hz. The opamp model was the same as illustrated in Figure 2.5. The output spectrum is shown in Figure 4.6.

It was also simulated using HSPICE. Simulating the first 200 pulses, the proper operation of the switches in a 1-V supply voltage was verified.

4.3.2. Low-Voltage DSM using N-Channel Scheme

Figure 4.7 shows another possible implementation of second-order $\Delta\Sigma$ ADC. The integrators in this scheme follow the idea discussed in Section 2.2. (see Figure 2.8). One advantage of this circuit over the previous one is that because of the difference voltage between opamp input and output, the opamp's analog ground could be set to real ground instead of a non-zero V_{ss}, which is a great advantage in low-voltage design. For simplicity, a single-ended implementation is shown; however a pseudo differential one is also realizable. A DC-biasing circuit at the comparator input, consisting of S15, S16, S17 and C16, compensates the DC-offset of the second integrator's(OP2) output. The combination of this biasing circuit and the comparator, introduces another $z^{-1/2}$ delay.

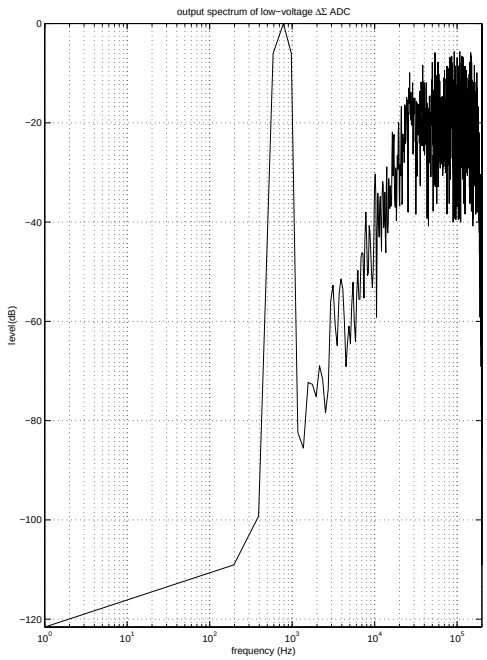


FIGURE 4.6: $\Delta\Sigma$ output spectrum

Yet another half clock cycle delay is needed to completely realize the block diagram of Figure 4.1. This is done by the edge-triggered SR flip-flop U1, which is clocked by $\Phi 2$.

The clock scheme is the same as the one shown in Figure 4.4. The low-voltage opamp and comparator structures are described in Section 5. The design was for fabrication in a 0.28 μm and 2.5 V CMOS process. The clock frequency was set to 2 MHz. The signal bandwidth was 300 Hz - 4 kHz, which is the nominal bandwidth for voice signal applications. The oversampling ratio (OSR) was of the order of 200. Since the objective was to verify by simulation the performance of the low-voltage integrator scheme, we avoided utilizing any special technique for better SNR performance. As it was mentioned earlier, V_{ss} was defined as 0 V, and we expect to have a reasonable effective voltage on CMOS switches. The threshold voltage for n-channel transistors is 0.55 V and for p-channel is about 0.9 V. Using a process with lower p-type threshold voltage, one can realize lower voltage circuits. For simplicity, the reference voltage (comparator output voltage level), was defined V_{dd}. However this will increase the risk of noise coupling into the circuit from the power supply lines. The simulated output waveforms are shown in Figure 4.8.

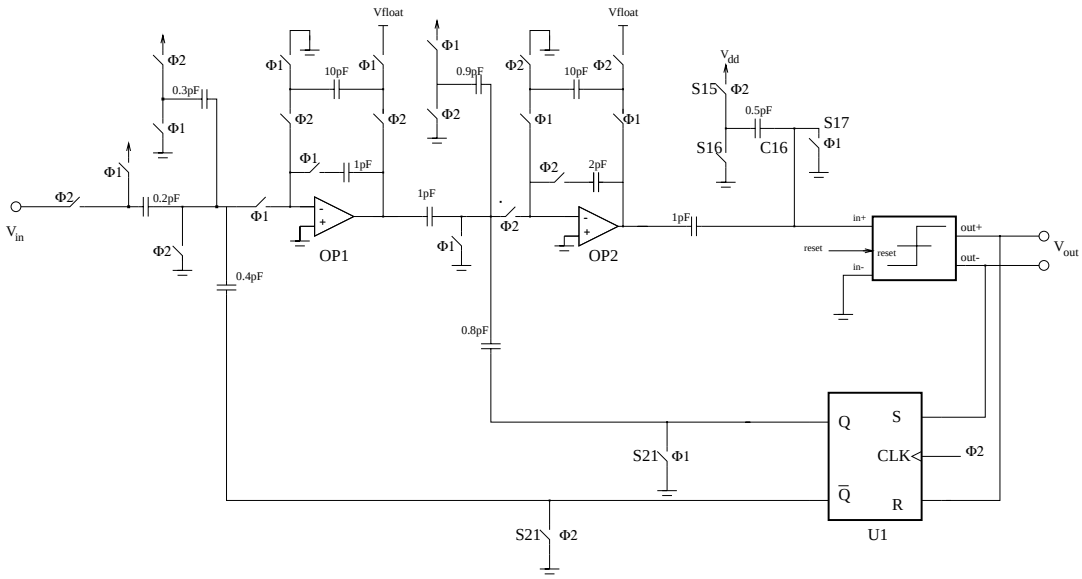


FIGURE 4.7: A low-voltage second-order $\Delta\Sigma$ ADC (n-channel scheme)

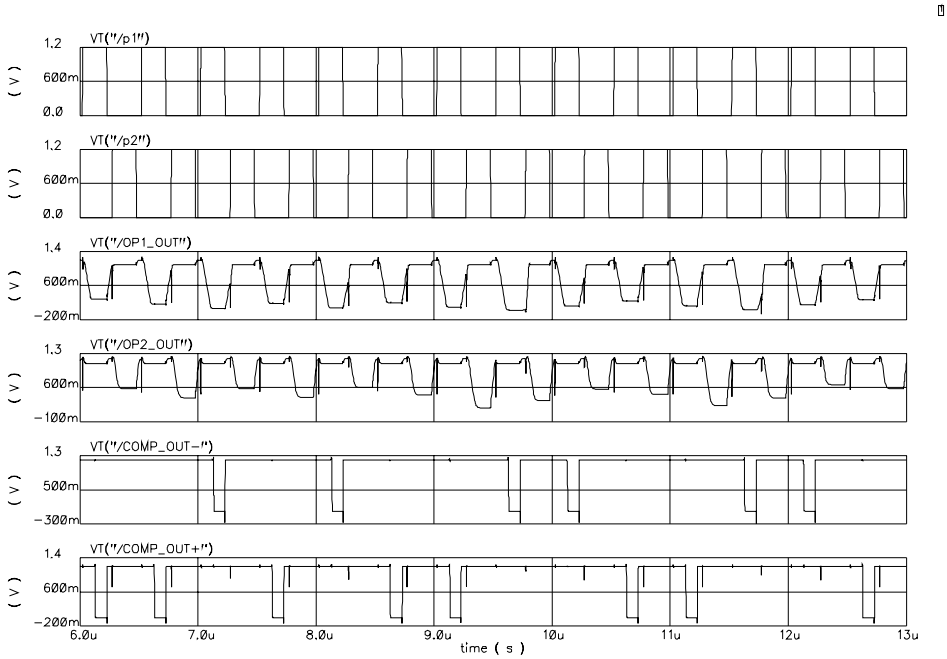


FIGURE 4.8: Waveforms at the opamp and comparator output terminals

5. LOW-VOLTAGE OPAMP DESIGN

Obviously, in order to use the low-voltage switched-capacitor scheme in high-frequency applications, the design of the opamp will be the key task. Also, any nonidealities of the opamp as the core of the active integrator, can lead to a deviation of the frequency response of the switched capacitor filters from the desired one (however there are techniques to reduce this problem [12]).

In general, large bandwidth and dc gain, high-speed common-mode feedback, relatively large output voltage swing and a good phase margin are some of the key issues. Because of restricted low power supply voltage, many traditional designs are not applicable.

The finite gain of the opamp makes the integrators leaky, and so it is an important issue in switched-capacitor designs.

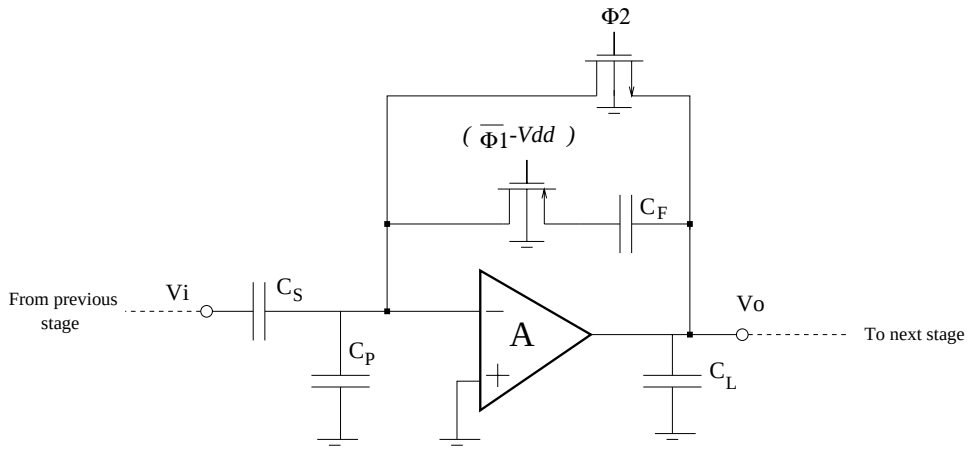


FIGURE 5.1: A low-voltage integrator block

Figure 5.1 shows a SC integrator with its associated parasitic capacitors . Its transfer function is:

$$\frac{V_o(z)}{V_i(z)} = \frac{1}{1+1/Ag}(\frac{C_s}{C_f})\frac{z^{-1}}{1-(1+1/Ag)z^{-1}} \tag{5.1}$$

$$g = \frac{C_f}{C_f + C_s + C_p} \tag{5.2}$$

A = opamp DC gain

C_P = opamp input parasitic capacitance

C_L = opamp output parasitic capacitance

The equation shows that higher loop gain Ag, reduces leakage. The integrator leakage degrades the low frequency noise suppression and lowers the overall SNR. As was mentioned earlier, this leakage is critical in case of SC biquad filter, but in delta-sigma design concept when the cascade architecture is used, the minimum gain required is much lower. For instance, in a second-order $\Delta\Sigma$ ADC a minimum gain of few hundred should be sufficient to achieve an overall SNDR of 95 dB [10].

The transient response and settling time of integrators are other important design parameters. They depend on the finite unity-gain frequency and phase characteristics of the amplifier. In the integrated amplifiers proposed in Section 2, during the reset phase the amplifier is set into its unity feedback configuration in which its phase and frequency response correspond to the opamp phase margin and unity-gain bandwidth. Care must be taken to avoid an oscillatory step response, since this leads to a long settling time.

These concepts are comprehensively discussed in many books and papers. The goal of this thesis is to investigate the application of new proposed schemes in low-voltage applications. Hence a novel low-voltage amplifier [10] with a few modification will be employed.

5.1. Low-Voltage Current Sources

In a low-voltage environment, traditional current sources suffer from their required drain-source voltage which should be larger than the compliance voltage (the minimum voltage required

Current Source Type	R_{out}	$V_{compliance}$
Simple	r_o	$V_{DS_{sat}}$
Cascode	$r_o^2 g_m$	$2V_{DS_{sat}} + V_T$
Regulated Cascode [16]	$r_o^3 g_m^2$	$2V_{DS_{sat}} + V_T$
Generalized Cascode [17]	$r_o^2 g_m^2$	$2V_{DS_{sat}}$
Active Regulated Cascode [18]	$Ar_o^2 g_m^2$	$2V_{DS_{sat}}$
Fan You method [15]	$r_o^2 g_m^2$	$V_{DS_{sat}}$

TABLE 5.1: Comparison of typical current sources

for a current source to operate). Several techniques have been proposed to prevent the output transistor in the current mirror from going into its triode region while having a wide swing output voltage.

Table 5.1 compares the output resistance (R_{out}) and minimum drain-source voltage of different current source topologies. As can be seen the method proposed by Fan You *et. al.* in 1997 [15] has the lowest compliance voltage, while introducing a rather high output resistance. However this current source has a more complex structure than the others.

5.2. Low-Voltage Opamp

In switched-capacitor circuits, opamps are designed to drive only capacitive loads. This simplifies its structure, since there is no need to have an output voltage buffer. These amplifiers are refered as transconductance opamps, or Operational Transconductance Amplifiers (OTAs).

It is possible to incorporate wide-swing current mirrors into folded-cascode amplifiers. The complete circuit is shown in Figure 5.2. It is basically a differential-input single-ended output two-stage Miller-compensated opamp [10]. The input differential pair consists of M1 and M2, while a low-voltage current mirror(M3-M4-M5-M8) realizes a differential- to single-ended transformation. The pair M5, M3 acts similarly to a diode-connected transistor at the input side of the mirror. The arrangement of n-type transistors M5 and M6 forms a folded current mirror , cascoded with the

input p-type transistor pair, M1 and M2. The use of opposite type transistors allows the drain of M6 to be at the same bias voltage as drain of M2. This is important especially when the opamp is supposed to work at very low power-supply voltages. A folded-cascode amplifier is basically a single gain stage. In this amplifier, the inverter M12 and M11 forms the second gain stage.

Excluding the output node, all nodes have relatively low impedance resulting in low voltage swing, which is appropriate for low power-supply voltages.

All MOS devices operate in saturation, and their sizes are the following:

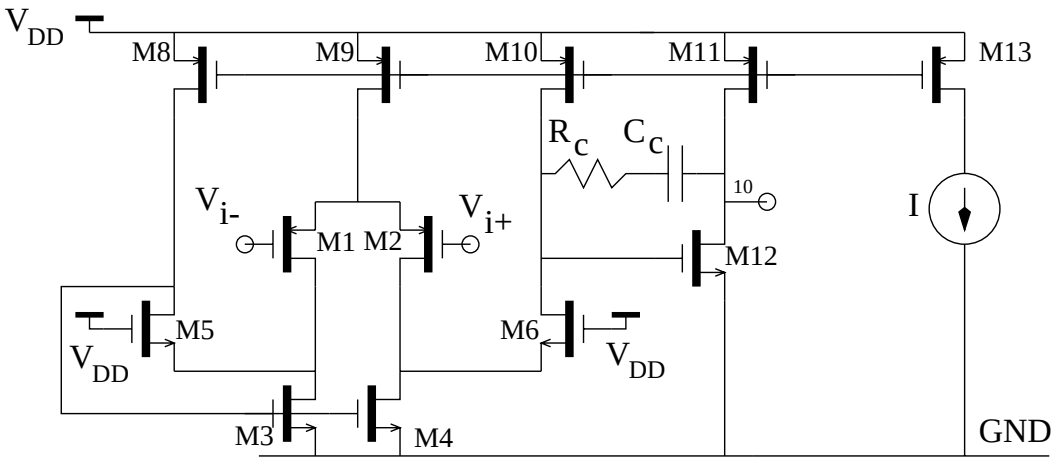


FIGURE 5.2: A low-voltage opamp

$M1/M2$	$400/0.28$
$M3/M4$	$100/1$
$M5/M6$	$14/0.5$
$M8/M10$	$100/16$
$M9$	$300/1$
$M12$	$100/0.28$
$M28$	$400/1.5$

This circuit was simulated using Cadence tools in 0.28 μm Lucent CMOS technology. The power-supply voltage was 1.2 V, and a 1.2 pF capacitor was used as the load. Figure 5.3 shows the frequency and phase response of the opamp.

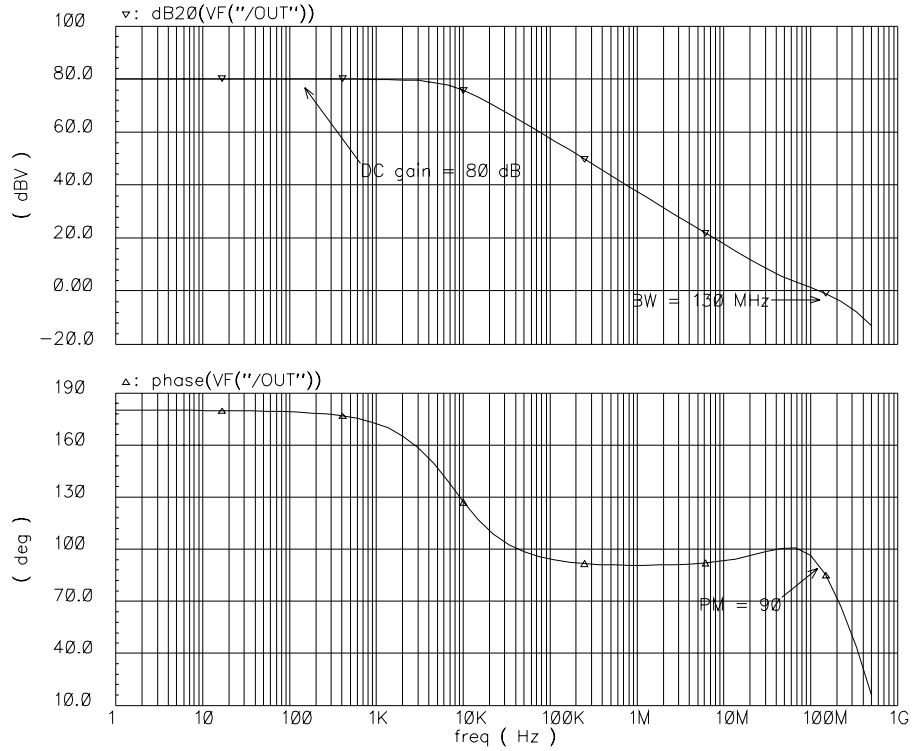


FIGURE 5.3: Opamp frequency response

A DC gain of 80 dB with 90 degree of phase margin and 130 MHz unity-gain bandwidth guarantees its operation in an audio-frequency second-order $\Delta\Sigma$ ADC with about 4 kHz signal bandwidth and an OSR of 100. Obviously the output signal swing is limited between $V_{dd} - V_{DSsat}$ to V_{DSsat}. The maximum input common mode voltage is $V_{dd} - V_{DSsat} - V_{th}$.

5.3. Low-Voltage Comparator

In $\Delta\Sigma$ modulators the comparator is used as a 1-bit quantizer. Since it appears after the loop gain block and before the output terminal, nonidealities associated with it are shaped by the loop in the same way that the quantization noise which it produces is shaped. That means that its nonidealities are reduced, and practically of less importance [14]. On the other hand any hysteresis in the comparator will cause significant distortion in the $\Delta\Sigma$ output. In low-supply voltages, resetting the comparator by shorting the nodes of the regenerative loop cannot be done, since the reset switch can not be closed. A low-voltage comparator [1] which avoids this problem is shown in Figure 5.4.

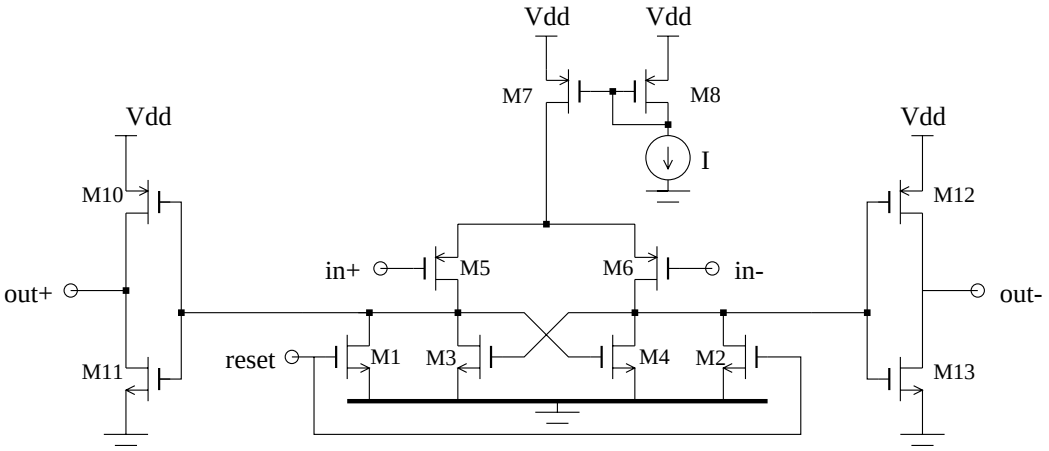


FIGURE 5.4: Low-voltage Comparator

In this scheme, the reset is done by shorting the output nodes with M1 and M2. Suppose the in+ input has a higher voltage than the in- input. After resetting, M6 will conduct first, and in a regenerative sequence the gate input of M3 will go high, pulling down the M4 gate. The inverter pairs, M10-M11 and M12-M13 are used in order to avoid that the comparator outputs be load dependent. Notice the common-mode voltage requirement on the circuit. It is obvious that we need a voltage shifting block similar to the one described earlier, to bring the common mode voltage to V_{ss}.

To test this circuit, a reset clock signal with a frequency of 2 MHz and an input signal with a 1 mV amplitude and 200 kHz frequency was applied. Figure 5.5 shows the input,clock and output

signals. Two 1 pF load capacitors were placed at the comparator OUT+ and OUT- outputs. It is obvious that the comparator outputs are high during reset.

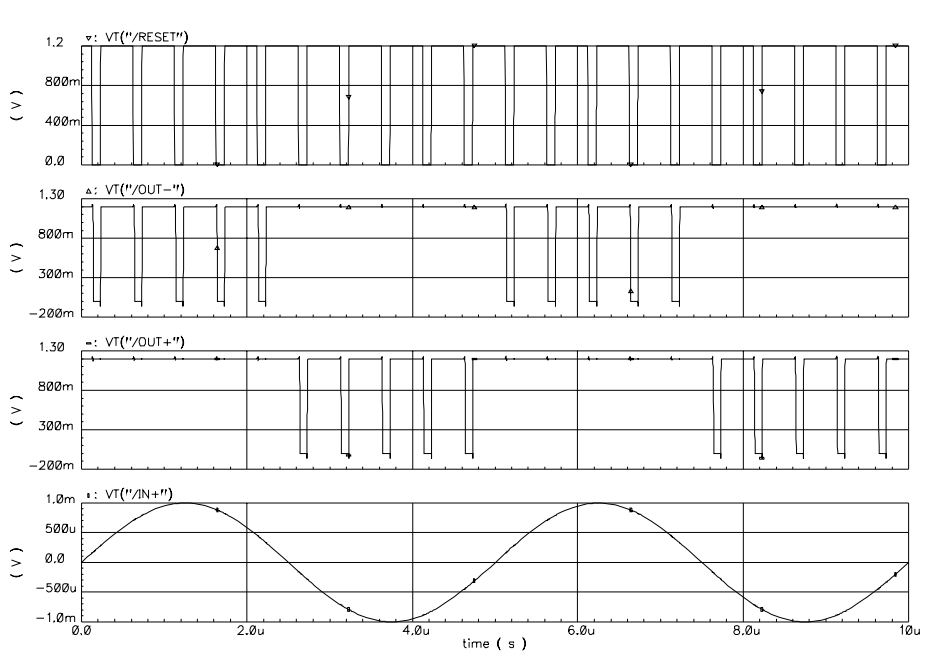


FIGURE 5.5: Comparator input and output signals

6. CONCLUSIONS AND FUTURE PLANS

6.1. Realization of Switched-Capacitor Circuits in Low-Voltage Supplies

The utilization of submicron CMOS technologies forces the use of lower power supply voltages. In traditional switched capacitor circuits, problems arise when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages, and hence they can't operate with supply voltages lower than 1.5 V.

So far, two solutions; clock boosting and switched-opamp methods have been proposed. In the clock boosting method, the gate-source voltage may exceed the permissible values, and the switched opamp suffers from a long settling time for the opamp, which causes a reduction in the circuit speed.

In this thesis, new circuit realizations for low-voltage switched-capacitor integrators were proposed.

The low-voltage integrator scheme using a PMOS transistor as the critical switch and driving the gate with a shifted clock instead of a boosted one (see Figure 2.1) has the advantage of circuit simplicity. In single-supply operation, the opamp needs about 150-200 mV as DC input common mode voltage to avoid saturation during the reset phase. This will increase the lower limit of power-supply voltage.

On the other hand, the use of the low-voltage integrator scheme using NMOS transistor as the critical switch (see Figure 2.8) will ease the restriction on the input common-mode voltage. However, more switches are required in this scheme, and the circuit will be more complex.

The master/slave method described in Section 2.3. is similar to the first method. However, there is no need to shift the clock signal level. The number of components in this scheme is doubled, but it is possible to operate the structure in a double-sampling mode.

The choice of one of these structures over another depends on the application and the performance requirements for that application. In general, in these schemes the power supply voltage must exceed $|V_{th}| + |V_{DSsat}|$. With a V_{thp} of the order of 0.7 V, we expect to be able to construct

a 1 V $\Delta\Sigma$ ADC or switched-capacitor filter. The advantage of these methods in comparison with the switched opamp approach is that in the reset mode the opamp operates with a feedback factor of one, avoid turning off and have a smaller output settling time.

Also in comparison with the clock boosting methods, the new schemes do not violate the allowable gate oxide voltage limits, which is a great concern in low-voltage processes.

Simulation results verified the theoretical concepts, and showed that the node voltages do not exceed junction-breakdown voltage. However, since by lowering the power-supply voltage the noise floor does not decrease, a reduced SNR value is expected in a real circuit implementation.

6.2. Future Plans

Based on the encouraging simulation results, we intend to lay out and fabricate in a 1.2 volt technology the two proposed second-order $\Delta\Sigma$ ADCs (Figures 4.5 and 4.7). Some simple SC filters, such as a biquad and a third-order filter will also be realized in both cascade and ladder forms.

In order to have better noise immunity, low-voltage common-mode rejection (CMRR) circuits are also needed if we need to implement these circuits in a fully-differential form.

It is reasonable to expect higher frequency and lower operating voltages for switched-capacitor circuits, using the novel integrator schemes once the CMOS technology offers lower threshold voltages.

BIBLIOGRAPHY

1. V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, W. Sansen, "A 900 mV 40μW switched-opamp delta-sigma modulator with 77 dB dynamic range," *IEEE International Solid State Circuits Conference*, pp. 68-69, 1998.

2. R. Castello and L. Tomasini, "1.5 V high-performance SC filters in BiCMOS technology," *IEEE J. of Solid State Circuits*, pp. 930-936, July 1991.

3. J. Crols and M. Steyaert, "Switched opamp: an approach to realize full CMOS SC circuits at very low supply voltages, "*IEEE J. of Solid State Circuits*, pp. 936-942, August 1994.

4. F. Maloberti, "Reduction of 1/f noise in SC ladder filters using correlated double sampling method," *Proc. IEEE International Conference on Communication Systems*, pp. 108-111, 1985.

5. G. Nicollini et al., "High-frequency fully differential filter using op amps without common-mode feedback," *IEEE J. of Solid State Circuits*, pp. 803-813, 1989.

6. Y. Nakagome et al., "Experimental 1.5 V 64 Mb DRAM," *IEEE J. of Solid State Circuits*, pp. 465-472, April 1991.

7. F. Maloberti, *personal communication*, July 21, 1997.

8. B. Boser, B. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-state circuits*, vol. SC-23, pp.1298-1308, Dec.1988.

9. P. Hurst, R. Levinson, "Delta-sigma A/Ds with reduced sensitivity To op-amp noise and gain," *IEEE International Symposium on Circuits and Systems*, pp. 254-257, 1989.

10. A. Baschirotto "A 40 MHz CMOS sample and hold operating at 1.2 V," *presented at European Solid-State Circuits Conference*, 1998.

11. Jieh-Tsong Wu, Yueh-Haung Chang, Kuen-Long Chang, "1.2 V CMOS switched-capacitor circuits," *IEEE International Solid State Circuits Conference*, pp. 388-389, 1996.

12. A. Baschirotto, F. Montecchi, R Castello, "A 15 MHz 20 mW BICMOS switched-capacitor biquad operating with 150 Ms/s sampling frequency," *IEEE J. of Solid State Circuits*, vol. 30 pp. 1357-1365, 1995.

13. J. Candy, G. Temes, "Oversampling methods for A/D and D/A conversion," *in Oversampling delta-sigma data converters*, IEEE Press, 1992.

14. S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters*, IEEE Press, 1992.

15. F. You, S. Embabi, J.F. Duque-Carrillo, E. Sanchez-Sinencio, "An improved tail current source for low voltage applications," *IEEE J. of Solid State Circuits*, vol. 32, pp. 1173-1180, August 1997.

16. E. Sackinger, W. Guggenbuhl, “A high-swing, high-impedance MOS cascode circuit”, *IEEE J. Solid-State Circuits*, vol. 25 pp. 289-298, Jan. 1990.

17. P. J. Crawley, G. W. Roberts, “High-swing MOS current mirror with arbitrarily high output resistance,” *Electronic Letters*, vol. 28, no. 4, pp. 361-363, February 1992.

18. T. Serrano, B. Linares-Barranco, “The active-input regulated-cascode current mirror,” *IEEE Transactions on Circuits Systems.*, vol. 41, pp. 464-467, June 1994.

19. D. Johns, K. Martin, “Analog Integrated Circuit Design,” Wiley, pp. 261-263, June 1997.

20. J. Steensgaard, *Group meeting*, March 16, 1998.

21. J. Steensgaard, *Group meeting*, April 13, 1998.