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ACCURATELY TUNABLE LOW-VOLTAGE CONTINUOUS-TIME FILTERS

1. INTRODUCTION

Almost all communication systems and measuring equipment of modern day contain various types of electrical filters that are realized in appropriate technologies. In general, a filter is a two port network designed to process the magnitude and/or phase of an input signal to generate a desired output signal. Today, most filter implementations are realized in monolithic integrated circuits as some form of an active filter (e.g. RC, G_m-C, MOSFET-C etc.). The integrability and size reduction of these filters have made them a very economical and electrically desirable solution. As the levels of integration are increasing, many system designs are realized on a single chip (System on Chip (SoC)) and integrated filters have become a “standard cell” in present day. One of the most critical issues in practical filter applications is the RC time constant variation (inversely proportional to the –3dB frequency) due to variations in process, temperature, etc.

The corner frequency of a switched capacitor filter is dependent on the product of the clock frequency and the ratio of capacitors. This makes it very accurate whereas in continuous time filters, the corner frequency is set by the RC time constant and it can vary widely over process, temperature, etc. [25]. Although switched capacitor filters provide accurate corner frequencies, due to their inherent

sampled nature, input anti-aliasing and output smoothing filters are required [8]. Further, in switched capacitor filters, internally generated opamp noise and power supply noise at high frequencies are aliased into the base-band due to sampling by each switch.

Switched capacitor filters suffer from various non-ideal effects like clock feed-through, charge injection, finite opamp gain and bandwidth but continuous time filters also face similar kind of problems with regard to linearity. Overall, each type of filter has its own advantages and disadvantages. The work herein focuses on overcoming the RC time constant variation by investigating a tunable continuous time filter. A new method is proposed which will be able to tune the filter very accurately considering the mismatches between the tuning part of the circuit and the filter in the process of tuning.

1.1 Types of Filter Implementations

Filter design does encounter a few challenges to cope with the continuously improving SoC designs. The filter's corner frequency is inversely proportional to the RC time constant. One of the most important issues for filter design in practical applications is the RC time constant variation due to process, temperature, etc. As R and C are not the same type of electrical components, the variations in process, temperature, etc. of R and C do not track each other. This, in the worst case, can result up to a ± 50% variation in the corner frequency of the filter (f_c). For some applications like high speed or highly selective filtering, Q tuning should be done to

maintain the exact shape of the transfer function [16]. However, this work does not deal with Q tuning. To compensate for this problem in continuous time filters, RC – time constant can be varied electronically by using some kind of automatic tuning.

1.2 Existing Tuning Techniques

Many tuning techniques have been proposed to compensate for the corner frequency variation and maintain the shape of the transfer function [4], [5], [6], [7]. Of those, the master-slave tuning technique is the most popular one. In this kind of scheme, the master and the slave track process and temperature variations well, but the accuracy of the tuning is limited by the mismatch between the master and the slave.

1.3 Thesis Organization

The organization of this thesis is done as follows. Chapter 2 discusses various tuning techniques and underlines the basic mismatch problem in master slave tuning. It also deals with the linearity issue in tunable continuous-time filters. Truly low-voltage continuous time filter design issues are presented. Chapter 3 deals with the proposed technique for the minimization of the master and slave mismatch, thereby tuning the filter very accurately. Circuit design of the complete system is presented in Chapter 4. Chapter 5 presents experimental results of the fabricated chip. Finally, Chapter 6 deals with the limitations of the proposed system and a few possible solutions.

2. TUNING, LINEARITY AND LOW-VOLTAGE ISSUES IN CONTINUOUS -TIME FILTERS

The key issues in the design of modern day continuous time filter design are time constant variation due to process, temperature variations and limited linearity of the tunable elements. This chapter discusses the above mentioned problems in detail. It also deals with the issues involved in low-voltage continuous-time filter design. The initial part deals with tuning in continuous time filters and latter sections deal with linearity and low-voltage issues.

2.1 Tuning in Continuous-time Filters

If accurate tuning of continuous time filters is to be guaranteed, then precise absolute element values must be realized and maintained during the circuit operation [16]. But these are not normally available because of the fabrication tolerances, temperature drifts, etc. To overcome this problem, a generally adopted solution is to design an on-chip automatic tuning circuitry. To make this on-chip automatic tuning possible, the RC time constants must be such that they are tunable. There are several ways to implement the on-chip automatic tuning. Some of these include voltage controlled resistors, trimmed resistors, varactors, etc. as tunable elements. For example, for the first order filter shown in Figure 2.1, the corner frequency is inversely proportional to the RC time constant as shown. To allow for tuning to compensate for the time constant variation, the resistor can be replaced by a

MOSFET operating in triode region. The equivalent resistance of the MOSFET can be varied by changing the gate voltage V_G

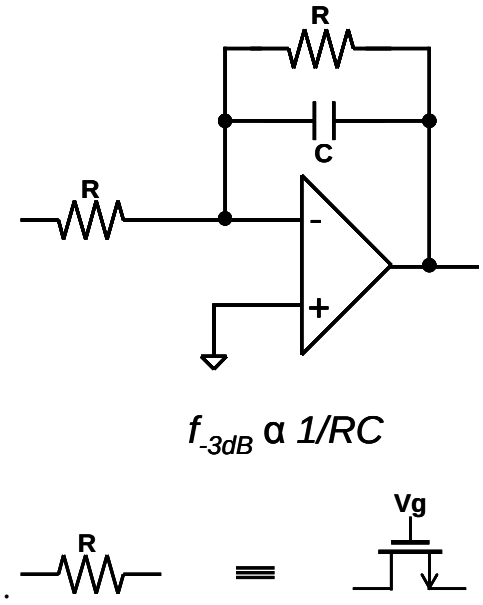


Figure 2.1 First order filter: R replaced by MOSFET in triode region

Automatic tuning methods can be broadly separated into two categories - direct tuning and indirect tuning. These methods will be described in detail in this section.

2.1.1 Direct and Indirect Tuning

Direct tuning is performed by observing the filter's output and correcting for the error in the -3dB frequency by adjusting the RC time constant automatically. The block diagram for this method is shown in Figure 2.2. The filter can be very accurately tuned by using this method but the main drawback is that it requires

interruption of the filter operation when it is being tuned. Essentially this is “foreground” in nature. Unless a redundant block is used to mask the circuit to appear as if the operation is uninterrupted, this method cannot provide “background” adjustment [3].

Indirect tuning is advantageous over direct tuning because of its inherent setup for background adjustment. In this method, the filter is always operational even when it is being tuned unlike in the case of direct tuning [8]. Master-slave tuning technique is one of the preferred indirect tuning methods. In master-slave tuning, two blocks - the master and the slave (the main filter block) are present as shown in Figure 2.3. The master block can be an accurate model of the slave. The output of the master block is observed and is used to correct for the errors (RC time constant variation) in the master and the slave. This method is very effective due to its background nature. The master must be accurately modeled such that it will have all the performance criteria of the main filter. The main drawback of master-slave tuning resides in the matching relationship of the master and the slave blocks, which relies heavily on tight component matching between the two circuit blocks. Any mismatch between the master and the slave will directly affect the accuracy of the desired -3dB corner frequency of the filter (the slave).

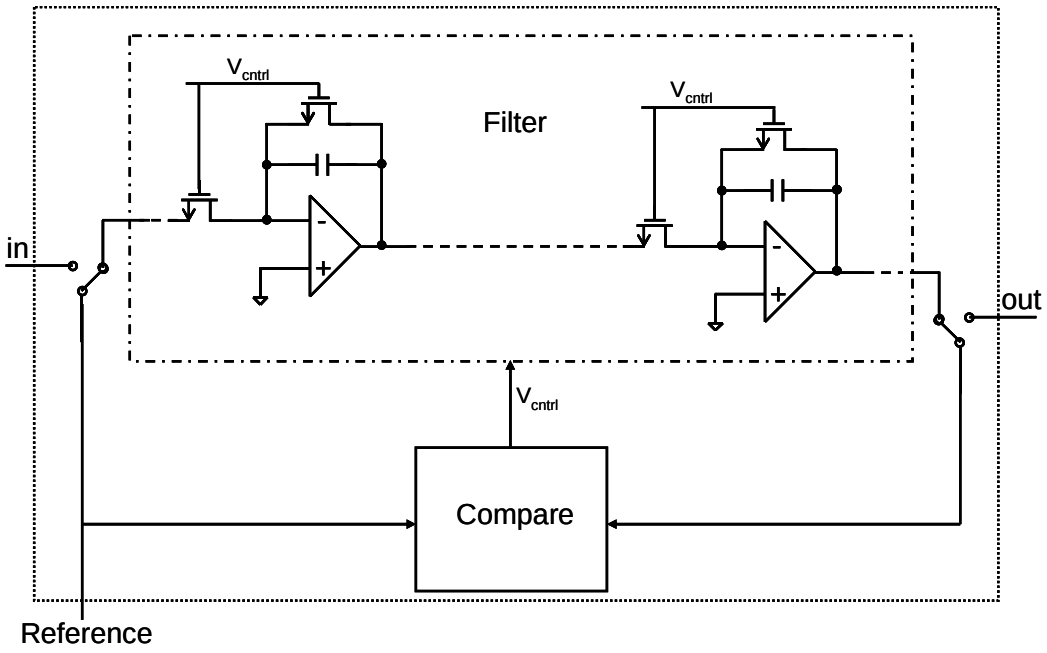


Figure 2.2 Direct tuning: Switches showing interruption of filter operation during tuning.

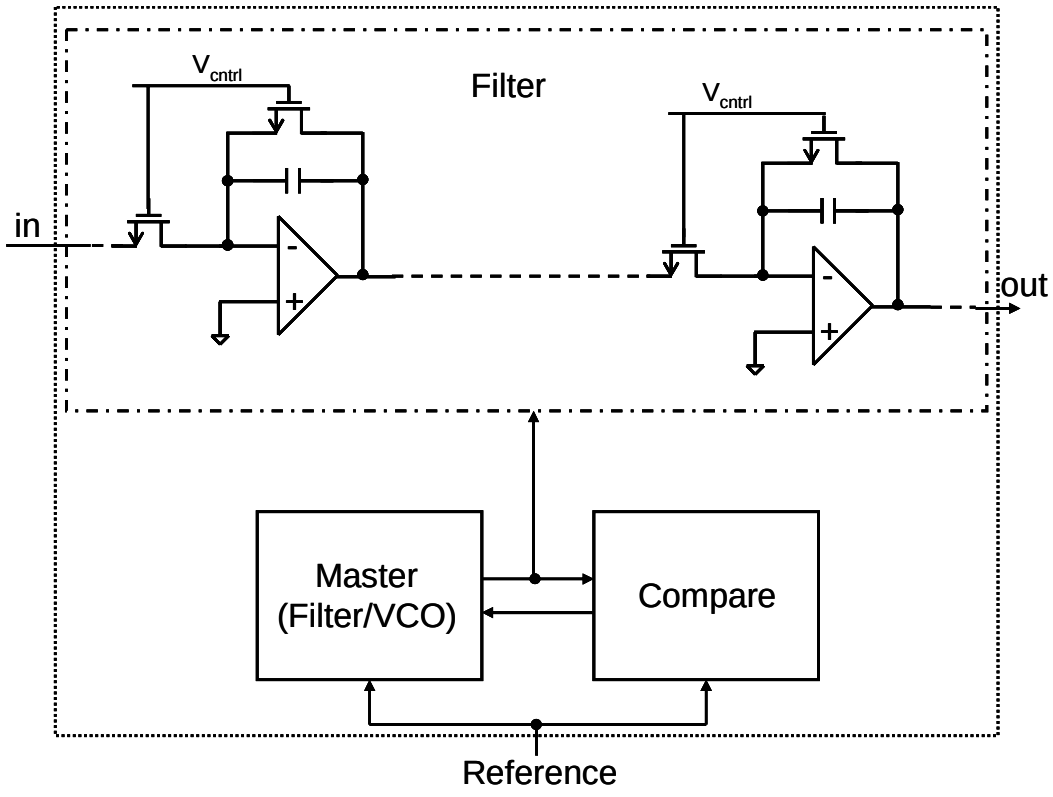


Figure 2.3 Indirect tuning illustration

2.1.2 Example Implementations of Master-slave Tuning

Transconductor-based tuning

An example implementation of the indirect tuning is shown in Figure 2.4 [22]. Here an extra transconductor/resistor is built which models the transconductance(G_m) in the filter. The resulting tuning voltage controls the filter transconductors.

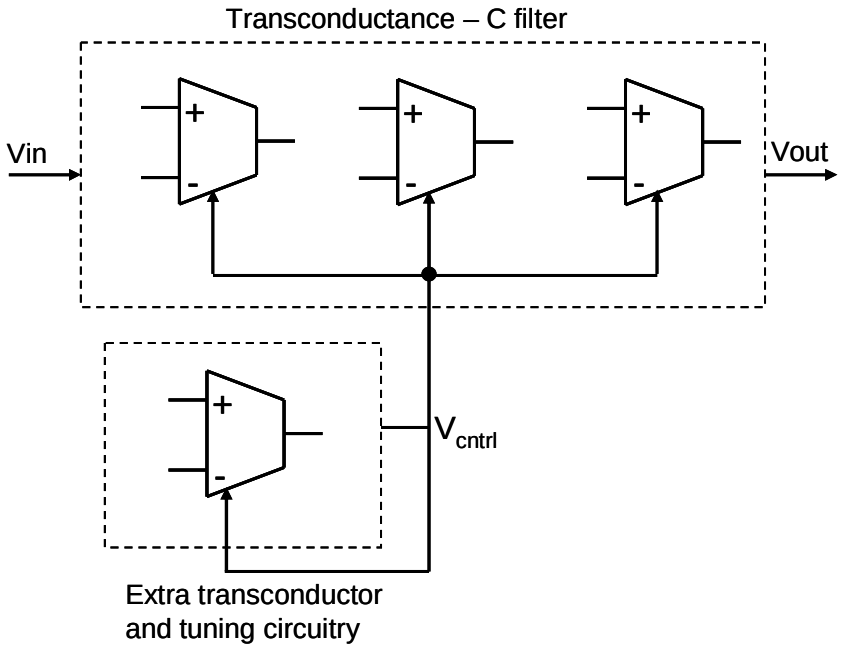


Figure 2.4 Indirect tuning example implementation

Integrated capacitance typically accounts for 10% variation in its value. Thus, in applications where a 10% variation can be tolerated, it is sufficient to set the G_m

value with the use of an external resistor. To set the G_m value equal to the inverse of a resistance, a variety of feedback circuits can be used. Two such implementations are shown in Figure 2.5. In the two implementations shown, it is assumed that the G_m value increases with control voltage/current. In Figure 2.5(a), if the G_m is small, then the current through R_{ext} is larger than the current output of the transconductor.

The difference between these two currents is integrated and the control voltage is increased as a result until the two currents become equal ($G_m=1/R_{ext}$). The circuit in Figure 2.5(b) shows two voltage-current converters. This circuit operates in a manner very similar to the one in Figure 2.5(a). If the G_m is too small , the control voltage at the top of C is less than V_{ref} and the V/I converter will increase I_{cntrl} which will make $G_m=1/R_{ext}$.

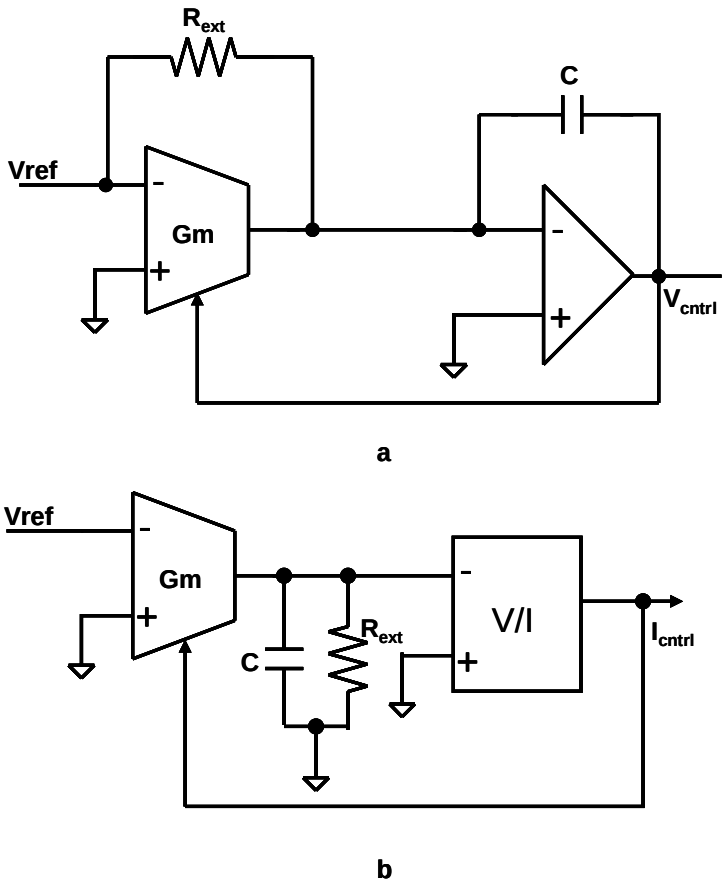


Figure 2.5 Constant transconductance tuning (a) Voltage controlled (b) Current controlled. In both circuits, it is assumed that the transconductance increases with the control signal

Time Constant-based Tuning

A precise tuning of the RC time constant can be achieved if an accurate clock is available [8], [22]. The clock can be used in the implementation shown in Figure 2.6 where a switched capacitor circuit is used [12]. This circuit is very similar to the one that is discussed in the previous section but the external resistor is replaced by an equivalent switched capacitor resistor ($R_{eq}=1/f_{clk}C_1$, f_{clk} being the frequency of φ_1 and φ_2). The R value is set to $1/f_{clk}C_1$. Thus the RC time constant is equal to $f_{clk}C_1/C_A$

where C_A is the capacitance used in the filter. An additional low pass filter, $R_{LP}C_{LP}$ can be seen which is used to remove the high frequency ripple because a switched capacitor circuit is used.

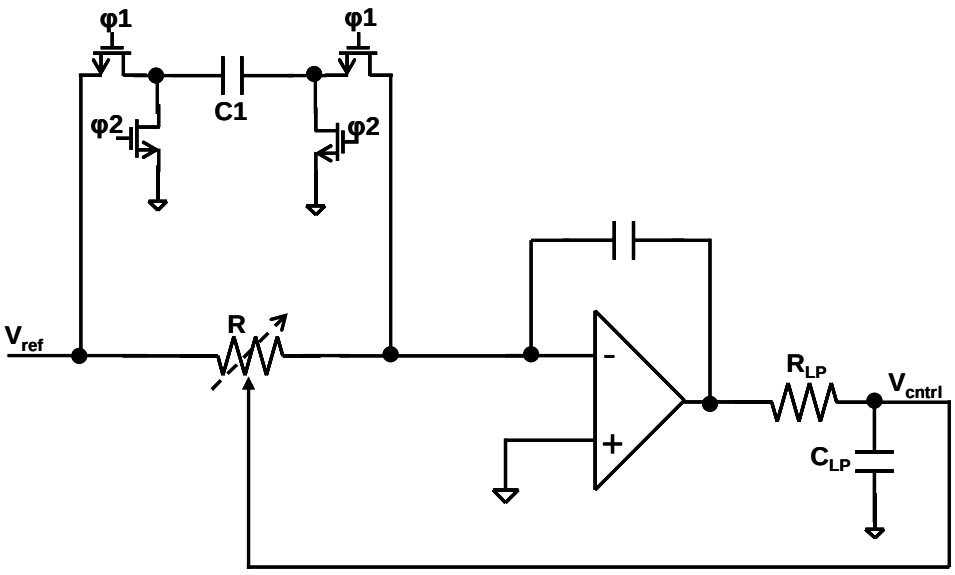


Figure 2.6 A frequency tuning circuit where 'R' is set by the switched capacitor circuit.

PLL-based Tuning

Another approach to use the accurate reference clock to tune the filter is by using a phase locked loop (PLL) as shown in Figure 2.7 [7]. The voltage controlled oscillator (VCO) in the PLL can be implemented by placing two continuous time integrators in a loop. The negative feedback ensures that the VCO output is locked to

an external reference clock. The control voltage obtained can be used to tune the filter. In this kind of tuning, it should be noted that the choice of the external clock reference is a trade-off because it affects both the tuning accuracy and the tuning signal leakage into the main filter. If the external clock reference is chosen to be at one of the zeros of the filter, then the tuning signal leakage can be eliminated. But, for good matching between the tuning circuit and the filter, it is best to choose a reference frequency that is equal to the filter's upper pass-band edge, but the reference signal leakage might be very severe in this case. If the reference frequency moves away from the filter's upper pass-band edge, the matching gets poorer but the tuning signal leakage is minimized [5], [13], [22]. Another problem with this approach is that if the VCO has low power supply rejection, any supply noise will inject jitter into the VCO that results in a noisy control voltage V_{cntrl}.

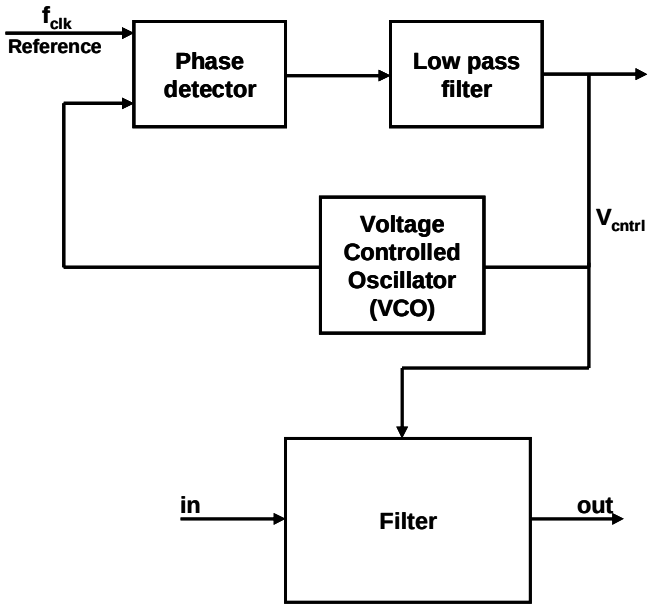


Figure 2.7 Frequency tuning using a PLL. The VCO is realized by using integrators that are tuned to adjust the VCO frequency.

A similar approach to the PLL based tuning is shown in Figure 2.8 [5]. Here, a tracking filter locks onto a reference frequency. This approach is reported to be less sensitive to supply noise as opposed to the previously discussed one. The output control voltage is used to adjust the G_m of the transconductors used in the main filter, assuming the transconductors in the main filter match those in the filter used for tuning.

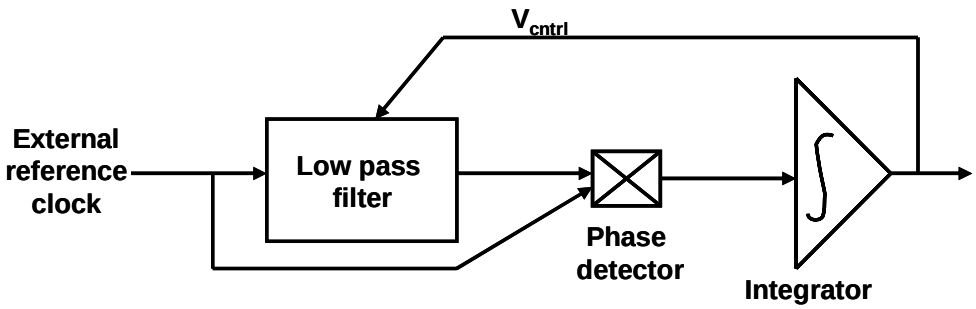


Figure 2.8 Tracking filter to derive the control signal for tuning the main filter.

2.1.3 Q Tuning

In applications which need highly selective filtering, non-ideal effects of the integrators and parasitic components force the need to tune the Q-factors of the poles of the filter. This needs an additional Q-control circuitry which increases the possibility of reference tuning signal leakage into the main filter. One of the approaches for Q- tuning is described here (shown in Figure 2.9 [22]). The phase of the filter's integrators is tuned such that they all have a 90-degree phase lag near the filter's pass-band. The integrator's phase response can be adjusted automatically by using a tunable resistor in series with the integrating capacitor. The control voltage for this tunable resistor is generated by the Q-tuning loop.

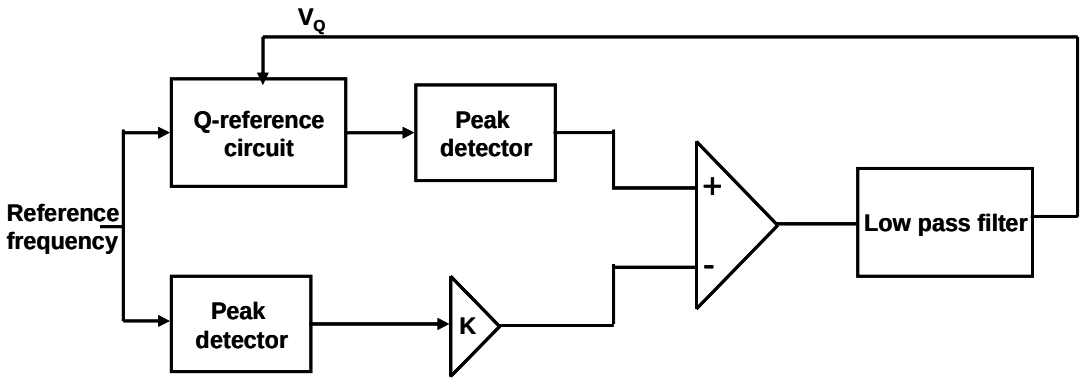


Figure 2.9 Q-tuning loop. V_Q is the Q-control voltage.

Until now, different implementations of master-slave tuning have been discussed. All of these suffer from the problem of master and slave mismatch. For example, in Figure 2.6, the matching between the tuning resistor and the filter resistor to which the same control voltage feeds is not perfect. The next chapter deals with possible solutions to minimize this mismatch.

2.2 Linearity of Continuous-time Filters

Highly linear continuous time filters are a definite requirement in modern day applications. The most popular among the electronically tunable filters are the MOSFET-C filters because of their simplicity. The gate voltage of the MOSFETs can be varied automatically to tune the filter. But the overall linearity of the filter is limited by the linearity of the MOSFET itself (typically 40-60dB), assuming an ideal opamp behavior.

2.2.1 Linearity improvement in MOSFET-C Filters

An n-channel MOSFET is shown in Figure 2.10. Its gate is connected to a dc control voltage obtained from an automatic tuning circuit. The substrate is connected to a fixed bias. The terminal voltages at the source (v_1)and the drain(v_2) remain V_{TH} below V_g to allow for the operation in triode region.

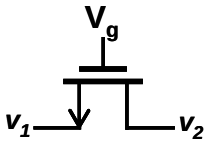


Figure 2.10 MOSFET in triode region as resistor.

The transconductance G_M is given by $G_M = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{TH})$

Triode region current equation: $I_D = \frac{W}{L}\mu_n C_{ox}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^{\ 2}}{2}]$

As the MOSFET is present at the input of the filter (Figure 2.11), the variation of drain-source voltage of the MOSFET introduces significant nonlinearity in the main filter. This V_{DS} variation can be minimized by having $2(V_{GS}-V_{TH}) >> V_{DS}$ as per the equation below.

$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{TH})V_{DS}$$

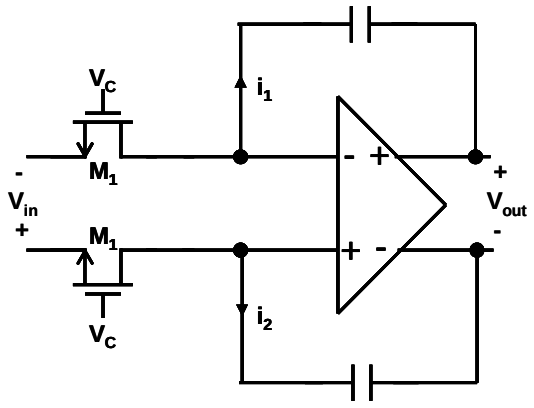


Figure 2.11 Fully differential integrator: MOSFETs used as resistors

For the Figure shown in 2.11,

$$i_{in} = i_1 - i_2 = [K(V_c - V_{TH})(\frac{V_{in}}{2}) - \frac{K}{2}(\frac{V_{in}}{2})^2] - [K(V_c - V_{TH})(\frac{-V_{in}}{2}) - \frac{K}{2}(\frac{-V_{in}}{2})^2] = K(V_{in} - V_{TH})V_{in}$$

$$V_{TH} = V_{TH0} + \gamma\sqrt{2\varphi_F + V_{SB}} - \gamma\sqrt{2\varphi_F}$$

Finite V_{DS} (= $\pm V_{in}/2$) causes threshold voltage variation (V_{SB+} and V_{SB-}), which introduces significant non-linearity. As V_{TH} is nonlinearly dependent on the input, if the input varies, the equivalent resistance of the MOSFET varies in a nonlinear fashion. By using fully differential structures, some the above mentioned nonlinearities can be reduced. Figure 2.12 shows a symmetric, cross-coupled structure that will cancel for V_{TH} variations with the input thus making the filter immune to the nonlinearity introduced by V_{TH} [11].

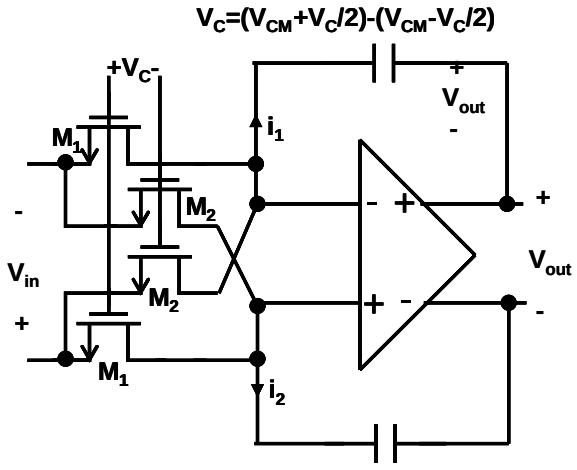


Figure 2.12 Fully differential integrator. Symmetrical structure to cancel V_{TH} effect [11]

For the Figure shown in 2.12,

$$i_{in} = i_1 - i_2 = [\{V_{CM} + \frac{V_C}{2} - V_{TH}^{+}\}(\frac{V_{in}}{2}) - \frac{K}{2}(\frac{V_{in}}{2})^2] + [\{V_{CM} + \frac{V_C}{2} - V_{TH}^{-}\}(\frac{-V_{in}}{2}) - \frac{K}{2}(\frac{V_{in}}{2})^2]$$
$$-[\{V_{CM} + \frac{V_C}{2} - V_{TH}^{-}\}(\frac{-V_{in}}{2}) - \frac{K}{2}(\frac{-V_{in}}{2})^2] - [\{V_{CM} + \frac{V_C}{2} - V_{TH}^{+}\}(\frac{V_{in}}{2}) - \frac{K}{2}(\frac{V_{in}}{2})^2]$$
$$= K(\frac{V_C}{2} + \frac{V_C}{2} + \frac{V_C}{2} + \frac{V_C}{2})(\frac{V_{in}}{2}) = KV_C V_{in}$$

Thus the threshold voltage variation due to finite V_{DS} (= $\pm V_{in}/2$) gets cancelled.

2.2.2 R-MOSFET-C Linearization Technique

Linearization by scaling signal swing

Another more fundamental way to reduce nonlinearity introduced by V_{DS} is proposed in [1]. Here the MOSFET is split into a part linear resistor and a MOSFET. Much of the input signal swing is dropped across the linear resistor. Thus the MOSFET can experience relatively lesser swing (Figure 2.13). This results in lesser V_{DS} variation, thus improving the linearity. This can be coupled with the idea discussed in [11] to reduce the V_{TH} variation with the input. But as discussed in detail in [3], if the symmetric structure proposed in [11] is used, it will result in a significant increase in the equivalent noise of the filter. If the equivalent resistance seen between the two inputs of the opamp by using the structure in Figure 2.12 is R_{eq}, the equivalent resistance with the modified structure shown in Figure 2.15 is $4R_{eq}$, thus reducing the output noise of the filter.

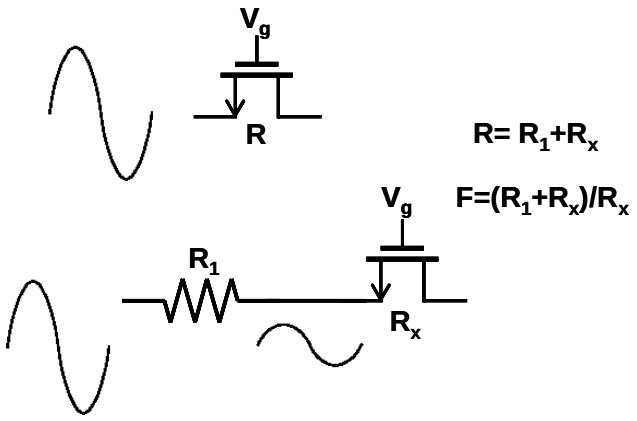


Figure 2.13 MOSFET to R-MOSFET conversion.. Reduced swing across the MOSFET

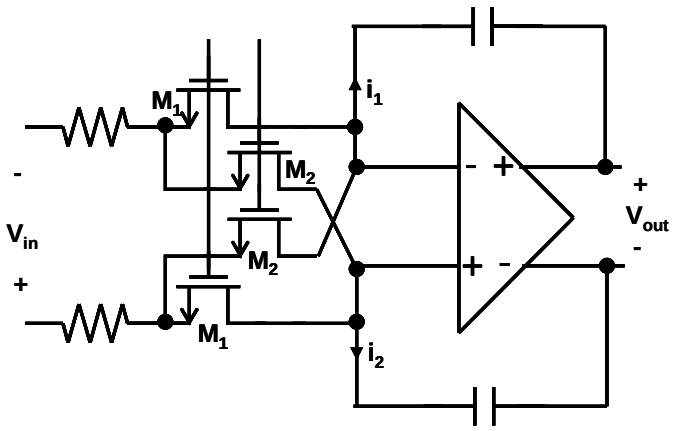


Figure 2.14 Using R-MOSFET structure along with V_{TH} cancellation circuit for better linearity.

Linearization by having Non-linear Elements in Feedback Loop

The discussions so far have shown that the linearity can be improved by scaling the input signal swing. In an active filter configuration, the integrator has a second input which forms a feedback loop. Thus the MOSFET part of the resistor can be shared between the input resistor and the feedback resistor (shown in Figure 2.15). This results in having the MOSFET, the key nonlinear element in a feedback loop. This kind of arrangement is known as R-MOSFET-C structure [1]. The linearity of a nonlinear element in a feedback loop is improved by the loop-gain, thus suppressing the nonlinearity by a significant amount [23]. Therefore, by using the structure given in [1], the linearity of the filter is improved in two ways, firstly it is improved because the MOSFET experiences a relatively lesser signal swing and secondly, the distortion is improved by a greater factor because the nonlinear elements are in a feedback loop. But the improvement of linearity by the feedback loop reduces as the filter's upper pass-band edge is approached because the net loop-gain reduces as filter's bandwidth is approached.

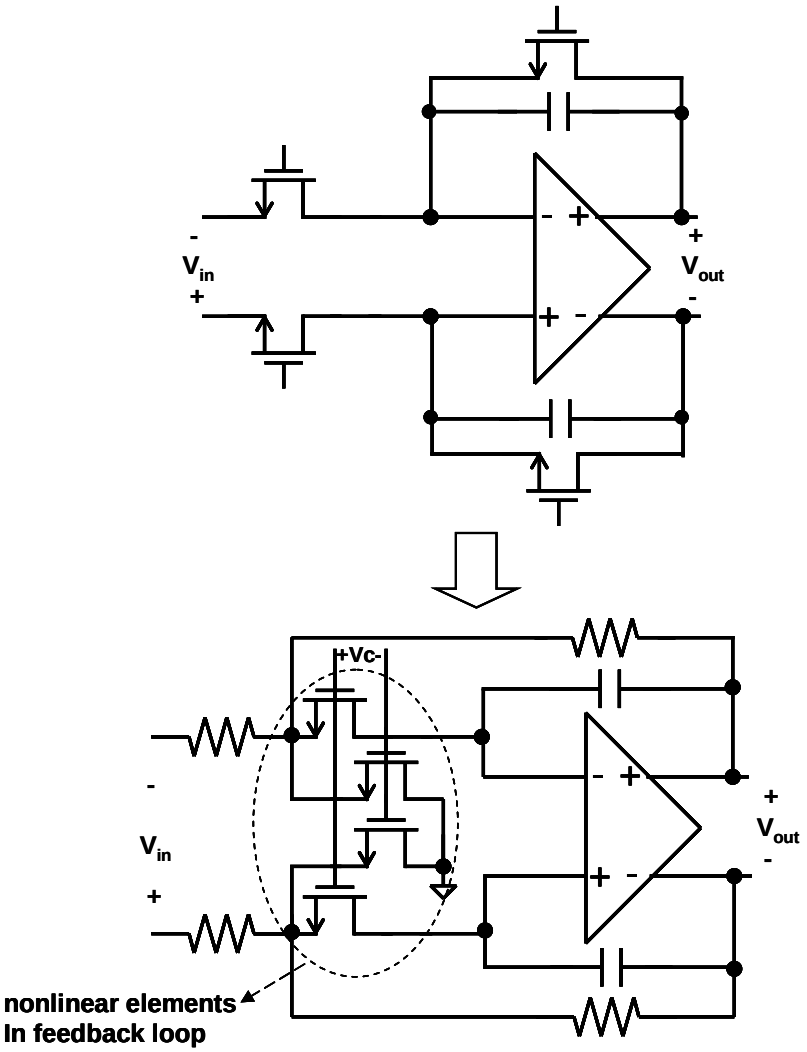


Figure 2.15 RC to R-MOSFET-C conversion

When converting from RC to R-MOSFET-C, the loading effect must be considered as discussed below. R_{11}, R_{22} should be converted to R-MOSFET as shown where R_X is the equivalent resistance of the MOSFET. Figure 2.16 shows the conversion in detail.

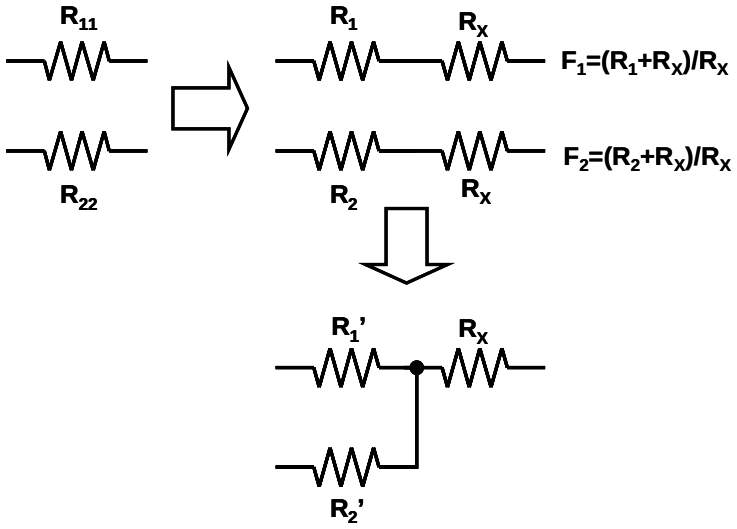


Figure 2.16 Figure showing the exact conversion from R to R-MOSFET.

Now to share R_X between R_1 and R_2, the original resistor values must be modified because of loading effect. The new R_1' and R_2' can be calculated by solving the equations given below.

$$F_1 = \frac{R_1^{'} + (R_2^{'} \,||\, R_X)}{(R_2^{'} \,||\, R_X)}$$

$$F_2 = \frac{R_2^{'} + (R_1^{'} \,||\, R_X)}{(R_1^{'} \,||\, R_X)}$$

2.3 Low-voltage Continuous-time Filter Design

2.3.1 Device Reliability

Design of low voltage continuous time filters is definitely a formidable challenge with the ever shrinking supply voltages. Advances in CMOS technology are driving the supply voltages of integrated circuits lower. The forecast of operating voltages for CMOS technology is shown in Figure 2.17 [19]. One of key issues as a result of reduction in supply voltages is device reliability especially in short channel devices.

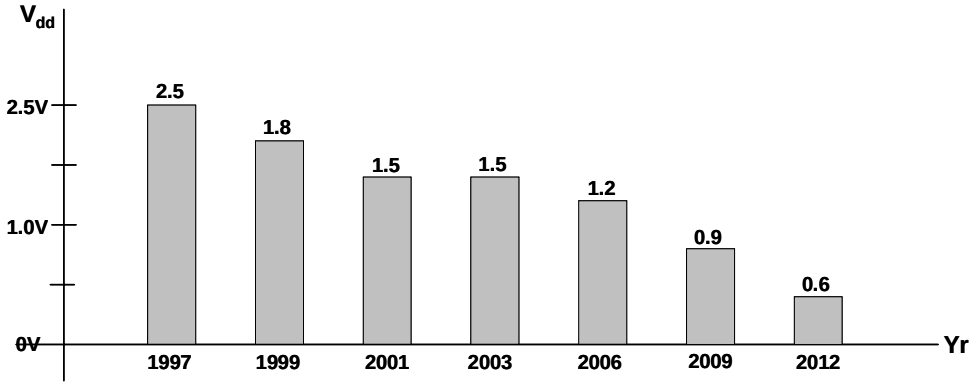


Figure 2.17 Semiconductor Industry Association 1997 forecast of CMOS voltage supply.

For a design to be very reliable, all the terminal-terminal voltages of the MOSFETs used in the design should always be limited by V_{DD} at any point of time. For example in present day technologies with reducing gate oxide thicknesses, excess

V_{GS} results in gate oxide stress and excess V_{DS} might cause hot electron effects thus affecting the device reliability in the long term.

2.3.2. Tuning Range Limitation

A MOSFET-C filter can be tuned by varying its gate voltage V_G (i.e., by varying the equivalent resistance). For the MOSFET to be operational, $V_{GSMIN} \geq V_{TH}$ and to prevent gate oxide breakdown, $V_{GSMAX} \leq V_{DD}$. So V_G can only be varied between V_{TH} and V_{DD} which implies that the tuning range is very small (Figure 2.18). Various techniques are proposed to overcome this tuning problem in chapter 6, but in this work, a high V_{DD} is used for the tuning part of the circuit such that enough tuning range is obtained. If $V_{GS} > V_{DD}$, then the oxide is subject to a lot of stress which eventually leads to oxide breakdown. But if thick oxide devices are used for the tunable part of the circuit, this problem can be ameliorated (Figure 2.19).

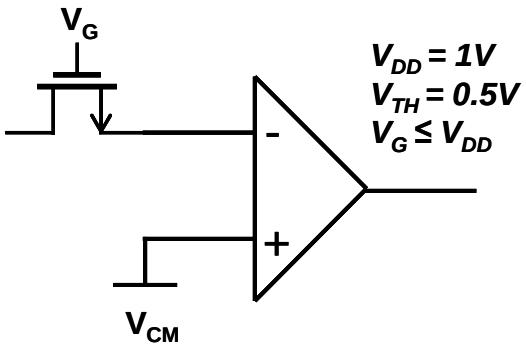


Figure 2.18 Part of the integrator showing the limitation of the gate voltage in low-voltage filters.

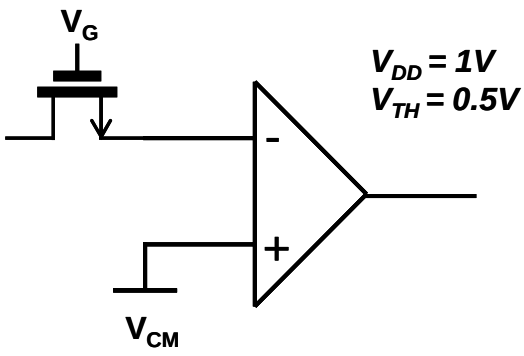


Figure 2.19 Use of thick oxide devices to allow for greater V_{GS}. Part of the integrator showing thick oxide MOSFET whose gate voltage can exceed V_{DD} to provide the sufficient tuning range.

Another technique that can be used to increase the tuning range is bootstrapping. The control voltage can be generated to be a sum common-mode voltage and control voltage. The common-mode voltage will turn on the resistor and the control voltage is used to tune the resistor. But designing a bootstrapped circuit in a truly low voltage sense itself is a difficult task. Progress is being made in this area [19], [20]. More details about low voltage filters are presented in chapter 6. The system described in this thesis uses thick oxide devices for the tunable elements and higher V_{DD} for the tuning circuit.

The linearity is improved by using R-MOSFET-C structure. High V_{DD} used to overcome the tuning range problems in the low-voltage filter implementation. Thick oxide devices are used as tunable elements (MOSFETs) to withstand the oxide stress.

The next chapter discusses the proposed scheme to obtain accurate tuning in continuous time filters by correcting for the master-slave mismatch problem.

3. MISMATCH MINIMIZATION SCHEME

As discussed in the previous chapter, the master slave tuning works very well across process and temperature corners but the accuracy is limited by the mismatch between the master and the slave blocks. In this chapter, the mismatch minimization scheme is discussed in detail.

The proposed work is to take care of the mismatch problem in master-slave tuning by trying to minimize the mismatch in the master and the slave, and thereby tuning the filter very accurately. Also this can be done on power-up, assuming that there is enough time available during the power-up mode of a chip and it can be used to cancel the mismatch between the master and the slave. Doing this is very useful because once the filter starts normal operation after power-up, the mismatch is minimized and the background nature of the master-slave tuning corrects for the process, temperature, etc. variations. Effectively this method uses both direct and indirect tuning methods. During the mismatch minimization on power up, both direct tuning and indirect tuning are in place. However, once the mismatch is minimized, only the indirect tuning is in control and the filter is tuned very accurately. The mismatch minimization is done by effectively introducing some calculated mismatch in the master itself. AC response of a simple biquad indicating 10% mismatch in the master and the slave can be seen in Figure 3.1.

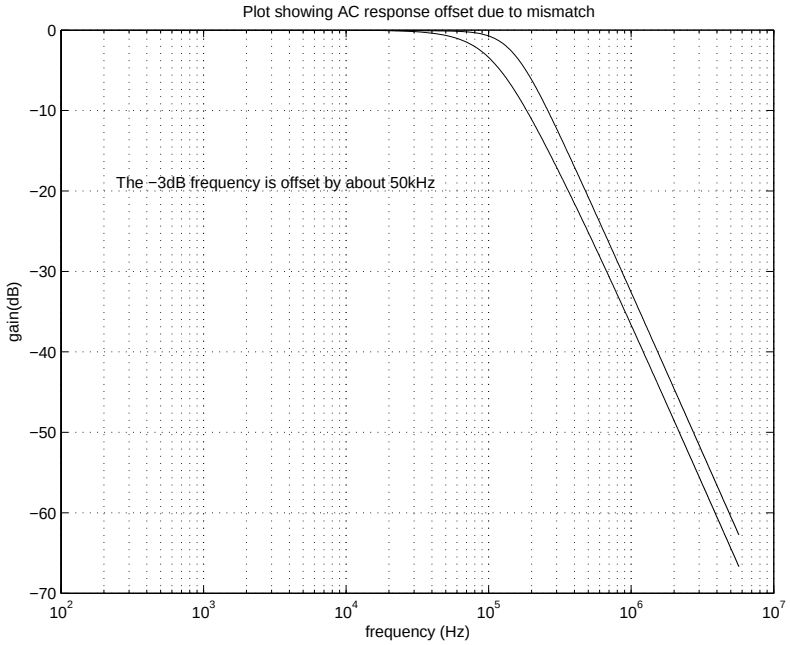


Figure 3.1 Simulation showing the AC response offset (cutoff frequencies are offset) due to mismatch.

The system level block diagram of the proposed scheme can be seen in Figure 3.2. As shown in the Figure, on power up, a sine wave of desired frequency (typically the -3dB frequency of the filter) is generated using the clock. This generated sine wave is passed through the filter (slave). The output of the filter is used to detect and correct for the mismatch between the master and the slave. The correction can be performed through the master circuit as discussed below.

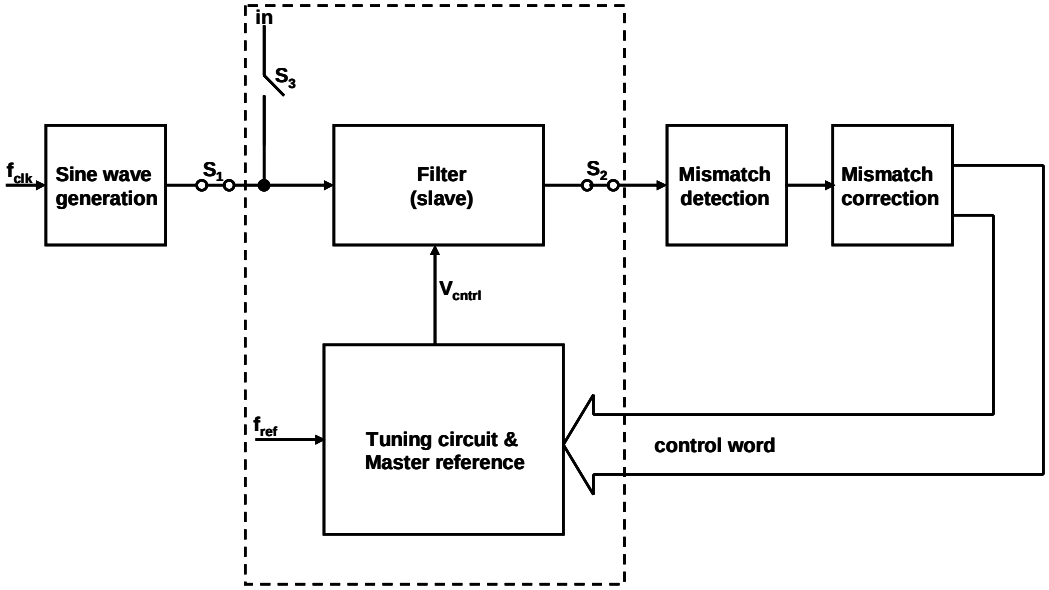


Figure 3.2 Block diagram of mismatch minimization system

S_1, S_2 are ON at power up and S_3 is ON after the mismatch minimization has been performed.

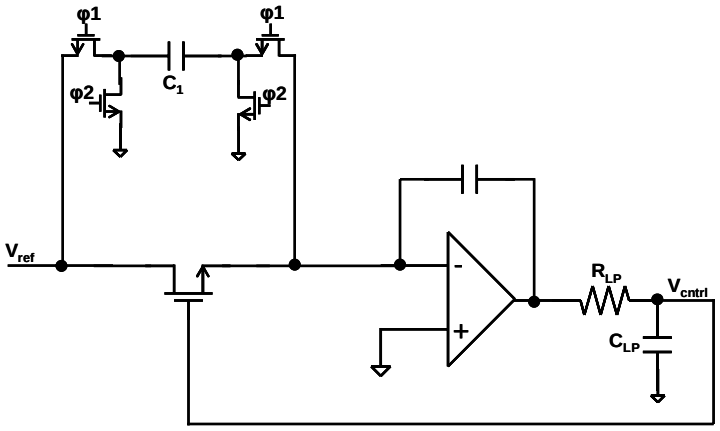


Figure 3.3 Switched capacitor based tuning

The mismatch detection and correction block diagram is shown in Figure 3.4.

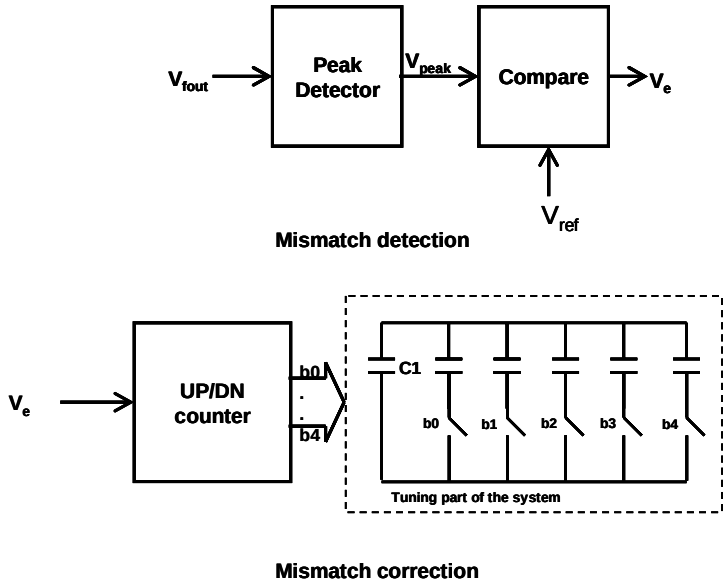


Figure 3.4 Mismatch detection and correction block diagram.

The master can be a switched capacitor resistor as shown in Figure 3.3 where the capacitor C_1 and f_{clk} (φ_1 and φ_2 are set by f_{clk}) sets the reference resistance value. Capacitor C_1 can be replaced by a capacitor bank as shown in Figure 3.4. The slave is the main filter itself. The filter output (-3dB value) peak is determined and compared with the ideal -3dB peak (i.e. the peak when the filter is tuned very accurately when no mismatches are present). The comparator output is fed to a UP/DN counter. The output of the counter will generate a control word which modifies the master reference (modifies the effective capacitance in the capacitor bank). Here the counter

output can be used to turn ON/OFF the switches of the capacitor bank (shown in Figure 3.4) in the tuning circuit such that the master is modified to account for the master-slave mismatch. The result is that the new RC time constant is relatively more accurate than the one where there is no mismatch correction in place. The counter will count UP/DOWN based on whether the mismatch is positive or negative. The comparator output determines whether the mismatch is positive or negative. This system is designed to accommodate for ± 10% mismatch correction. Once the mismatch minimization is done, the counter is turned off and the counter output is frozen so that the effective capacitance of the reference switch capacitor is changed to accommodate for the mismatch between the master and the slave. The filter can operate in normal mode once the mismatch minimization scheme is turned off (as shown in Figure 3.2, switches S_1 and S_2 are turned off in normal operation mode and S_3 is turned ON).

4. IMPLEMENTATION OF THE SYSTEM

The implementation of the system discussed in Chapter 3 is dealt with in this chapter. The design of the basic filter, tuning circuit and the mismatch minimization scheme is presented. To verify the concept of mismatch minimization on power up to tune the filter accurately, a simple low-pass Butterworth biquad is implemented. The corner frequency (-3dB frequency) of the filter is chosen to be 200 kHz and the power supply for the filter part is 1V. The tuning circuit uses a higher supply (1.8V) as discussed in Chapter 2.

4.1 Filter and Tuning Circuit Design

As mentioned in chapter 2, the master can be a reference resistor, a reference frequency which defines a time constant, etc. The master used in this work is a reference frequency. In this section, design of continuous-time filter and tuning circuit has been discussed.

4.1.1 Filter Design

Active filter design can be done through various approaches. Standard LC ladder based, biquad based and Sallen-Key based design are a few examples to quote. Each of the approaches mentioned above have their advantages and disadvantages. For example, if LC ladder approach is used, the filter will have very less pass band sensitivity due to component inaccuracies because in a LC ladder type of

implementation, the poles and zeroes tend to move together if there is any component variation. If a biquad based implementation is considered, the pass band sensitivity is worse because in the presence of component inaccuracies, poles and zeros of each of the biquad stage track each other, but they do not track with the rest of the biquad stages [26], [27]. Both approaches are advantageous in their own ways. The biquad approach is simple to implement, as higher order filters can be realized by just cascading multiple biquads whereas a systematic procedure has to be followed to implement any kind of LC ladder based filter and the design can be complicated. This work uses a simple Butterworth biquad filter. As the basic idea is to implement the accurate tuning scheme, complicated filter designs are not explored. But this technique can be very easily extended to higher order filters.

A continuous time biquad structure can be obtained by using the general biquad transfer function H(s).

$$H(s) = \frac{{w_o}^2}{s^2 + \frac{w_o}{Q}s + {w_o}^2}$$

where w_o and Q are the pole frequency and the pole Q respectively.

Rearranging the equation gives,

$$V_{out}(s) = -\frac{1}{s}\left(\frac{w_o}{Q}V_{out}(s) - w_0 V_{c1}(s)\right)$$

where,

$$V_{c1}(s) = -\frac{1}{s}\left(w_o V_{in}(s) + w_o V_{out}(s)\right)$$

A signal flow graph describing the above two equations is shown below.

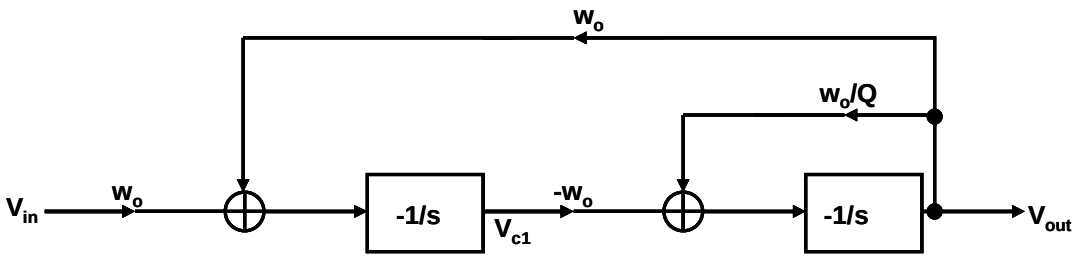


Figure 4.1 Signal flow graph of the biquad

The equivalent active RC realization for the signal flow graph is shown in Figure 4.2.

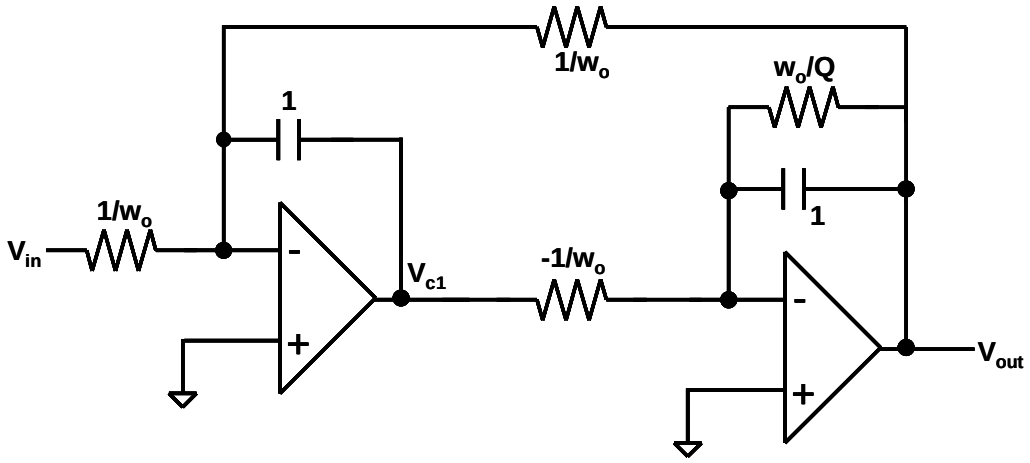
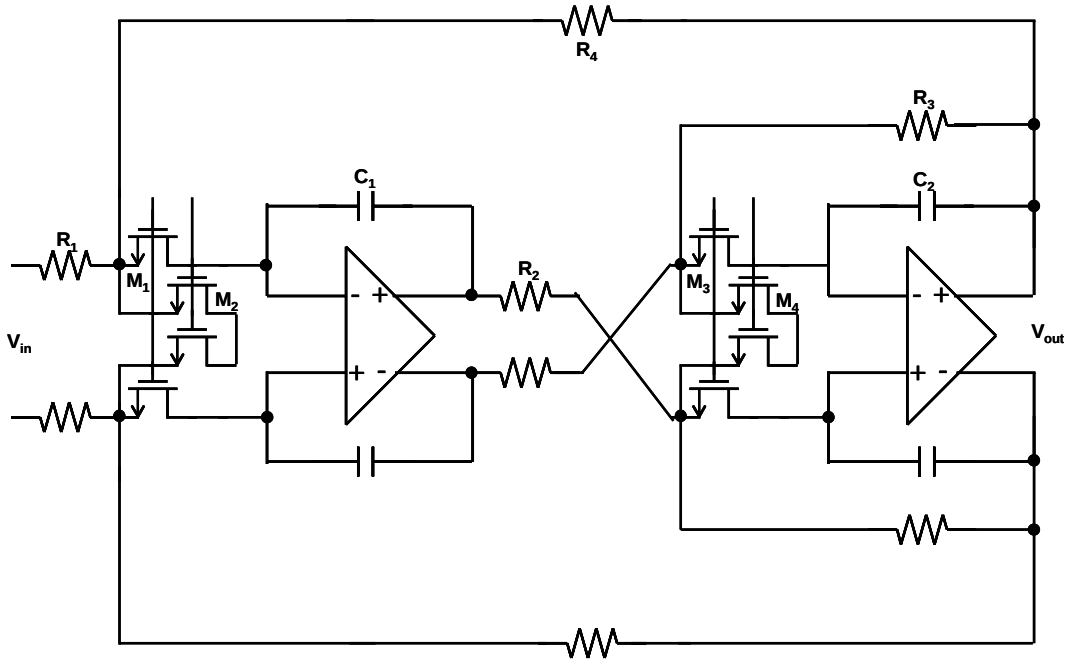


Figure 4.2 Single-ended equivalent active-RC implementation of the biquad

As discussed earlier in Chapter2, the R-MOSFET-C structure is used to improve the linearity of the filter. Also, a fully differential version of the filter is used to exploit the R-MOSFET-C structure. The negative resistor shown in Figure 4.2 can be implemented by cross coupling the 2nd stage inputs in a fully differential structure. The R-MOSFET-C version of the filter is shown in Figure 4.3. A differential structure is chosen so that the dynamic range is maximized and linearity improved because even-order harmonics are suppressed by fully differential circuits.



R1=47.76KΩ	R2=32.35KΩ	R3=33.35KΩ	R4=47.76KΩ	R1=47.76KΩ
C1=14.52pF	C2=10pF	M1,M2=2.5u/3.75u	M3,M4=2.5u/4.75u	

Figure 4.3 Fully differential R-MOSFET-C version of the biquad

The filter consists of operational amplifiers, MOSFETs in triode region, linear resistors and capacitors. The gain of the operational amplifier is chosen high enough to suppress the nonlinear distortion of the MOSFET within the filter's bandwidth according to the discussion in chapter 2. The source/drain ends of M2,M4 are left floating because, the circuit will set these voltages to the common mode voltage. Also, not cross coupling helps in improved noise performance. Simulated AC response of the filter is shown in Figure 4.4

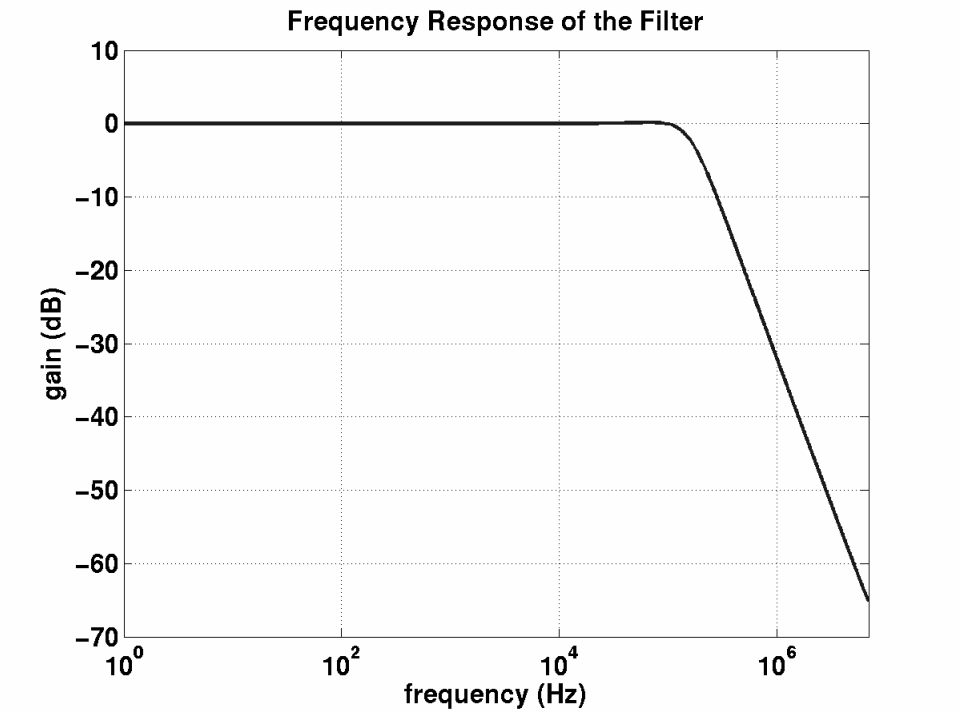


Figure 4.4 Filter AC response

Operational Amplifier Design

A high gain two stage operational amplifier was chosen so that the first stage provides the high gain and the second stage provides high output swing to maximize the dynamic range [23]. High gain of the opamp helps in having enough loop gain for lower frequency inputs and thus improves the linearity of the filter significantly [3]. The operational amplifier is shown in Figure 4.5. Miller compensation is used to stabilize the opamp. As it is a fully differential structure, there is a definite need for a common mode feedback circuit (CMFB). As the second stage is not a very high gain stage, a resistive CMFB can be used. For the gain of the opamp to be not limited by the resistive CMFB, the resistors are chosen to be the dominant factors contributing to the overall opamp gain. The opamp along with the CMFB can be seen in Figure 4.5. The opamp simulated gain = 80dB, bandwidth = 35MHz and phase margin = 60^{o} .

The gain and phase plot is shown in Figure 4.6. The opamp is designed such that it will provide an output swing of $1V_{pp}$ differential.

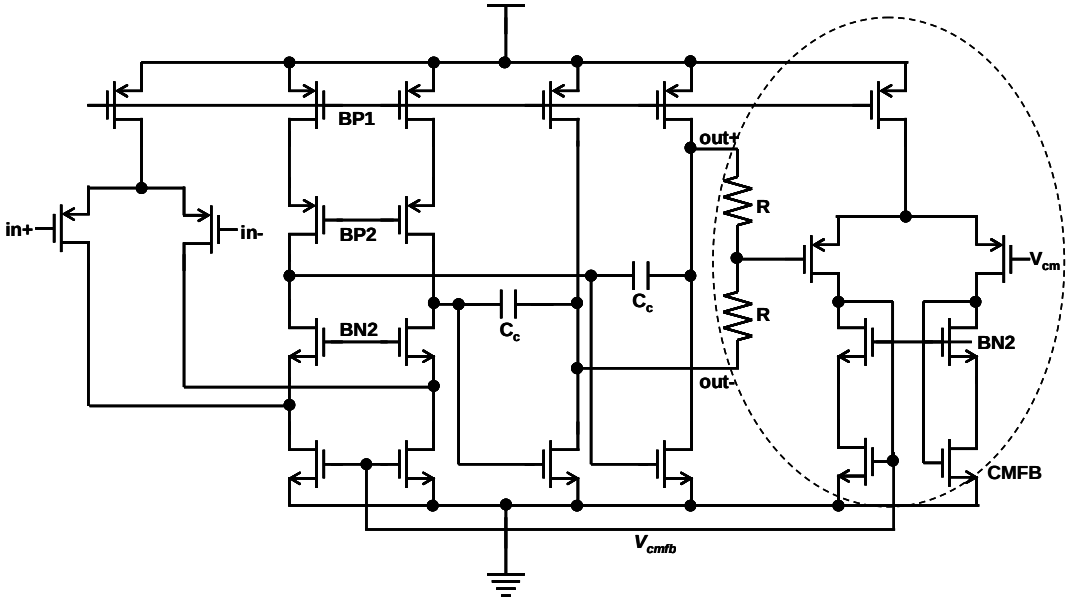


Figure 4.5 Operational amplifier used in the filter.

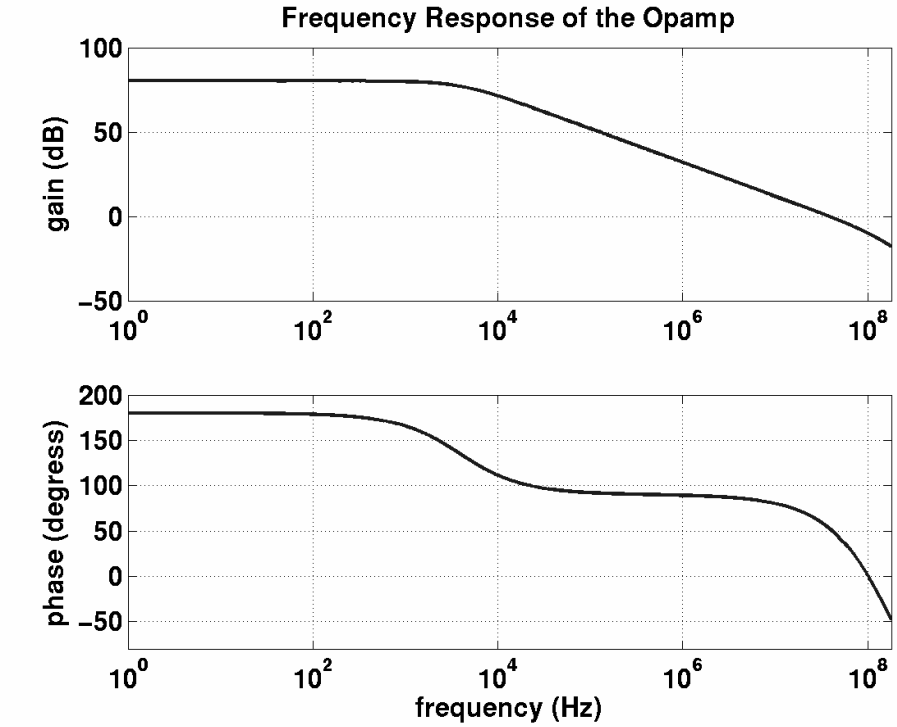


Figure 4.6 Opamp AC response

4.1.2 Tuning Circuit Implementation

The other important part of the proposed system is the tuning circuit. Inaccuracies in frequency response of the filter are contributed mostly due to the RC time constant variation. The RC time constant varies due to environmental factors such as temperature changes, ageing, etc. This error results in a shift of the frequency response of the filter. In applications which employ these filters as anti-aliasing or smoothing filters in conjunction with sampled data filters, this shift in frequency response can be accommodated if the sampling frequency to signal frequency ratio is high. In other applications, this variation in the frequency response may not be tolerated. To overcome this time constant variation, continuous time filters employ automatic on-chip tuning. Tuning based on external reference is widely used in most of the cases. This external reference can be a reference clock or a very accurate reference resistor. In case where a 10 percent accuracy can be tolerated, it can be sufficient to set only the R value to an external reference whereas the 10% variations are accounted for capacitor variations.

For many of the applications, accuracy is critical. In such systems, one must clearly take capacitor tolerances also into account. A precise tuning of RC time constant can be obtained if an accurate reference clock is available. This reference clock can be used to set the RC time constant to an accurate value.

The tuning circuit implementation is done based on switched capacitor resistor reference. The circuit configuration is very similar to the one discussed in chapter 2

(refer Figure 2.6), but a slight modification is made to accommodate for the fully differential tuning demanded by the R-MOSFET-C structure [3].

The complete schematic of the tuning circuit used for the automatic tuning of the filter is shown in Figure 4.7. The lower portion of the circuit provides the common mode control voltage V_{CM} which maintains the designated voltage scale factor F (F-factor is discussed in Chapter2). The common mode voltage merges with the differential tuning voltage at the input of opamp3 in Figure 4.7. The time constant matching in this case is accomplished by varying the differential control voltage V_{cp} - V_{cn}. Figure 4.9 shows the transient settling of the control voltages V_{cp} and V_{cn}.

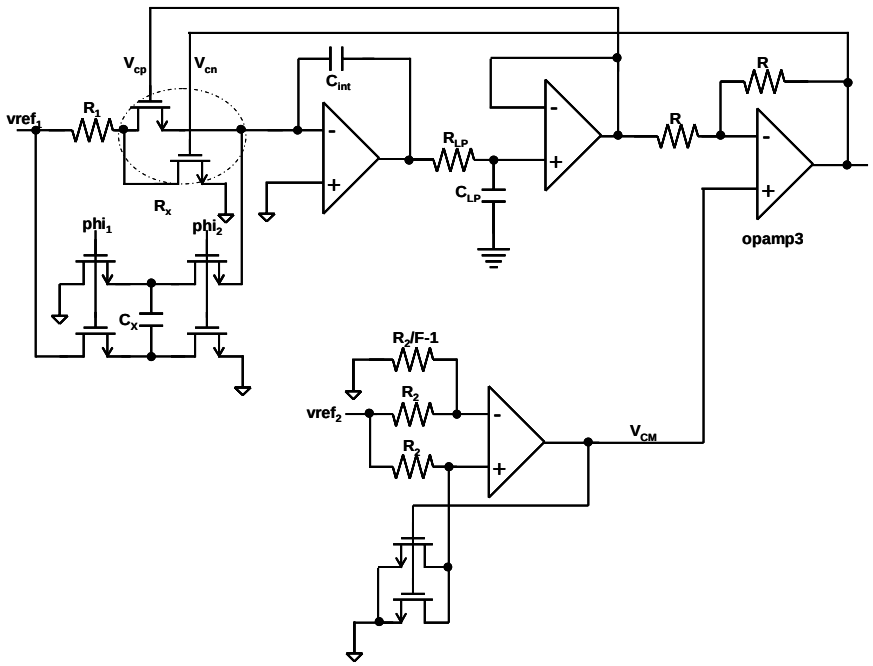


Figure 4.7 Tuning circuit to provide differential tuning

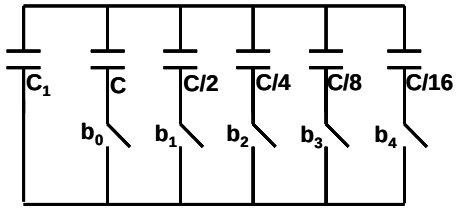


Figure 4.8 C_X is replaced by a capacitor bank shown.

As discussed before, the accuracy of the time constant matching is limited by the mismatch between the master time constant ($f_{clk}C_X/C_{fil}$) and the slave time constant $1/R_{fil}C_{fil}$. In the proposed system, the mismatch minimization is performed through the master block. Once the mismatch is detected, it is corrected for by varying the capacitor C_X (as shown in the capacitor bank) based on the amount of mismatch. The control word (b_0….b_4) for the capacitor bank is generated automatically on power-up by the proposed scheme. Once the mismatch is minimized, the control word is frozen and the filter can operate along with automatic tuning but with the mismatches minimized. Effectively, the process, temperature, etc. variations are tracked well by the tuning circuit and the existing mismatch is minimized on power up. Such an arrangement can achieve very accurate filter corner frequencies in the presence of process, temperature, etc. variations and mismatches.

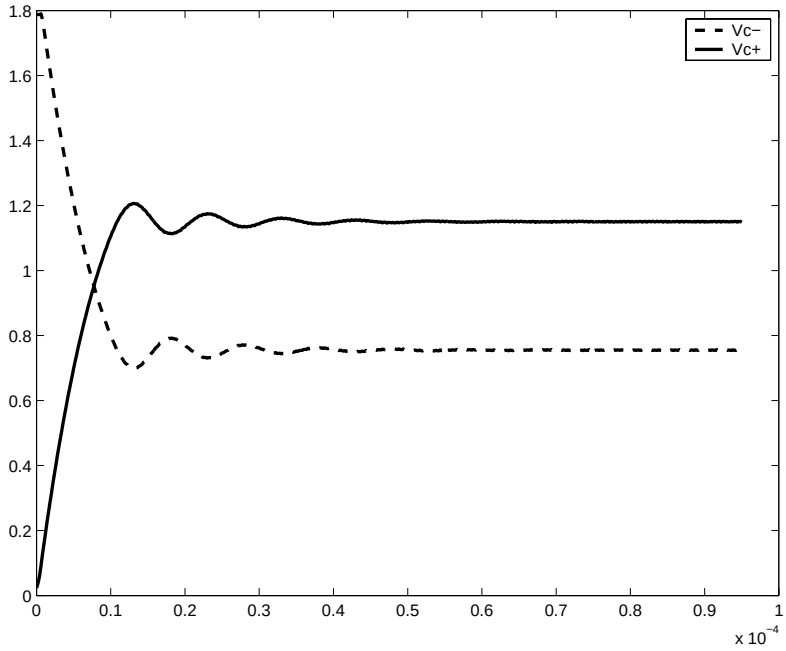


Figure 4.9 Simulation result showing control voltage settling.

4.2 Mismatch Minimization Implementation

The tuning circuit sets the -3dB corner frequency of the filter based on the reference switched capacitor resistor. If the input is given to the filter at the corner frequency, the output should ideally be -3dB attenuated compared to the input. But due to mismatch between the switched capacitor resistor (master) and the filter resistor (slave), the output will not be ideal. This section deals with the details of how the mismatch is detected and corrected.

4.2.1 Sine-wave Generation

As explained in chapter 3, the mismatch minimization is done on power up. This is performed by combining direct tuning on power up along with the master slave tuning. As shown in Figure 4.9, a sine wave of desired frequency (corner frequency) is generated. Sine-wave generation is done assuming that only clock is available on power up. Using the clock and combining it with a digital state machine, a digital output is obtained which in turn feeds a non-linear digital to analog converter (DAC). The generation of digital logic, the principle and operation of the DAC is discussed in this section. The block diagram of the sine wave generation is shown in Figure 4.10.

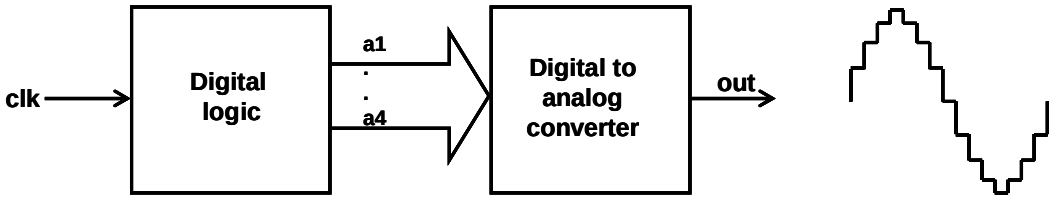


Figure 4.10 Block diagram of sine-wave generation

The digital logic consists of a bi-directional shift register along with some combinational logic which will generate digital outputs as needed by the DAC (a_1, a_2, a_3, a_4 as shown in Figure 4.11). After the desired outputs are obtained from the digital logic, the DAC is used to generate the sine wave using the outputs provided by the

digital block. A current mode DAC is chosen for its simplicity and ease of implementation in the context of this application.

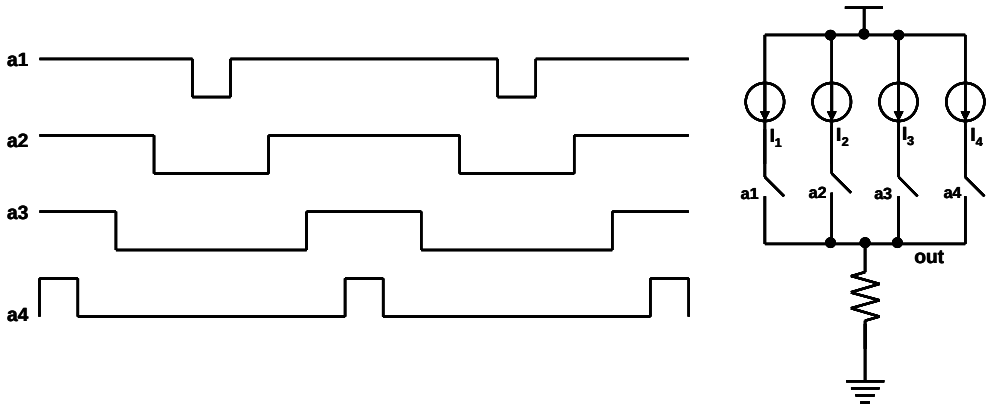


Figure 4.11 Current Mode Digital to Analog Converter.

Table 4.1 Table showing the current source sizing ratios

Current source	Ratio
I1	sin(π/8)
I2	sin(π/4)-sin(π/8)
I3	sin(3π/8)-sin(π/4)
I4	sin(π/2)-sin(3π/8)

Digital to Analog Converter (DAC)

The conceptual diagram of the current mode DAC and the inputs of the DAC are shown in Figure 4.11. The output of the DAC is in the form of a sine-wave. To obtain this, the current sources are sized according to the sine wave output as shown in table 4.1. For example, for 4-bit DAC used for this purpose, one quarter of the

sine-wave is generated by dividing the range from 0 to sin(π/2) into 4 voltage levels. Table 4.1 shows the ratio of the steps of a quarter sine-wave. The current sources are sized according to the values given in the table. The DAC is nonlinear in the sense that the output levels of the DAC are not equal but are in a corresponding sine-wave format. Actual implementation is done differentially, this requires eight current sources instead of four for the single-ended case.

The implementation of the DAC can be seen in Figure 4.12 Current sources I_1….I_4 are sized in the ratio of values in Table 4.1. Similarly current sources I_5….I_8.are sized accordingly. The implementation of each of the current sources is done as shown in Figure 4.13.

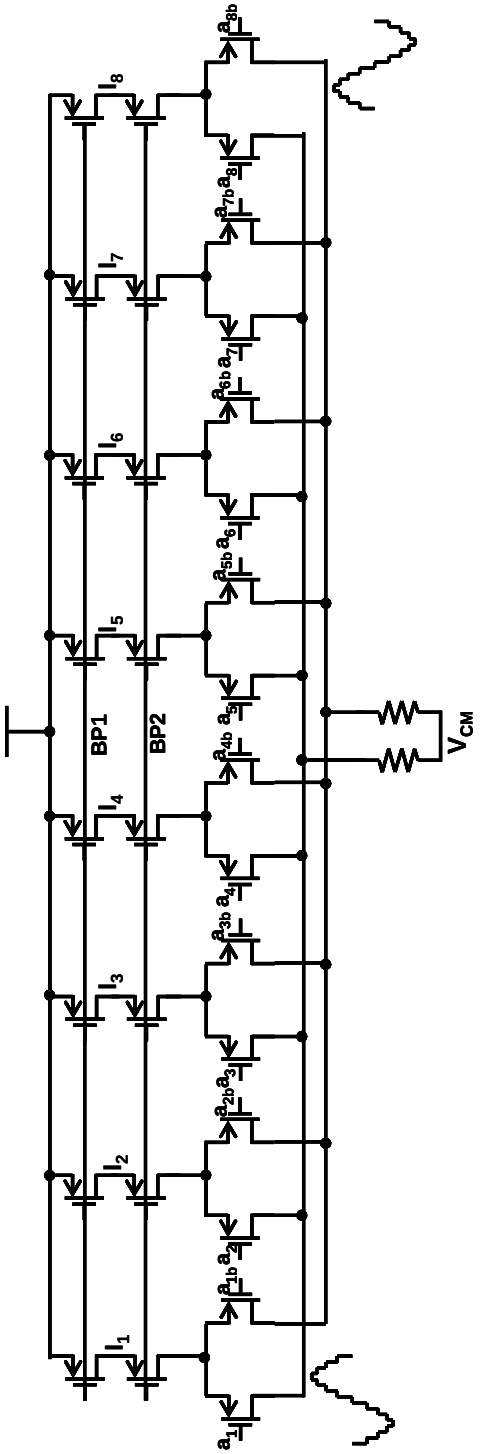


Figure 4.12 Differential current mode DAC

Cascoding is used to obtain good current matching, which is attained by minimizing the effect of channel length modulation.

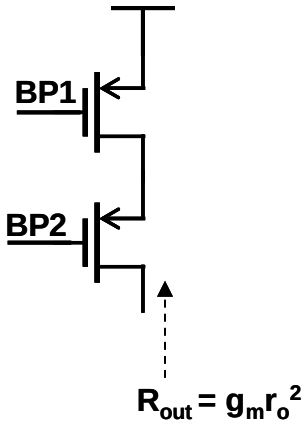


Figure 4.13 Figure showing improvement of output impedance by cascoding.

The lengths of the current sources are made long such that the "r_o" of each transistor is maximized and results in improving the output impedance of the current source. The V_{eff} i.e. (V_{GS}-V_{TH}) of the transistors is made large such that the V_{TH} mismatch between the current sources is minimized. Mathematical analysis can be performed to calculate the effect of W/L mismatches and V_{TH} mismatches in the current sources and the result is shown below [23].

$$\frac{\Delta I_D}{I_D} = \frac{\Delta W / L}{W / L} - 2\frac{\Delta V_t}{V_{GS} - V_t}$$

As per the above equation, the current mismatch is minimized by increasing V_{GS}-V_{TH} and increasing W, L.

4.2.2 Mismatch Detection and Correction

Any error in the filter's corner frequency can be detected by observing the transient output of the filter. If an input given to the filter is exactly at the corner frequency, the output is expected to be -3dB attenuated. Any deviation from the -3dB attenuation indicates an error in the corner frequency of the filter. Now if the power-up generated sine wave(frequency = corner frequency of the filter) is fed to the filter which is running along with the background tuning scheme, the output amplitude of the filter should ideally be -3dB less than the input amplitude. But due to the presence master-slave mismatch, the output will be different from the expected value. This error can be detected and corrected.

Mismatch detection is done as follows. The output of the filter can be known by determining the peak output value. The ideal peak value should be -3dB attenuated from the input peak value. The peak of the filter output can be detected by using a peak detector. This detected peak is compared with the ideal peak and an error signal is obtained. This error signal resulting from the comparison is then be used to do the necessary correction to minimize the mismatches.

If there are any common mode variations at the output of the filter, then the detected peak of the output may not really reflect the real peak that indicates the -3dB attenuation as shown in Figure 4.14. If the output peak to peak value of the filter is

determined instead of just the peak value, even in the presence of any common mode variations the peak to peak value of the output reflects the real output value.

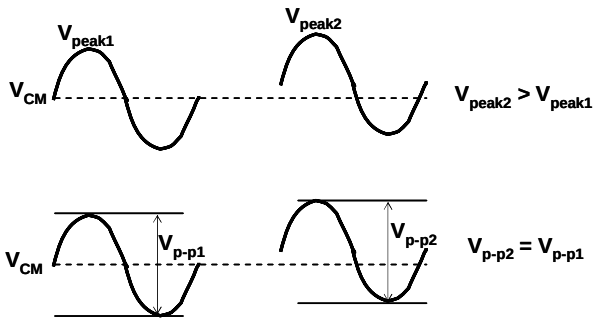


Figure 4.14 Output peak and peak to peak values illustration

The mismatch detection and correction block diagram is shown in Figure 4.15. Here, the output peak to peak value of the filter is compared with the ideal peak to peak value (corresponding to V_{ref}) and the comparator's output is used for correction. The generation of ideal output peak to peak can be done by externally providing a reference and generating both the positive and negative peak values.

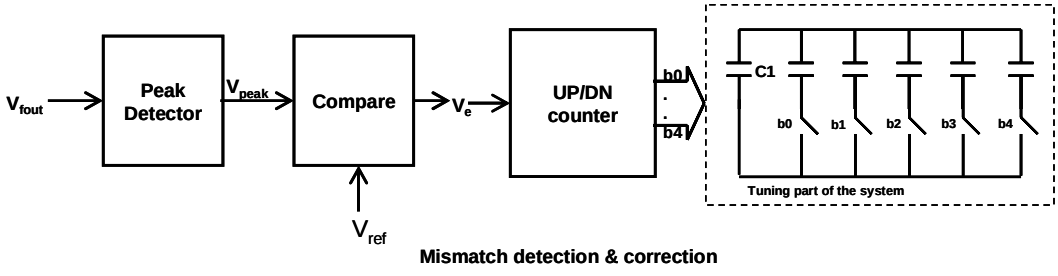


Figure 4.15 Mismatch detection and correction

The counter output can be used to modify the capacitance of the master switched capacitor resistor as discussed previously. As shown in Figure 4.14, this capacitor is replaced by a capacitor bank and the capacitors in the bank can be switched ON/OFF depending on the output of the comparator. The input to the UP/DN counter is the output of the comparator. The output of the comparator indicates if the mismatch is positive or negative i.e., if the filter's (slave) equivalent resistance is greater then or less than the switched capacitor resistance (master).

If the comparator's output is logic 1, the counter counts UP switching the capacitors ON and if the comparator's output is logic 0, the counter counts down, switching OFF the capacitors, thus decreasing the net capacitance in the switched capacitor resistor. The sizing of the switching capacitors in the capacitor bank is decided based on the amount of total mismatch that can be corrected. This work assumes that in the worst case there can be ±10% mismatches present and the capacitor bank is designed accordingly.

The circuit level design of the mismatch detection and correction is explained in the following section. As mentioned before, all the circuit level design is done in a fully differential manner to obtain good linearity, better signal swing and high common mode rejection.

Peak Detector

In the peak detector shown in Figure 4.15, a comparator is used to determine if $V_{in} > V_{ppeak}$. When such a condition occurs, the output of the comparator goes high

and the transmission gate (TG) turns on, forcing $V_{ppeak}=V_{in}$. As long the input remains less than V_{ppeak}, the comparator's output is low and the TG is off [22]. As soon as the input goes above V_{ppeak}, the TG turns back on and new peak is stored on the capacitor C_{hold}. The peak detector has a decaying circuit to reset the peak periodically such that the circuit will be able to detect a new peak each cycle. This is very critical because, when the control word of the switched capacitor resistor is updated, the output of the filter changes and the peak detector should be able to provide the comparator with the correct peak value. So, the peak detector reset is done every clock cycle along with the counter update. As the whole system is implemented differentially, two peak detectors are used to detect the both the positive peak and negative peak.

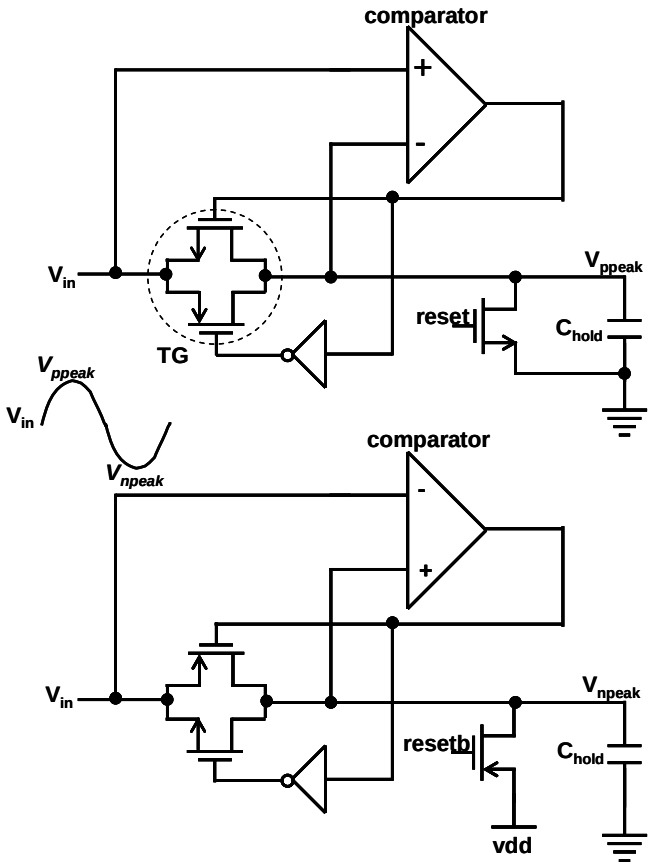


Figure 4.16 Peak detector circuit: Two used to detect both V_{ppeak} and V_{npeak}

Comparator

The comparator compares the peak to peak value of the filter output and the ideal peak to peak value. But the peak detector provides only the positive and negative peaks and not the exact peak to peak value. Similar is the case with the ideal positive and negative peaks. For this purpose of peak to peak voltage comparison, a differential difference comparator is used. This comparator compares the peak to peak

value of the output to the ideal peak to peak value. The implementation of the comparator is shown in Figure 4.16 [22].

$$V_{inp}+V_{refp} > V_{inn}+V_{refn}$$

$$\Rightarrow \quad V_{inp}-V_{inn} > V_{refp}-V_{refn}$$

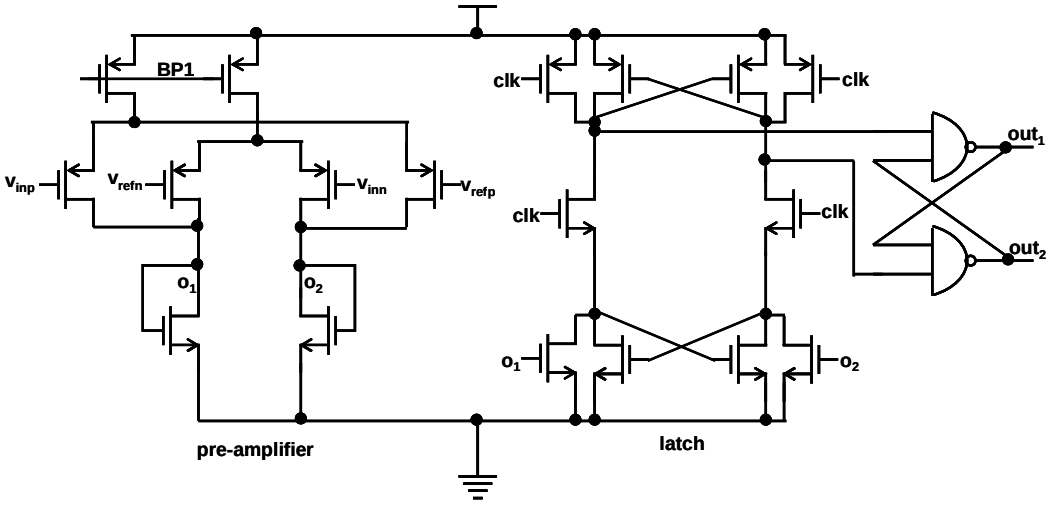


Figure 4.17 Differential difference comparator. It consists of a pre-amplifier and a latch.

The comparator consists of a preamplifier and a latch. The preamplifier prevents the comparator kickback from the output to the inputs of the comparator. The transistors in the preamplifier and the latch are made wide and long to minimize any random offsets contributed by the device geometry mismatches.

Counter

The comparator output drives the UP/DOWN counter. The UP/DOWN counter is designed using conventional synchronous logic. The number of bits for the counter is determined by the number of capacitors needed that can be switched ON/OFF to correct for the mismatch. 5 bits were chosen such that the necessary mismatch correction could be performed. T flip flops are used for the purpose of the counter design. The counter is a 5 bit UP/DOWN counter designed using sequential logic.

The system design is done in such a way that when the power up control loop settles, the last bit of the control word toggles. The corner frequency change due to the variation in the control voltage resulting from the toggling of the last bit is within the specified accuracy limit (<1% variation).

4.2.3 Timing Considerations

Essentially on power up there are two loops running simultaneously. The background tuning loop to take care of the process, temperature variations and the mismatch minimization loop to alleviate the mismatch between the master and the slave. It is of prime importance to guarantee that these two loops do not interact and cause some potential errors in the system. This can be done by ensuring proper timing for each of the loops. For example, if the background tuning loop settles in 0.5ms, then the mismatch minimization loop should be run such that after each update of the control word, the background tuning loop must settle before the next update occurs.

Therefore, mismatch minimization should be a relatively slower loop than background tuning loop. The timing diagram can be seen in Figure 4.17, along with the peak detector reset timing. Simulations indicates background tuning circuit settles in < 500us as shown in Figure 4.9.

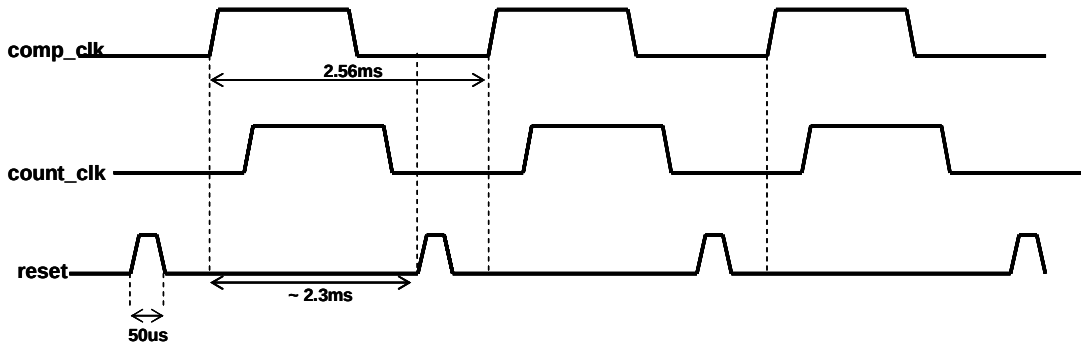


Figure 4.18 Timing diagram of the power up tuning loop

5. EXPERIMENTAL RESULTS

A 200 kHz -3dB frequency, 2nd order low pass filter was designed in 0.18µ CMOS technology. The filter is tuned very accurately by using a novel mismatch minimization scheme. This chapter presents measurement details of the fabricated chip. The chief claims of the work: linearity, low-voltage operation, accurate tuning are verified and appropriate results are presented. The initial part of the chapter presents and discusses the key measurement results and the latter describes the problems encountered in the process of measuring the chip and possible solutions.

5.1 Measurement Results

Figure 5.1 shows the measured output spectrum for a 10 kHz, 250mVpp input signal for the filter. It can be seen that the Total Harmonic Distortion (THD) is -81dB (power supply of 1V). Total harmonic Distortion Vs input swing for various power supplies is shown in Figure 5.2. It can be seen from the figure that the filter has -80dB THD for a 10 kHz, 200mVpp input signal with a power supply of 0.8V. Also as the input signal swing is increases, the THD degrades as expected because of the non-linearities from the opamp 2nd stage and MOSFET resistors. As the power supply increases, it is observed that there is a slight improvement in the THD. Signal to Noise Ratio for a 250mVpp 10 kHz input signal is 56dB. The overall SNR is lower than expected, the main reason being flicker (1/f) noise of the opamp. Figure 5.1 confirms this claim: the low frequency noise has a slope approximately equal to -10

dB/dec, which essentially is due to 1/f noise. If the 1/f noise is neglected, then SNR is about 84dB. Figure 5.3 shows THD Vs input frequency. It can be concluded from this figure that as the input frequency is increased, the Total Harmonic Distortion of the filter degrades. This is due to the fact that the loop gain decreases as the bandwidth of the filter is approached which results in less suppression of the non-linearities due to the MOSFET resistors used in the filter.

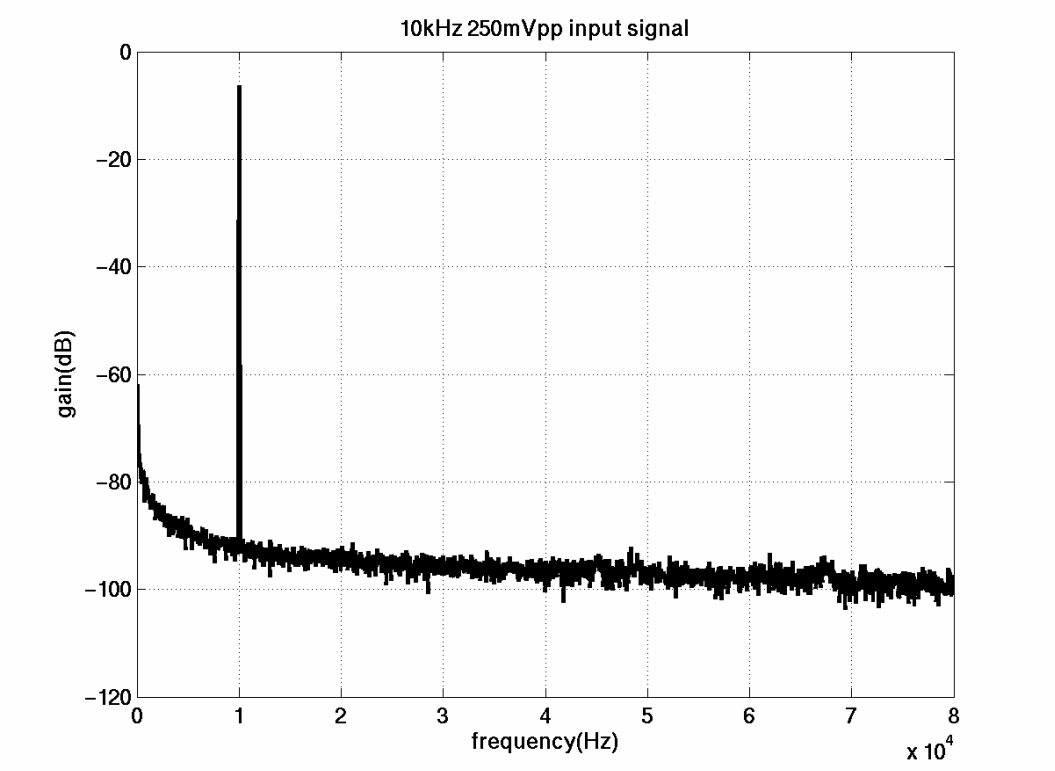


Figure 5.1 Measured output spectrum of a 10 kHz 250mVpp input signal.

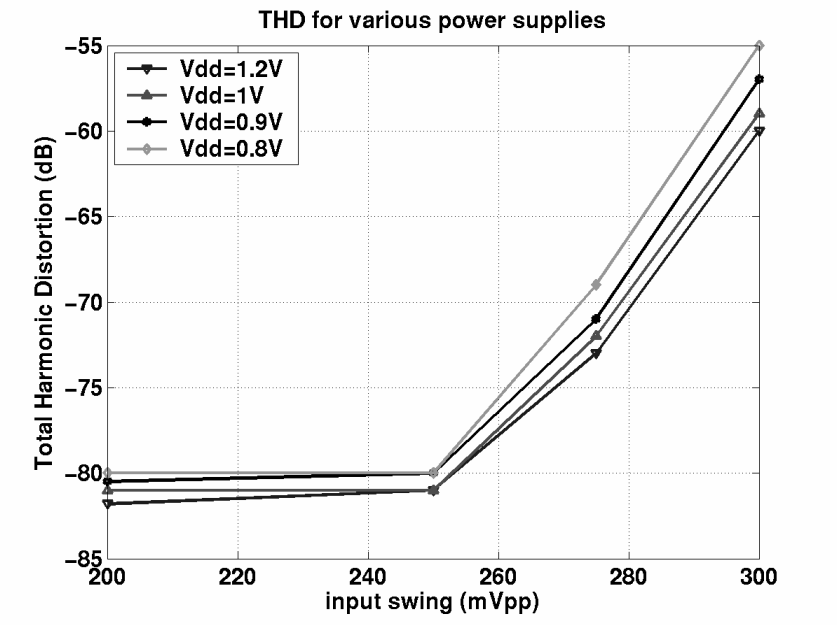


Figure 5.2 Figure showing THD Vs input signal swing for various power supply voltages.

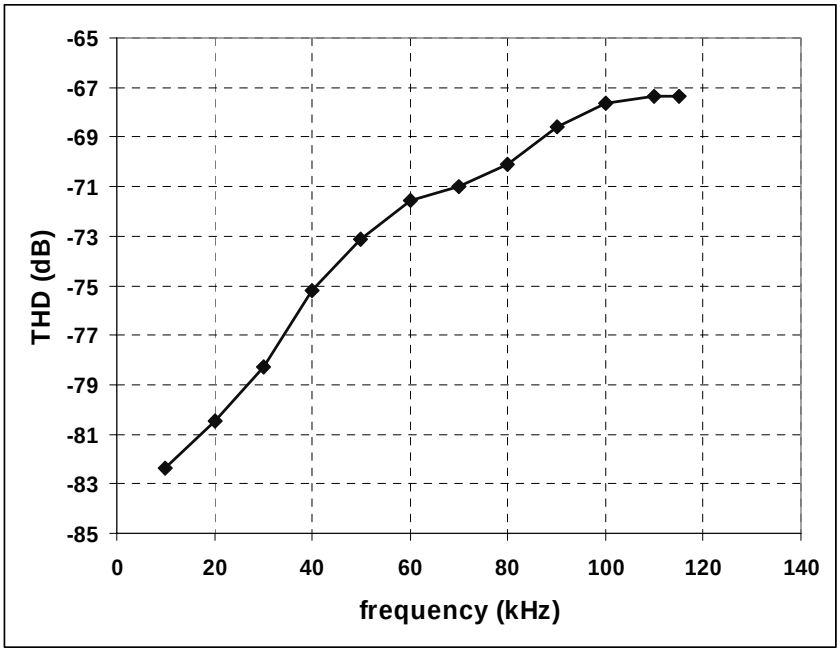


Figure 5.3 THD Vs Input frequency.

Measurement results demonstrating the power-up tuning for the system are presented in this section. Figure 5.4 shows the measured frequency response of 3 chips with the power-up mismatch minimization scheme OFF, Figure 5.5 indicates the measured frequency response of the same 3 chips with the power-up mismatch minimization performed. It can be concluded from Figures 5.4 and 5.5 that the filter is tuned to an accurate corner frequency (115 kHz) when the power-up mismatch minimization scheme is ON. The corner frequency of 115 kHz was chosen based on Table 5.1. The explanation of how Table 5.1 is arrived at is given in the next section.

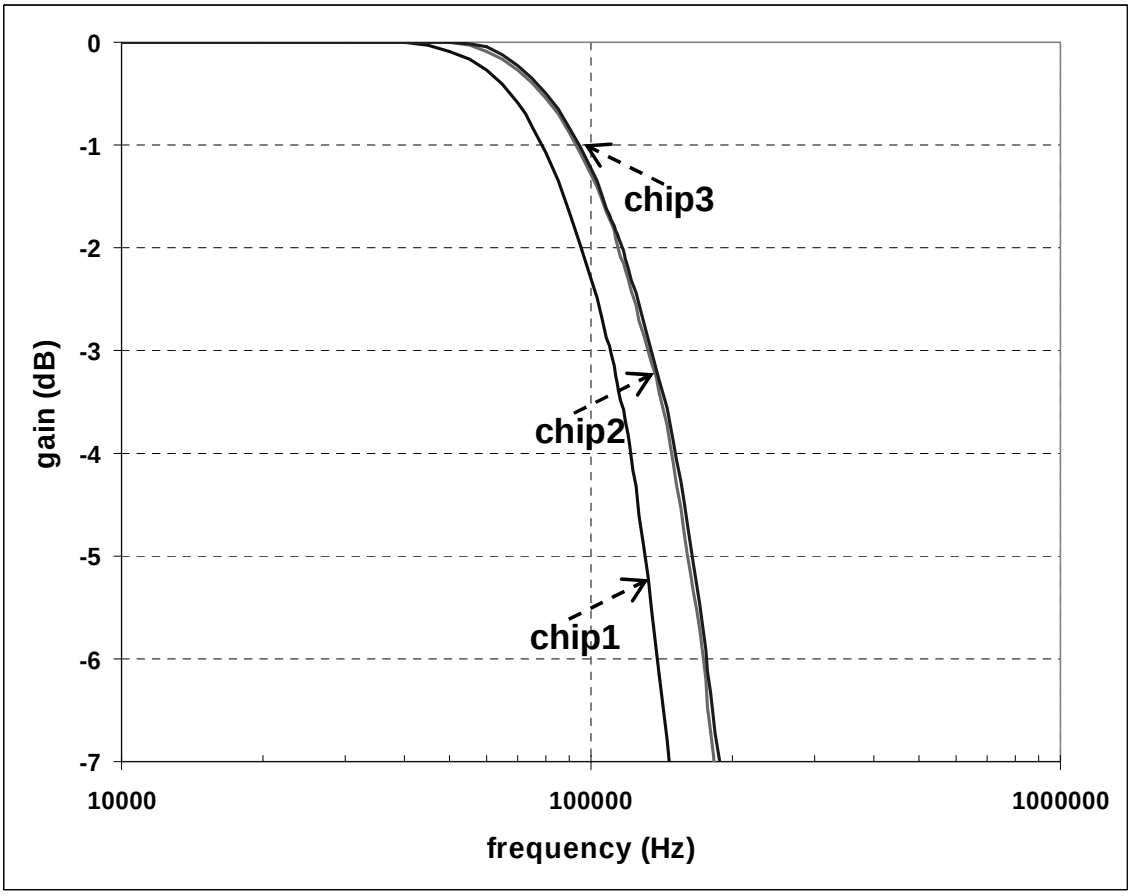


Figure 5.4 Frequency responses of 3 chips with power-up mismatch minimization scheme OFF. f_{-3dB1}=106kHz, f_{-3dB2}=129kHz, f_{-3dB3}=130kHz.

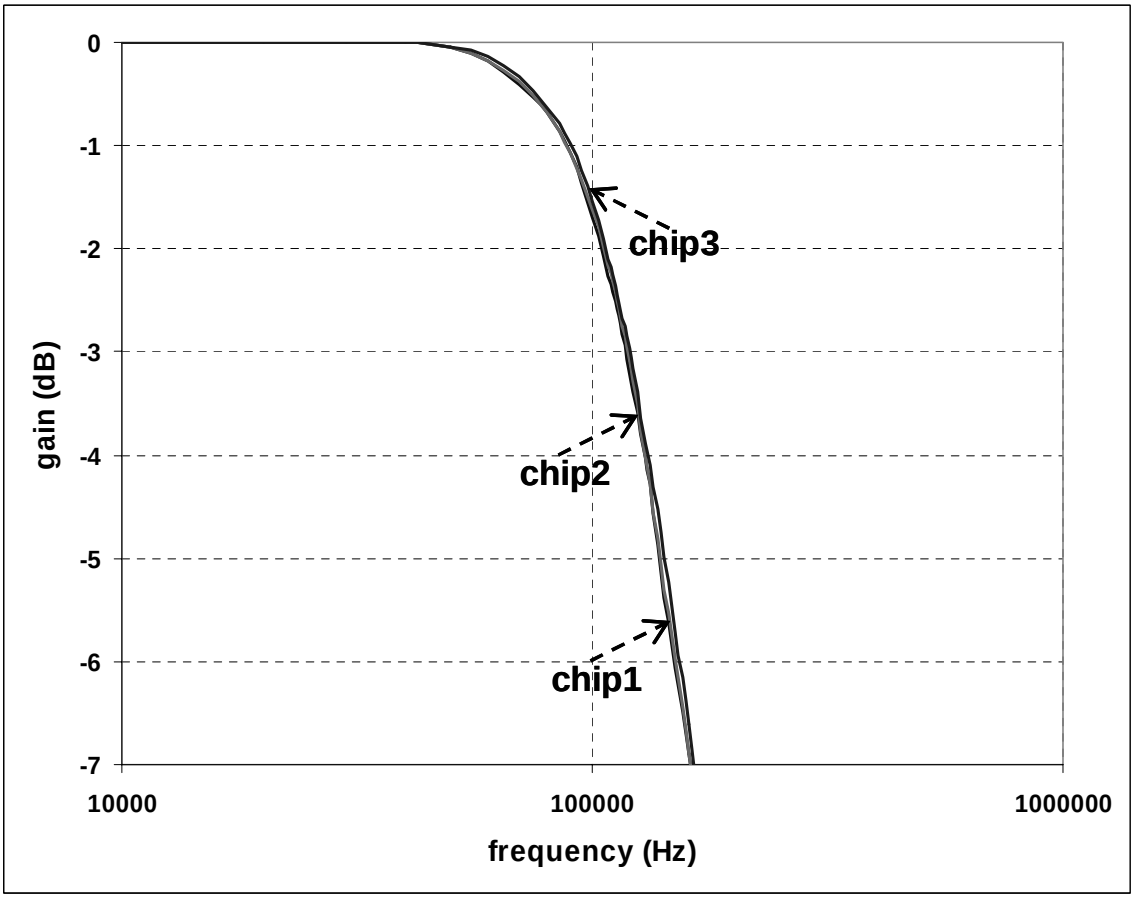


Figure 5.5 Frequency responses of 3 chips with the power-up mismatch minimization scheme ON. f_{-3dB1}=117kHz, f_{-3dB2}=119kHz, f_{-3dB3}=120kHz

Table 5.1 Table showing the frequency ranges for various chips. Chip#1,2,3 are chosen for demonstration of accurate corner frequency measurement.

chip#	frequency range(kHz) low	high
1	*105*	*132*
2	*101*	*123*
3	*106*	*131*
4	138	147
5	105	109
6	110	114
7	107	112
8	100	104
9	103	109
10	103	110
11	124	131
12	126	130
13	119	125
14	129	138
15	133	140
16	139	144
17	138	143
18	142	146
19	141	146
20	144	149
21	149	156
22	147	152
23	150	155
24	154	158
25	162	169
26	183	192

5.2 Measurement Issues

This part of the chapter deals with the problems that are encountered in the process of measurements due to various reasons. It was observed that the control voltage outputs (Vcp, Vcn) of the tuning circuit (shown in Figure 4.7) are oscillating for certain clock frequency inputs. Measurements are performed on various chips to

confirm these oscillations. Each chip is found to be having a certain range of clock frequencies for which the tuning control voltages are stable. Table5.1 lists the range of corner frequencies, which essentially are set by the clock frequencies of the tuning circuit for each chip that has been tested. Table 5.1 is prepared after measuring various chips and determining the range for which the control voltage outputs are stable. Three chips (#1,#2,#3) have a comparatively wide overlapping frequency range and these 3 chips are used to arrive at the results presented in Figures 5.4 ad 5.5 to verify the accurate tuning of the filter. The corner frequency is chosen based on the frequency ranges to be 115 kHz. The possible explanation for the oscillations in the tuning control voltages is that, the tuning loop has 2 dominant poles: one contributed by R_{LP} and C_{LP}, the other by C_{int} and the equivalent R-MOSFET resistor. R_{LP}, C_{LP} are implemented using a MOSFET resistor and MOSFET capacitor, but the equivalent MOSFET R_{LP}, C_{LP} vary due to gate voltage, process, temperature, etc. variations, thus changing the equivalent dominant pole $1/(R_{LP}C_{LP})$ which might have caused oscillations. One solution for this problem is to replace the R_{LP}, C_{LP} by real linear resistor and capacitor so that the equivalent pole resulting from R_{LP}, C_{LP} is not varying very widely. Also a detailed stability analysis should have been done to verify the tuning loop stability at the design phase.

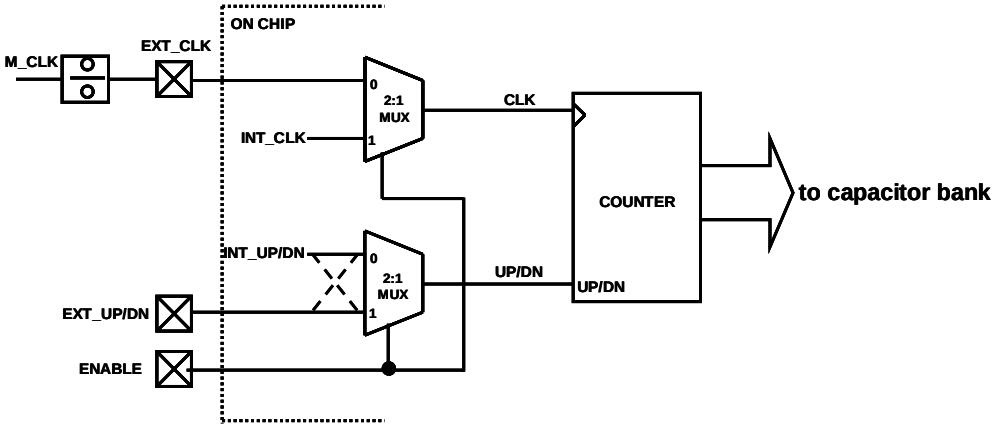


Figure 5.6 Control logic for the operation of power-up mismatch minimization scheme. Dashed lines at the input of the MUX indicate the correct connections for the control logic.

Another issue, which is mainly due to a design problem in the control logic, is observed in the process of measuring the chip. As shown in Figure 5.6, the design is made such that, when the control signal, ENABLE is logic 1, then the power-up mismatch minimization has to be performed. On the other hand when ENABLE is logic 0, an option of tuning the filter externally using the counter is incorporated (dashed lines in Figure 5.6). But the problem in the control logic does not allow for the required operation because, when ENABLE is logic 1, then the internally generated clock for the counter is active whereas the externally provided UP/DN is also active at the same time. This allows the counter to always count UP or count DN depending on the external UP/DN input. This problem is overcome by making ENABLE as logic 0 and providing the internally generated UP/DN for the counter and simultaneously providing the necessary external clock for the counter to be

triggered thus updating the output of the counter based on internally generated comparator output to tune the filter accurately. The external clock is provided with the appropriate division using the master clock as the reference.

A die photograph of the fabricated chip and a brief performance summary are presented here.

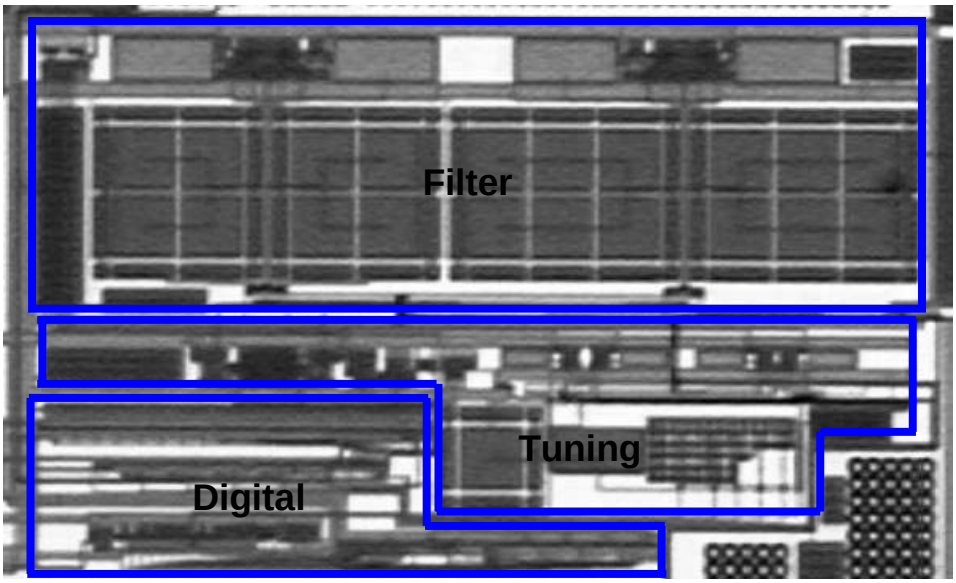


Figure 5.7 Die photograph of the fabricated chip.

Table 5.2 Performance summary table.

Performance Summary	
Corner frequency	115 kHz
Die area	800u x 500u
Power consumtion	Filter : 2.6mW (Vdd=1V)
	Tuning : 7mW (Vdd=1.8V)
Linearity (THD)	250mVpp, 10kHz signal: -81dB (Vdd=0.8V)
Signal to Noise ratio(SNR)	250mVpp, 10kHz signal: 55dB

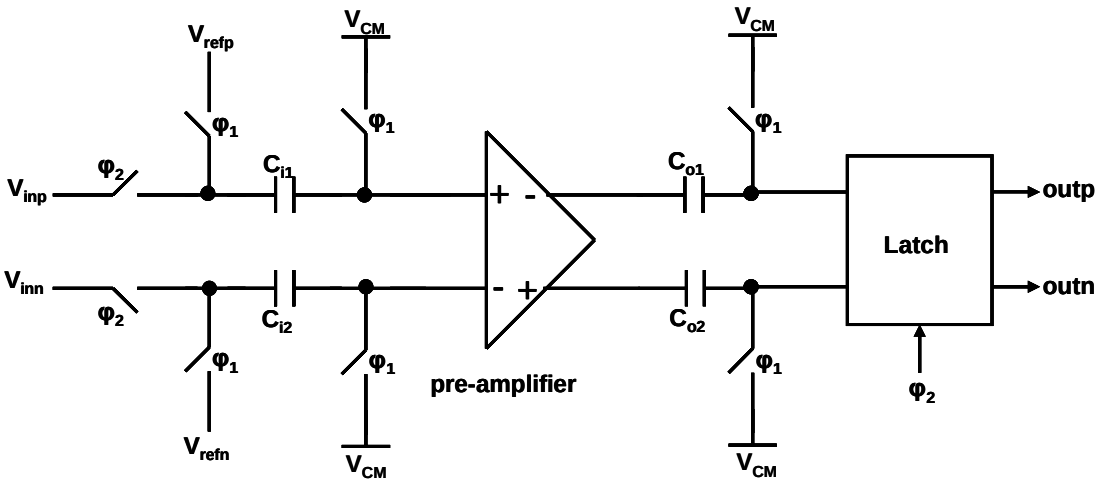
6. LIMITATIONS AND SUGGESTED IMPROVEMENTS

The idea of mismatch minimization discussed in the previous chapters is to tune the filter's corner frequency very accurately. The implementation is explained in Chapter4. The accuracy of this method can be limited by the type of implementation used.

6.1 Comparator Offsets

The implementation discussed in Chapter 4 does not consider the offsets of the comparators used in the mismatch detection and correction blocks. Mainly, the offset of the comparator used to compare the peak to peak value of the filter output to the ideal peak to peak value directly affects the control word that modifies the master reference resistor.

Also the offset of the comparator used in the peak detector might not detect the accurate peak of the output in presence of any inherent offsets. Offset cancellation can be performed on these comparators to minimize the offsets. The comparator used for the comparison of the output peak to peak and the ideal peak to peak can be offset compensated by modifying the circuit of the comparator shown in Figure 4.16.



φ_1 phase: output offset storage, φ_2 phase: offset cancellation and comparison.

Figure 6.1 Comparator with offset cancellation

As shown in Figure 6.1, offset cancellation can be performed by storing the amplified offset of the comparator at the output using capacitors C_{o1}, C_{o2}. With output offset storage method, the offset is cancelled by shorting the pre-amplifier outputs to V_{CM} and storing the amplified offset of the comparator at the output [17]. The offset contributed by the latch part of the comparator can be minimized by having a high gain pre-amplifier. But, on the other hand, if the gain of the pre-amplifier is high, during the offset storing phase, the outputs of the pre-amplifier will saturate and the offset cancellation is not performed accurately. Typically the pre-amplifier should be designed with a gain of less than 10.

Note that the preamplifier is just a differential amplifier instead of a difference differential amplifier that was used in Figure 4.17. The difference operation can be performed using switches and capacitors at the input of the preamplifier (C_{11}, C_{12}). In

one phase the input capacitors store the ideal reference peak values and in the next phase, the capacitor provides the difference between the output peak and the reference peak to the input of the pre-amplifier. Implementation of the pre-amplifier can be seen in Figure 6.2.

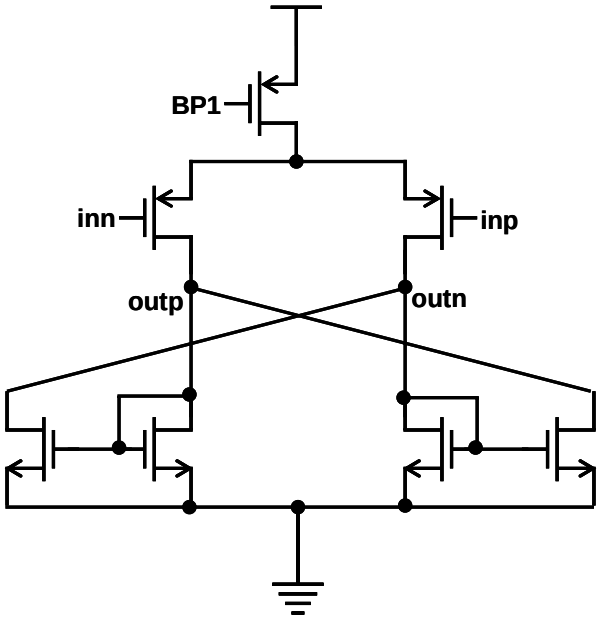


Figure 6.2 Pre-amplifier circuit

6.2 Low-voltage issues in continuous-time filters and possible solutions

Chapter 2 discussed in brief about the key issues encountered in the design of low-voltage continuous time filters. The solutions to some of the issues discussed in Chapter 2 are proposed here.

The design of tuning circuit using a low V_{DD} is a challenging task because the tuning circuit may not provide enough tuning range to compensate for all the process, temperature variations because the control voltage is limited by the supply voltage. In this section, a couple of solutions are proposed to overcome the tuning range problem but still maintain the device reliability constraints i.e. any terminal-terminal voltage of the transistor should never exceed V_{DD}.

A PMOS resistor is used in place of the tunable element in the filter. The resistance of the PMOS can be varied by changing the gate voltage of the transistor automatically to tune the filter. The tuning range limitation can be eliminated by generating a control voltage (V_G) which is equal to V_{cntrl}-V_{CM}. But, low-voltage design demands the terminal to terminal voltage to not exceed V_{DD}. The circuit shown in Figure 6.3 generates the differential control voltages needed for the filter to be tuned. This circuit is a variant of the clock boosting circuit proposed in [18].

It provides a varying signal from V_{cp} to V_{cp}-V_{DD} and V_{cn} to V_{cn}- V_{DD}. The tunable PMOS resistors need the voltages V_{cp}-V_{DD} and V_{cn}-V_{DD} as discussed above. These values can be held by using switches and capacitors as shown in Figure 6.3. A NMOS switch and a capacitor can be used to hold these values, but the drawback of this method is that the bulk of the NMOS should be tied to the source which demands a dual well process.

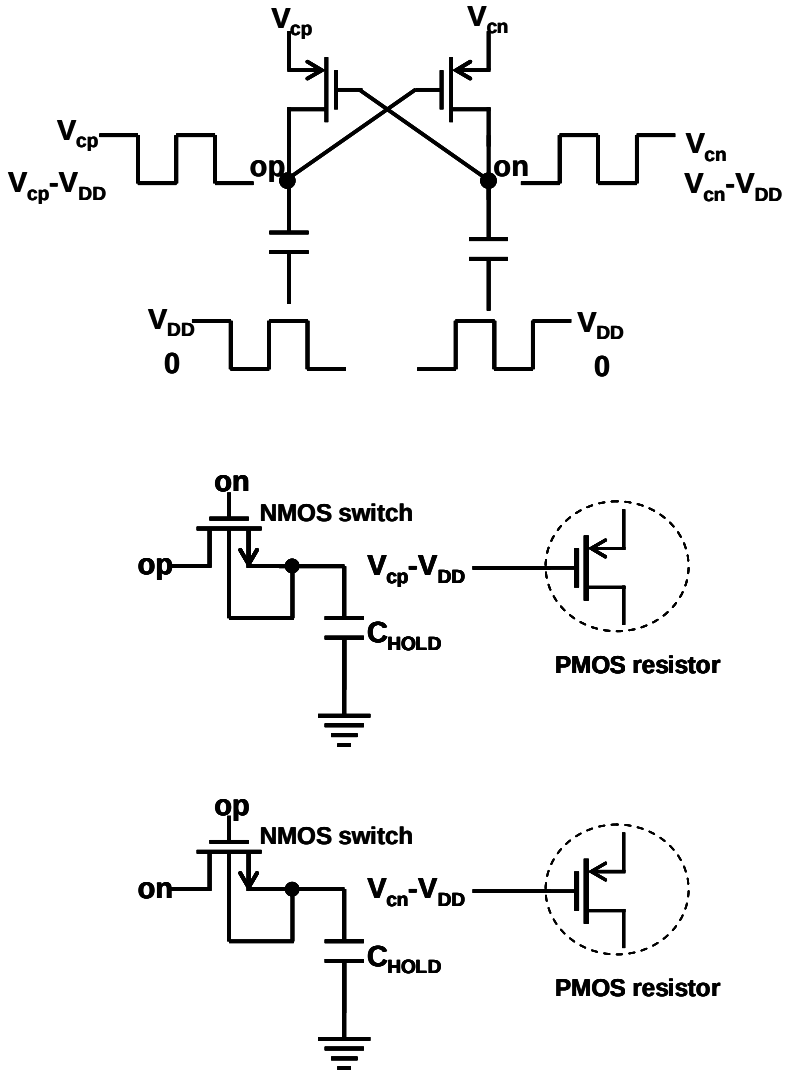


Figure 6.3 PMOS gate voltage generation

An alternate approach is proposed if NMOS resistors are used as tunable elements. The gate voltage for the transistor can be generated to be $V_{CM}+V_{cntrl}$. Bootstrapping can be used to generate this voltage. The conceptual diagram of bootstrapping is shown in Figure 6.4. The implementation of this approach is not very

simple because care should be taken in the circuit such that at no point of time the transistor's terminal to terminal voltage should exceed V_{DD}. The circuit proposed in [20] can be modified (shown in Figure 6.5) slightly to generate the necessary control voltage for the filter.

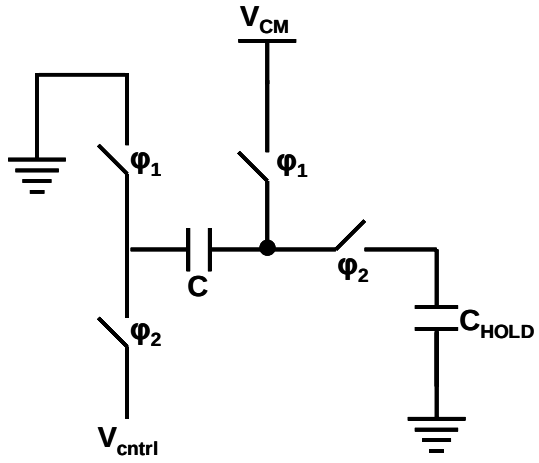


Figure 6.4 Bootstrapping concept

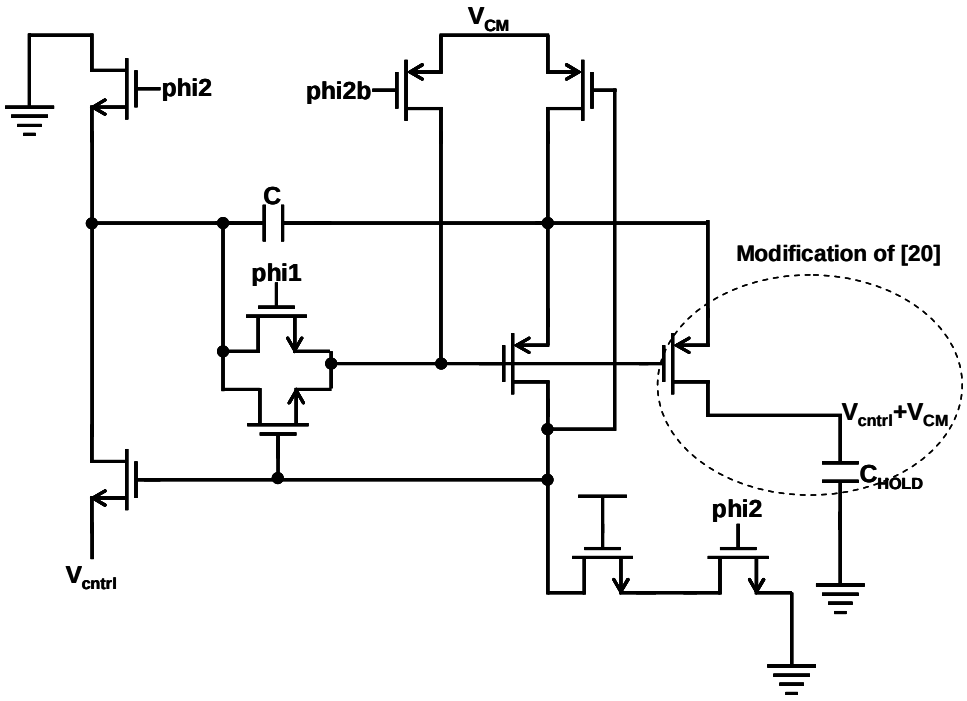


Figure 6.5 Modified version of the implementation proposed in [20]

7. CONCLUSIONS

One of the key challenges in continuous-time filter design is to overcome the time constant variation across process and temperature corners. This thesis describes a method which will tune the filter very accurately in the presence of process, temperature variations and mismatches. Background tuning is performed to overcome the process and temperature variations whereas foreground tuning on power-up is performed in conjunction with background tuning to minimize the mismatches thus tuning the filter very accurately.

Linearity improvements techniques are discussed to improve the linearity of the filter. One of existing techniques has been used in this work to obtain high linearity. Challenges encountered in the design of truly low-voltage filters are discussed and possible solutions are proposed.

A 115 kHz low-pass 2^{nd} order Butterworth filter is implemented in 0.18µ CMOS technology. Measurements indicate a Total Harmonic Distortion of -82 dB for a 10 kHz 250mVpp input signal. Accurate tuning is performed by power-up mismatch minimization technique.

The limitations of the proposed mismatch minimization technique are presented and a few ideas are discussed to improve the performance of the existing scheme. A few issues with measurements are presented.

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