Oscillators and Phase Locked Loops for Space Radiation Environments

by
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My mother and father have offered me a constant, unwavering umbrella of support throughout my life. They have encouraged me to think for myself and chase my dreams. The belief that any goal is attainable with work and commitment was instilled in me at an early age and I am confident I owe most of my success to that belief. I am grateful for the old broken electronics that my father gave me to destroy. The hours spent in the garage trying to figure out how things worked sparked a thirst in my mind that was not easily quenched. I love you both dearly and I truly appreciate everything you've done for me.

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To my dear Kim, I give every moment. I am infinitely lucky to have such a caring and wonderful woman with which to share my time. Your contribution to my life is immeasurable, and can't imagine it without you. I love you over all else and my strongest desire is to grow old and happy with you by my side.

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OSCILLATORS AND PHASE LOCKED LOOPS FOR SPACE RADIATION ENVIRONMENTS

1. INTRODUCTION

Phase locked loops (PLLs) are versatile circuits used for many purposes. Their main feature is the ability to transform a low frequency reference signal to a higher frequency. This makes them appealing for clock generation and radio frequency transceiver circuits. PLLs have been studied extensively and are widely understood [1]-[8]. New variations on the basic charge-pump PLL (CPLL) shown in Figure 1.1 are an area of current research interest.

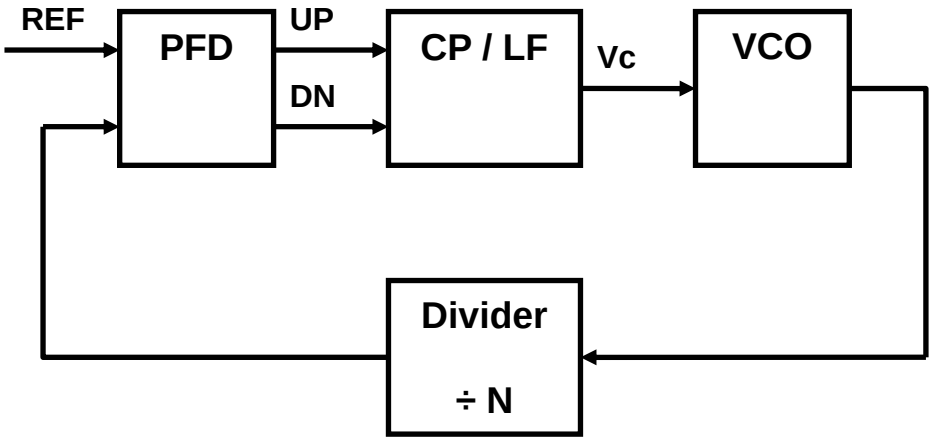

Figure 1.1. Block diagram of a CPLL.

A CPLL works as follows: A reference signal (REF) is fed to a phase-frequency detector (PFD). The PFD compares the reference to its other input and outputs UP or DOWN pulses corresponding to which signal has a higher frequency. The charge pump (CP) interprets the UP and DOWN pulses and switches a current source to either add or remove charge from the loop filter (LF). The loop filter controls the dynamic behavior of the PLL. The output of the LF is the voltage

controlled oscillator (VCO) control voltage. This is fed to the VCO which outputs a signal whose frequency is dependent on the VCO control voltage. The VCO output is optionally fed through a divider which divides the frequency of the signal by an integer N. This divided signal travels back to the second input of the PFD and is compared to the reference signal. When the phase and frequency of the reference and divided signals match, the PLL is said to be locked. The divider allows the output of the VCO to operate exactly N times higher in frequency than the reference, but still track frequency changes in the reference or the VCO.

Cosmic radiation [9] can interact with circuits in mysterious ways. The radiation effect is the interaction of radiation with the silicon crystal of a microelectronic circuit. They can be caused by several types of radiation which in turn can cause several different physical effects in silicon. Two effects are most commonly studied [10, 11]. The single event effect (SEE) is caused by a single energetic particle generating electrons and holes in the silicon which drift to nodes in the circuit. The total ionizing dose (TID) effect occurs when charge becomes trapped in the gate oxide of a transistor changing the characteristics of the transistor. TID radiation is typically quantified by the rad unit of radiation energy absorption. One rad is equal to .01 Joules of energy absorbed per kg of material. The material must be specified for the unit to have meaning. Also note that Si and SiO_2 have different densities and 1 rad(Si) $\neq$ 1 rad(SiO_2). The first report of radiation interfering with circuits was in 1975 when a communications satellite detected 4 upsets (memory bits in error) over the course of 17 years [12, 13]. As technology dimensions scales to ever smaller values, the radiation problem has worsened. Now satellite electronics are always given thorough attention to the effect of radiation on the circuit. Research has been successful in determining the causes and several solutions to the radiation effect in digital circuits. Analog electronics, however, play a much smaller role in a satellite's electronic system and, therefore, have been somewhat neglected by the radiation electronics community.

The primary goal of this research was to explore new ways of mitigating radiation effects in PLL circuitry. A silicon on insulator (SOI) process seems especially suitable to this application. In an SOI process, the transistors are formed on a layer of silicon dioxide (SiO_2) instead of a thick layer of semiconducting bulk silicon. Thus, if an energetic ion were to strike an SOI transistor, only the electron-hole pairs above the SiO_2 would drift to nodes in the circuit. This could be an order of magnitude less that the charge collected in a traditional process [14]. Designing and characterizing a PLL in an SOI process became the first goal of the research. The design of the test chip is detailed in Chapter 2. The test setup and results are presented in Chapter 3. Chapter 4 presents the design of a digitally controlled VCO and Chapter 5 concludes the work.

2. TEST STRUCTURE DESIGN

Fourteen oscillators and two complete PLLs were designed for this project. Eight of the oscillators were ring type and six were LC oscillators. One of the PLLs used a ring oscillator and the other used an LC oscillator. The test structures were designed in the Honeywell MOI-5 process. This is an SOI process with a minimum gate length of 0.35 microns. The LC oscillators on the test chip were designed by the author and design details will be presented in this chapter. The other structures were designed by other members of the research team and their design will not be discussed here.

2.1. LC Oscillator Design

LC voltage controlled oscillators (VCOs) use a cross-coupled pair of transistors to provide a negative resistance to an RLC tank. The cross-coupled pair cancels out the resistance of the parasitic elements in the tank and provides enough loop gain to excite and sustain oscillations. A varactor is used to vary the resonant frequency of the LC tank. It has been shown that a complimentary design using both PMOS and NMOS cross coupled pairs results in better phase noise performance for a given bias current [15]. To reduce and control the current draw of a complimentary LC oscillator, a current source is usually used. Most commonly this current source is implemented as either a PMOS or NMOS current mirror. Schematics for complimentary oscillators with an NMOS and PMOS current source are shown in Figure 2.1.

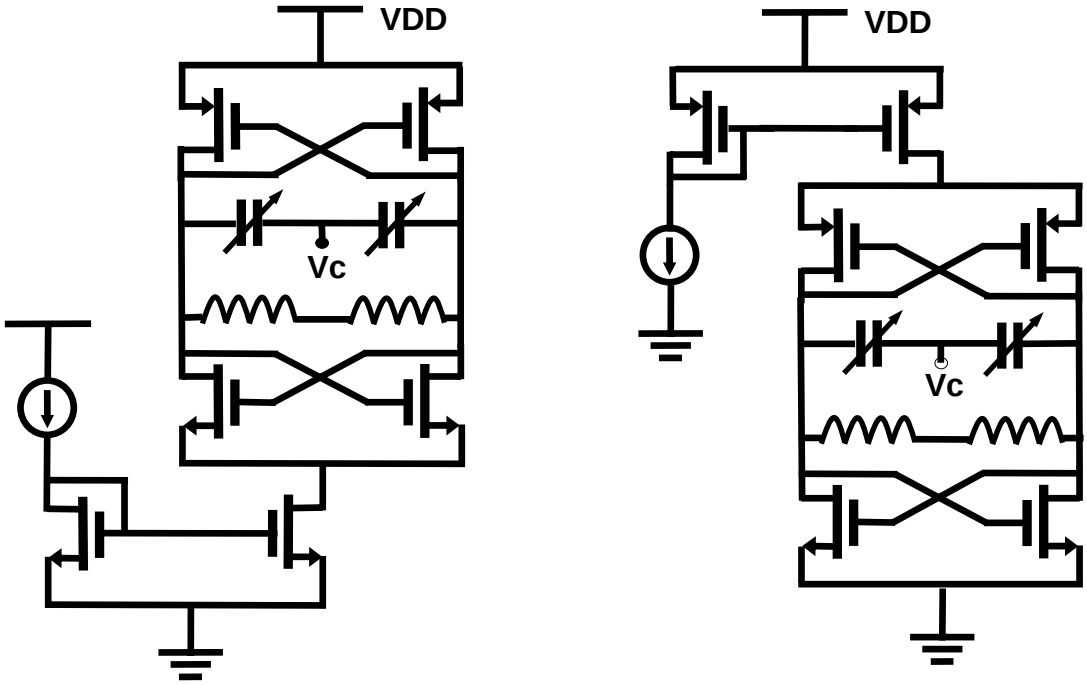

Figure 2.1. LC VCOs with NMOS and PMOS current sources.

2.1.1. Figure Of Merit

A figure of merit (FOM) is used to compare oscillator performance. The figure of merit used is a measure of three of the most important specifications of electrical oscillators: the operating frequency, the phase noise at a particular offset frequency, and the power consumption. It is calculated according to the following equation [16]:

$$FOM = 20\log(f_0) - L(1MHz) - 10\log(P_D)$$

where f_0 is the oscillation frequency, $L(1MHz)$ is the single-sideband phase noise in dBc/Hz at 1MHz from the carrier and P_D is the power dissipation.

2.1.2. Power Supply Noise Rejection

In addition to radiation resistance, the ability of oscillators to maintain low jitter performance in the presence of power supply noise was also a design goal. The two configurations of Figure 2.1 have roughly similar phase noise performance with the PMOS current source oscillator being slightly better due to its smaller flicker noise contribution. The rejection of power supply noise is quite different however [17]. The current mirror greatly attenuates the noise that is injected through it making the NMOS source effective at rejecting ground noise and the PMOS source effective at rejecting VDD noise. Simulation results for the two cases are shown in Figures 2.2 and 2.3.

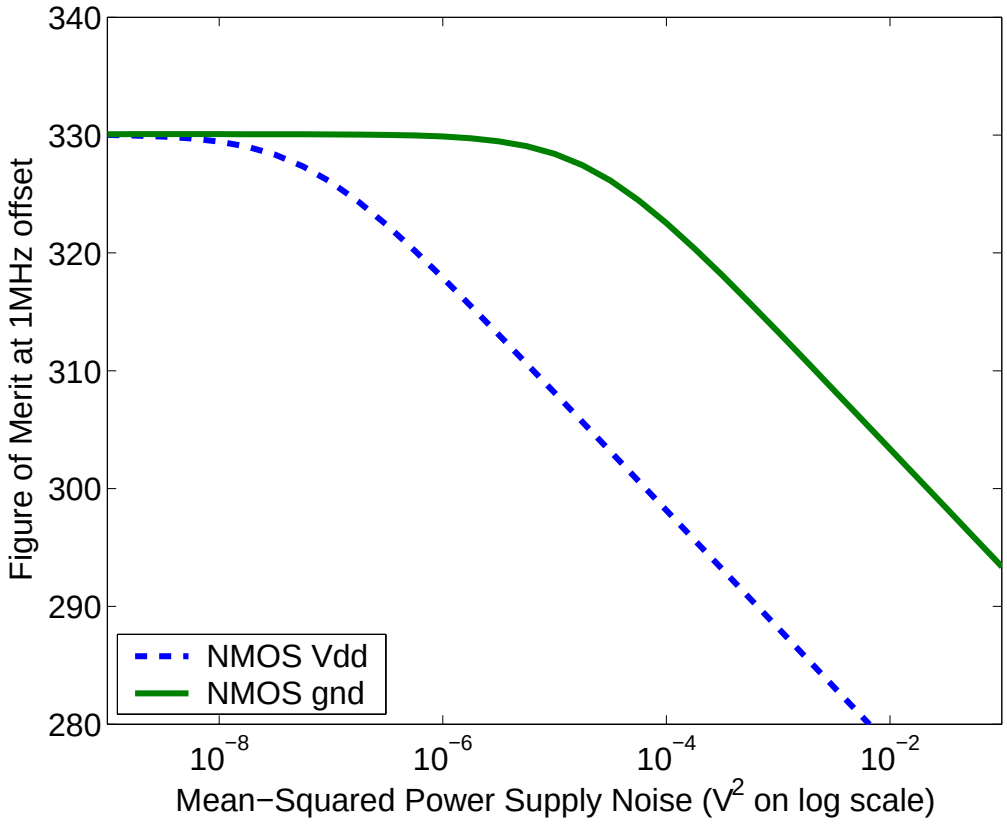

Figure 2.2. NMOS source oscillator injected with GND and V_{DD} noise.

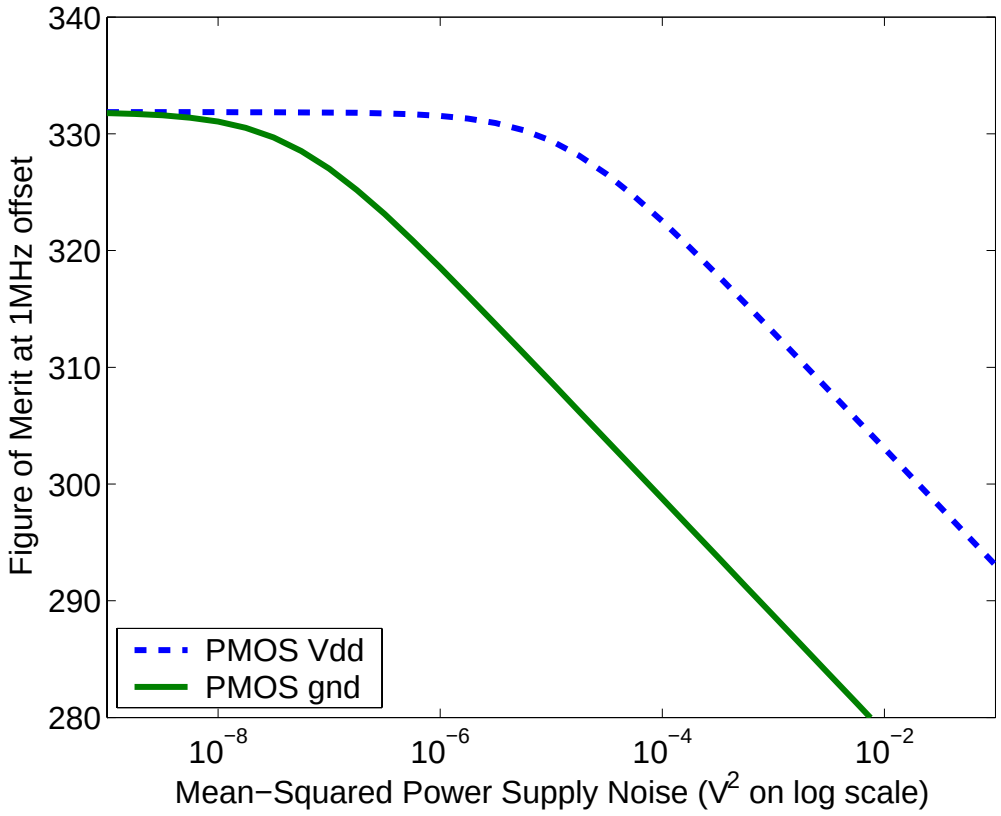

Figure 2.3. PMOS source oscillator injected with GND and V_{DD} noise.

Based on the above analysis, we have pursued a dual current source structure that has not yet appeared in literature. The initial finding was that a complimentary oscillator with both PMOS and NMOS current sources would show good performance in the presence of both ground and V_{DD} noise. This is a likely situation in many mixed-signal applications. A schematic of the dual current source structure is shown in Figure 2.4. The supply noise rejection simulations for the new structure are shown in Figure 2.5. The simulations confirm our intuition that the new dual current source structure can tolerate injected noise from both V_{DD} and ground while the single current source structures can tolerate only one source of noise. An added benefit of this structure is that the common mode voltage of the oscillator can be controlled by mismatching the NMOS and PMOS current mirrors.

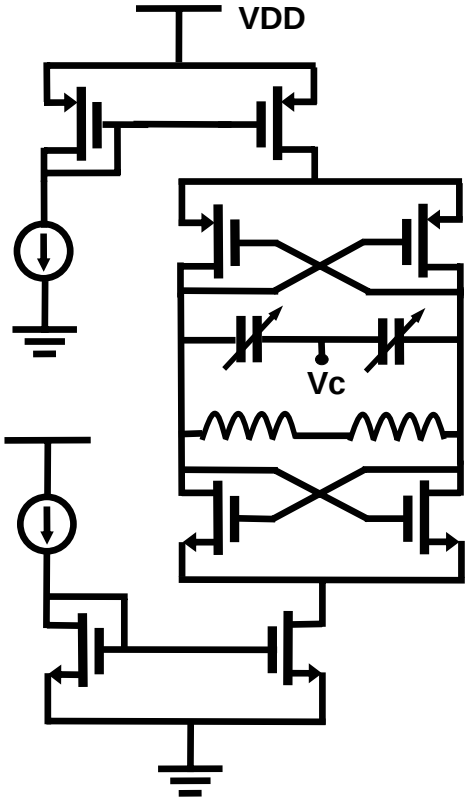

Figure 2.4. Schematic of the dual current source structure.

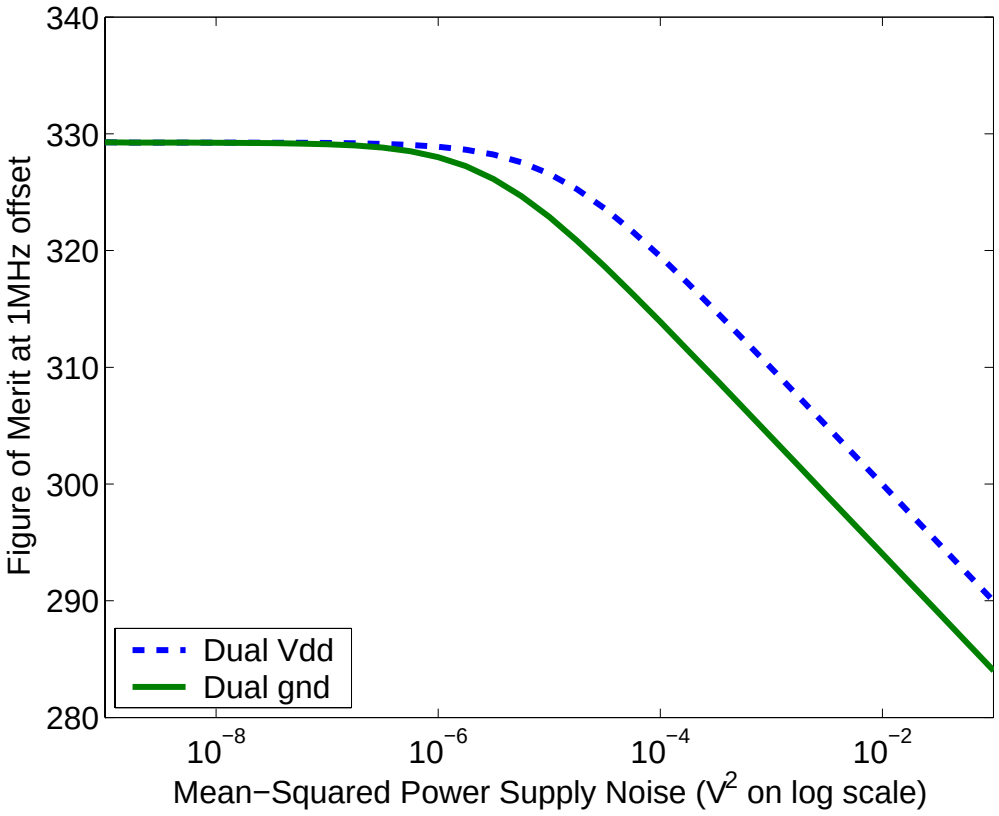

Figure 2.5. Dual current source oscillator injected with GND and V_{DD} noise.

2.1.3. Effect of Body Ties

The Honeywell process that was used has body ties built into the MOS devices. The differences between oscillators with and without body ties was also evaluated. Transistors without body ties are not supported by the simulation models available in the Honeywell design kit, so simulations on these devices would not be accurate. In simulation, removing the body ties has little effect on either the phase noise or the power supply rejection. Therefore, each of the fabricated oscillators has a body tied version and a floating body version for comparison.

2.1.4. Bias Point

The oscillators were designed to operate with a 3mA nominal current. This puts them near the transition between the voltage and current limited regime. Phase noise in LC oscillators is inversely proportional to the voltage swing of the tank [18]. Thus it is beneficial to maximize the voltage swing of the output. For low currents the output voltage swing can be approximated by the formula [15]:

$$V_{\text{tank}} \approx I_{\text{tail}} R_{\text{eq}}$$

Thus, to maximize the phase noise performance, we should maximize the tail current. The tank voltage cannot increase indefinitely, of course, and as the output voltage approaches the power supply limits, the devices enter the triode region [19]. This limits the voltage swing to slightly less than the operating voltage; 3.3V in our case. Since increasing the current through the oscillator directly increases the power consumption, it is not advisable to set it arbitrarily large as this decreases the FOM.

With the FOM in mind we can easily find the optimal bias point which balances phase noise improvement with power consumption. The bias current is swept for all three oscillator structures and the FOM of each is calculated in Figure 2.6. The dual current source design has a slightly worse performance than either of the single source configurations due to the added noise of the extra transistors and the reduction in output swing from having four transistors in the stack instead of three. The oscillators are optimized such that the noise from the transistors is largely dominated by the noise from the inductor, so the reduction in FOM is not as dramatic.

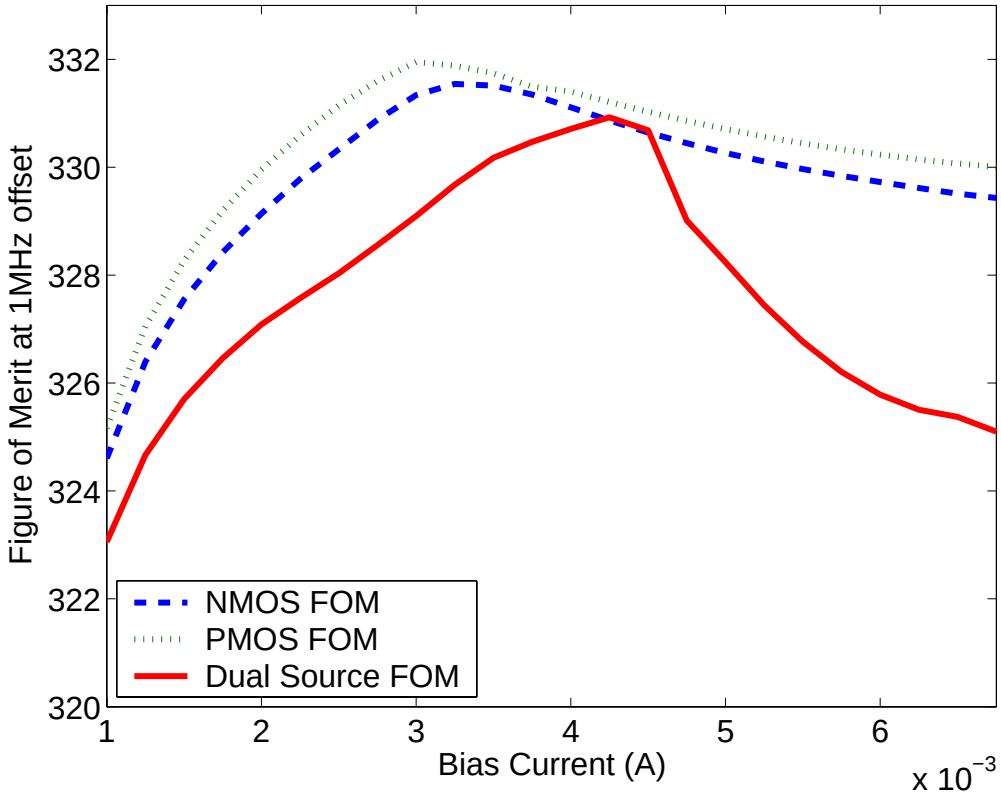

Figure 2.6. Sweeping bias current shows an optimal value at 3-4mA.

2.1.5. Layout

Careful consideration was taken in the layout of the oscillators to maintain as much symmetry as possible between the differential parts of the circuit. The parasitic resistance in the tank can greatly degrade the quality factor of the tank which is detrimental to the noise performance. Thus metal traces are designed to minimize the resistance even with the relatively high currents involved.

2.1.6. Test Cases

To simultaneously verify the noise rejection and the effect of body ties, several test LC oscillators were fabricated in the Honeywell MOI5 process. These were the three different biasing schemes each with and without body ties for a total of 6 structures.

2.2. Other Test Structures

In addition to the LC oscillators, four different versions of the Lee/Kim and Maneatis oscillators that were designed and analyzed in [20], [21] were included on the test chip. These include the Lee/Kim oscillator with two different layout geometries, the Maneatis oscillator with transistors providing a symmetric load, and the Maneatis oscillator with a linear load as described in [20]. The two Lee/Kim geometries enable comparison of the traditional layout with asymmetric signal lines on delay cells to a new layout that matches signal delays at the expense of asymmetric power supply connections. [21] provides a detailed description of these ring oscillators. The testing and results of all the structures on the test chip will be discussed in Chapter 3.

2.3. Test Chip

In total, the test chip included two complete PLLs, 14 VCOs and a number of other test structures. The total chip area was roughly 5mm by 5mm. The test chip was packaged in a 121 pin ceramic pin grid array (PGA) package. The package has a taped on lid which can be removed to expose the bare die. Figure 2.7 shows a die photo of the test chip with the PLLs and VCOs highlighted.

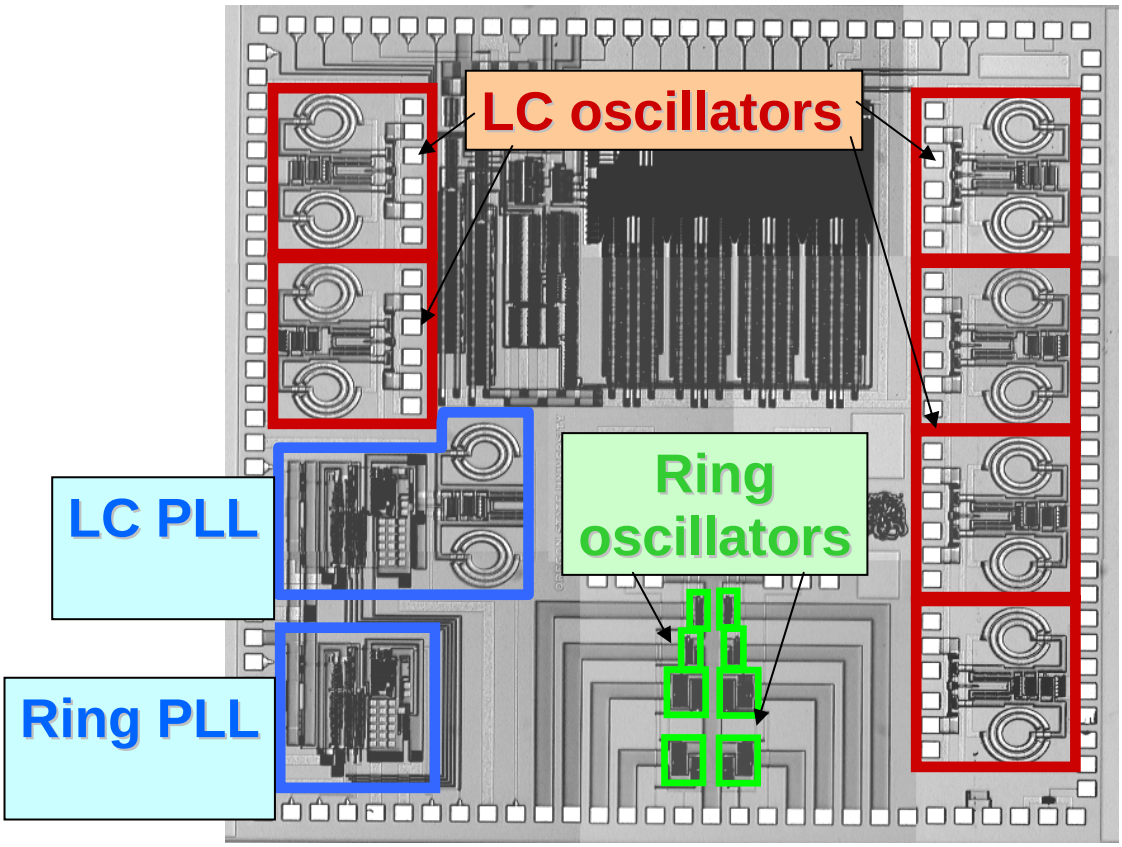

Figure 2.7. Die photo of first test chip.

3. RADIATION TESTING

The first test shuttle was exposed to total dose radiation at the Kirtland Air Force Base in Albuquerque, New Mexico. Two tests were done. The first used a single 500krad (SiO_2) dose and measured all the oscillator test structures on the chip. The second exposed the chip to several doses and measured only the performance of the ring PLL. The LC PLL was unable to achieve lock. The Low Energy X-Ray (LEXR) source at AFRL provided the X-ray radiation for both tests. The measurements for the first test were done at OSU. The measurements for the ring PLL test were done on site at AFRL. The last data point of that test was taken after a delay at OSU to estimate the annealing effect in the Honeywell MOI5 process.

3.1. Test Setup

The radiation exposure was provided by the LEXR source inside a room with lead walls. The packaged chip was mounted on a circuit board which in turn was mounted in an aluminum box for mechanical stability and accurate positioning with reference to the LEXR source. This is critical for accurate dosimetry of the LEXR source.

The test board is designed to provide an interface for the input and output signals and also to provide bias to the test PLLs. The board was positioned such that only the active die was exposed to the radiation. The only active component on the test board is a voltage regulator which sets the DC value of the VDD bus to 3.3V. The VDD bus is routed to all the different test structures and each is switchable with a jumper. This allows us to monitor the current consumption of the PLL's and to only power up the structures of interest for the current test. The signal inputs and outputs are via SMA connectors. The inputs and outputs were connected through 50-ohm connections to a digital storage oscilloscope. The cables were kept as short as

possible, but they must pass through the walls of the LEXR chamber to reach the test equipment outside. Figure 3.1 shows a picture of the LEXR source in the test chamber. Attached is a cryo chamber which was not used in our test.

Figure 3.1. LEXR source in test chamber.

The lid of the ceramic chip package was removed during the test to expose the bare silicon die. This was to ensure that the X-ray radiation had an unimpeded path to the die.

3.2. Results

3.2.1. Single shot

The first test was a single 500krad (SiO_2) at 100 rad/sec dose to all the oscillator test structures on the chip. Each oscillator's tuning range was measured before and after radiation. The 500krad had a small effect in some of the oscillators. It did not prevent any of the circuits from functioning. The most notable effect was the shift in the control voltage of the ring oscillators. The ring oscillators ran roughly

100MHz slower for a given control voltage after the radiation. The LC oscillators with no body ties also suffered from a shift, but in the opposite direction and on the order of a few tens of MHz. The tuning range was also compared to simulation data. Figures 3.2-7 show the tuning range of the VCOs.

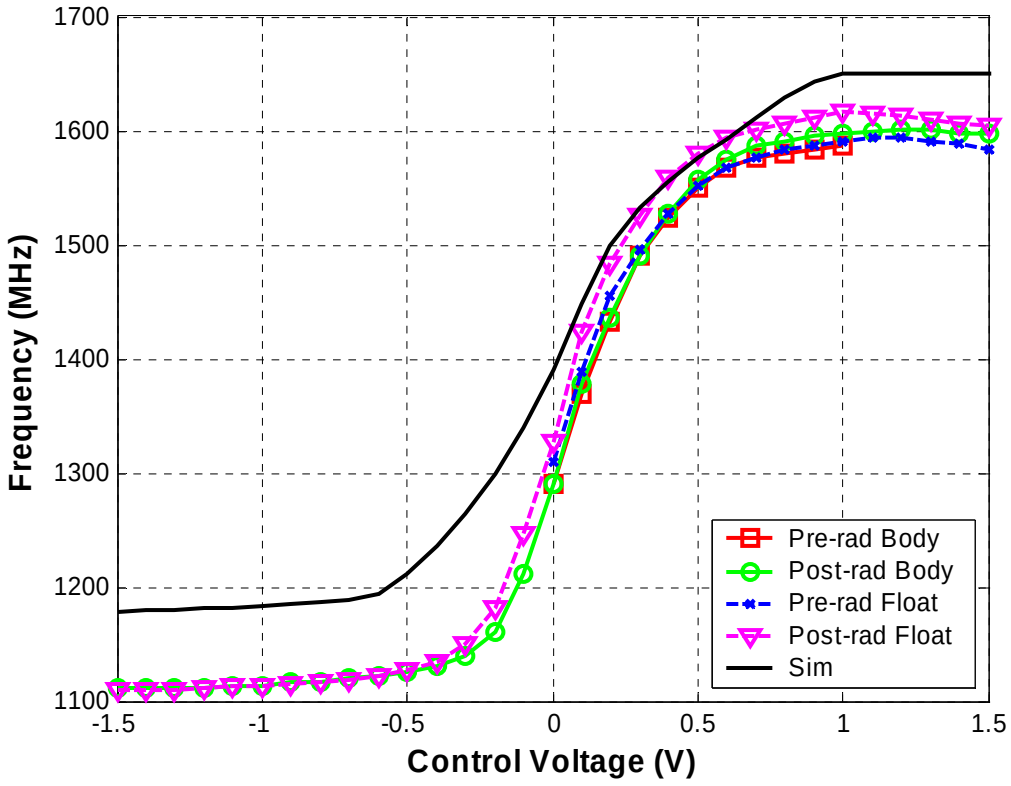

Figure 3.2. Tuning curve for PMOS source LC VCO.

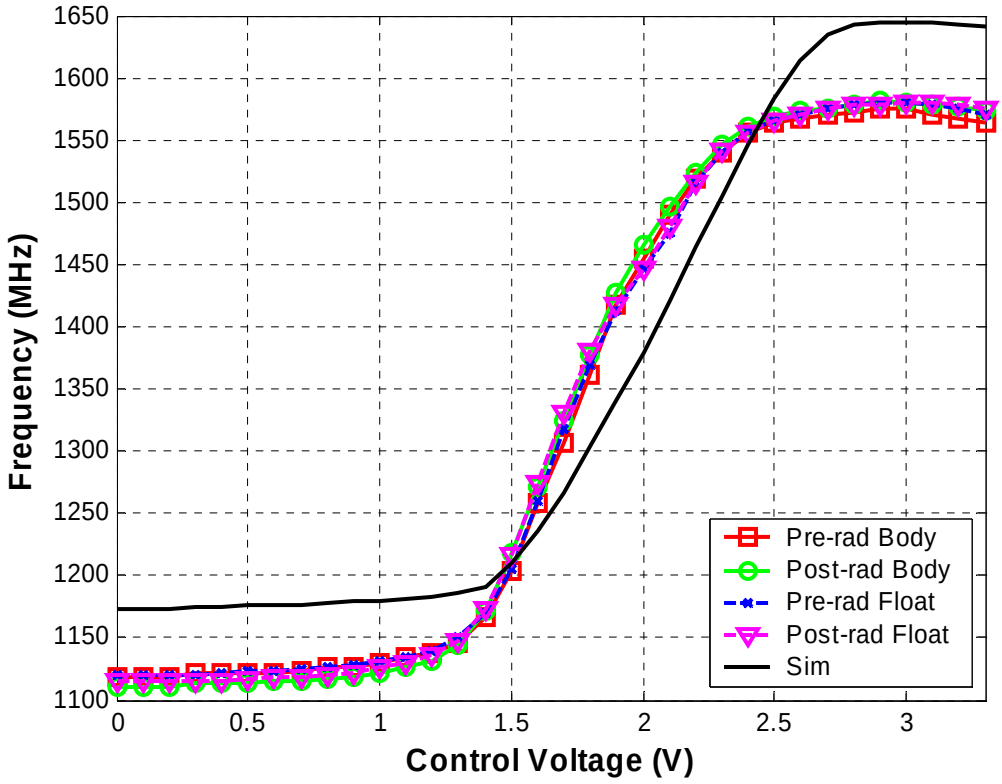

Figure 3.3. Tuning curve for NMOS source LC VCO.

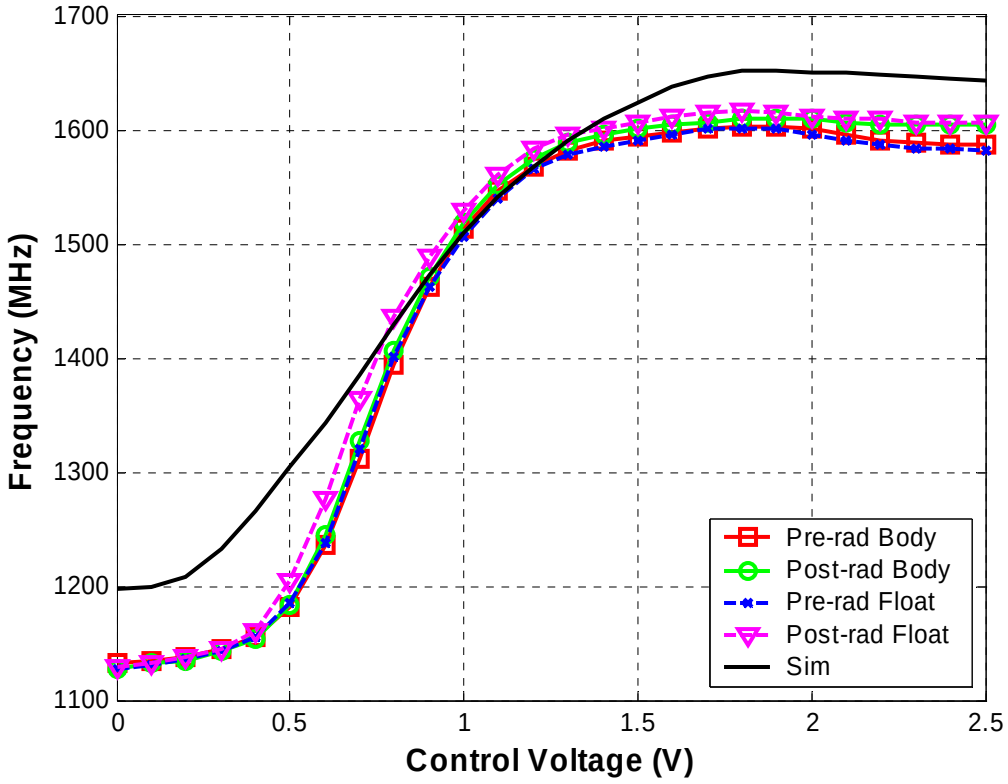

Figure 3.4. Tuning curve for complimentary source LC VCO.

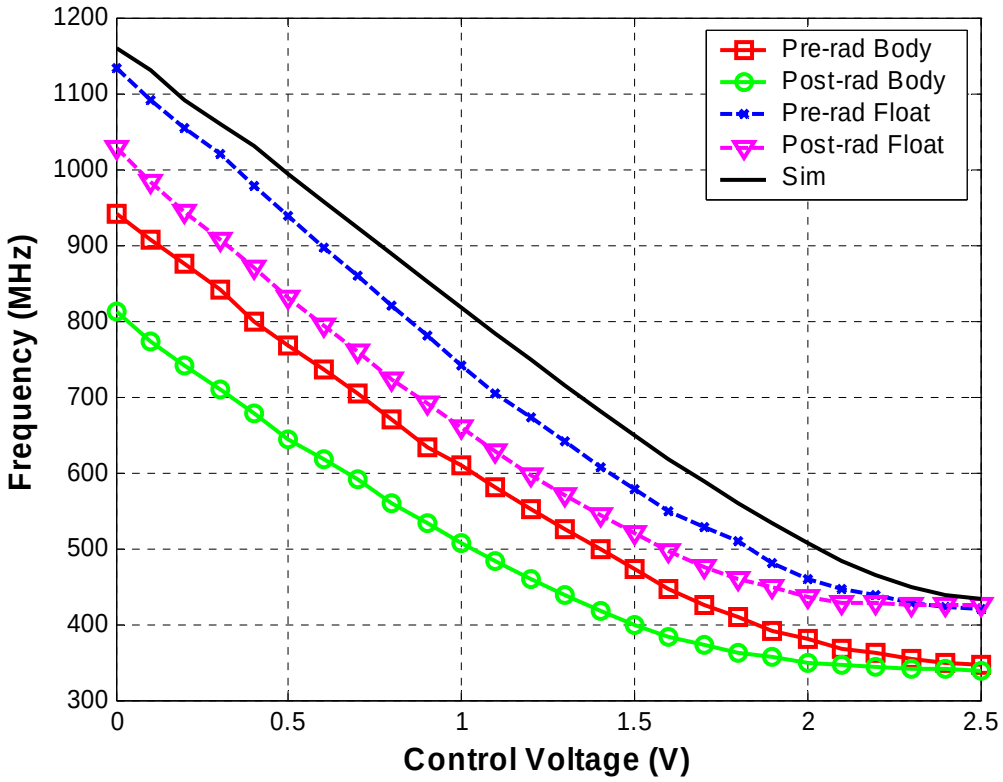

Figure 3.5. Tuning curve for Lee/Kim traditional layout VCO.

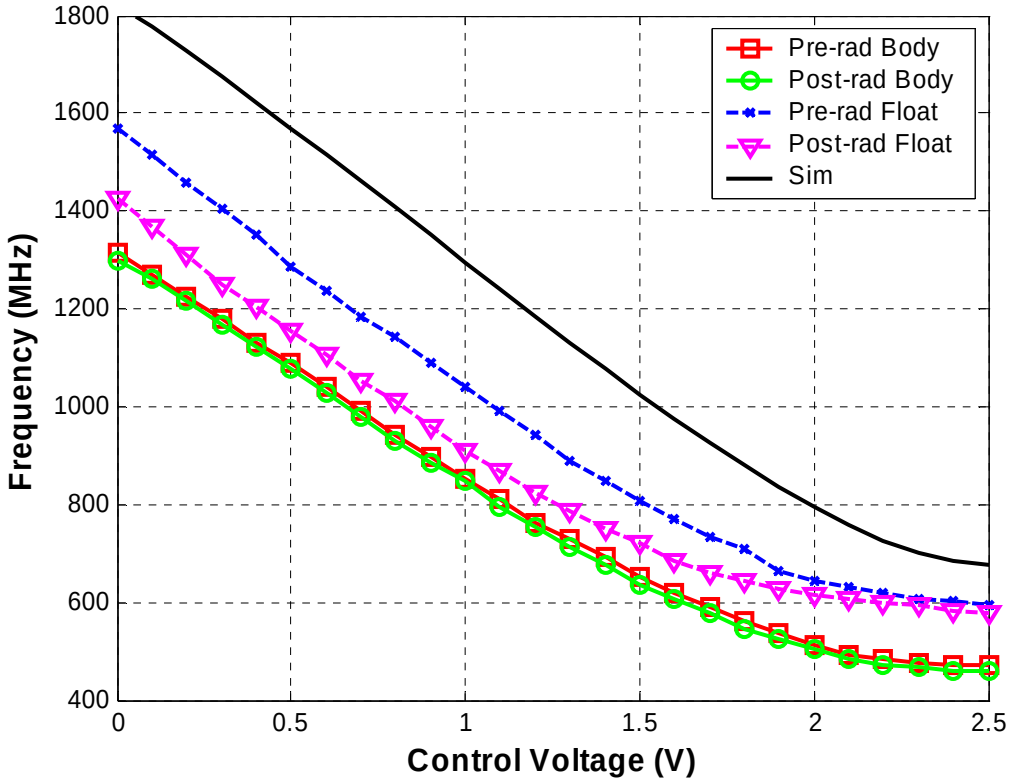

Figure 3.6. Tuning curve for Lee/Kim optimized layout VCO.

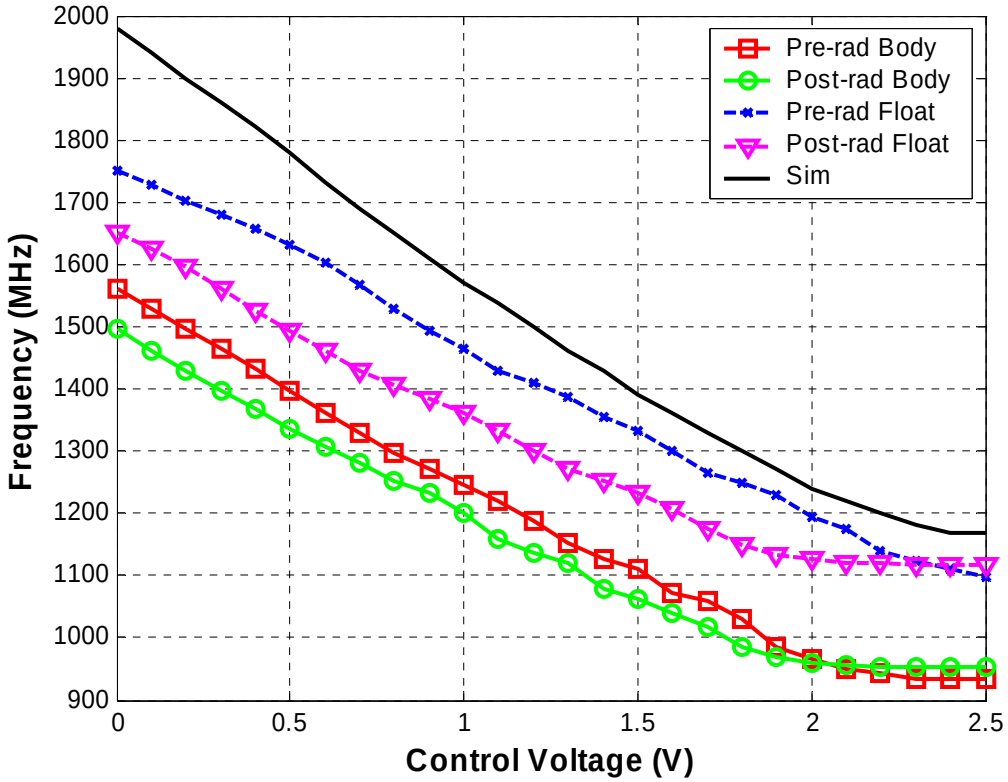

Figure 3.7. Tuning curve for linear-load Maneatis VCO.

3.2.2. PLL Test

The ring PLL was tested for functionality at total dose radiation levels up to 6.2Mrad (SiO_2). The lock range was measured at 9 radiation levels and once again 35 days later with no additional radiation exposure. This final test was done to determine if annealing was contributing significantly to the measurements. Figure 3.8 shows the power consumption of the PLL as a function of the radiation dose. The measurement was taken at a reference frequency of 45MHz. After an annealing delay of 35 days, there is little change in the power consumption suggesting that the annealing effect is small.

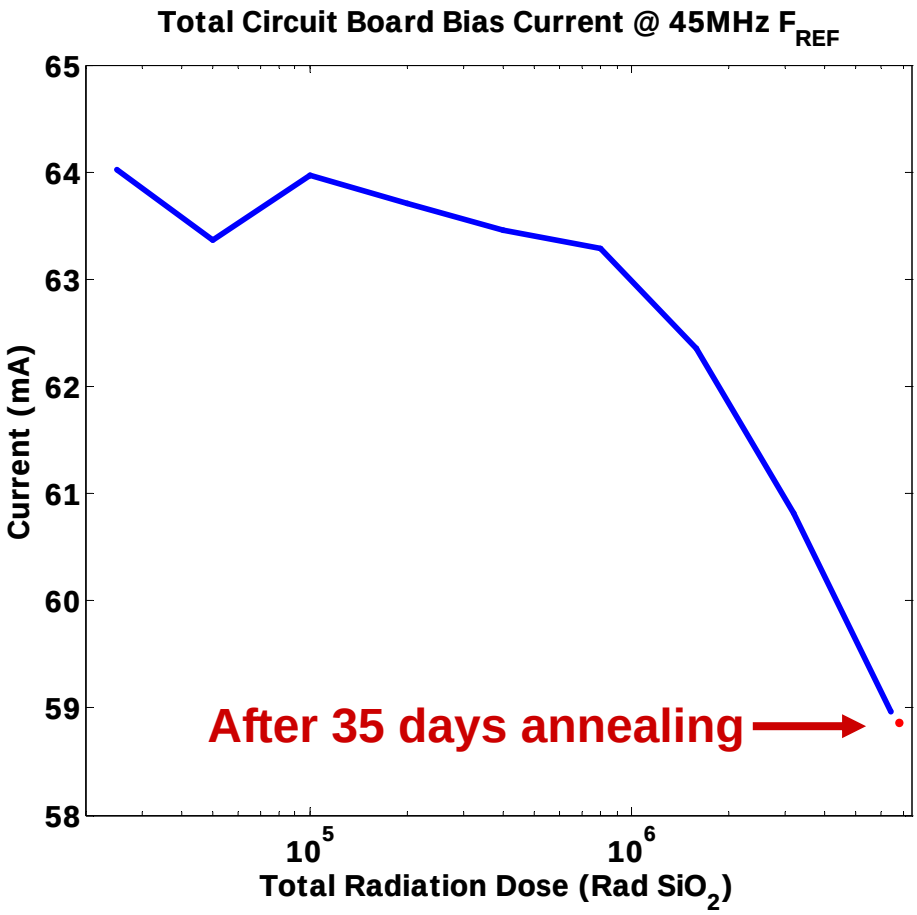

Figure 3.8. Power consumption of the PLL versus radiation exposure.

A plot of the lock range as a function of the total radiation dose is shown in Figure 3.9. The PLL was able to achieve lock even after the highest dose. The lock range was shifted somewhat from the radiation as can be seen in the plot. This effect would not prevent the PLL from operating properly. Again the final test was redone after 35 days to see the annealing effect.

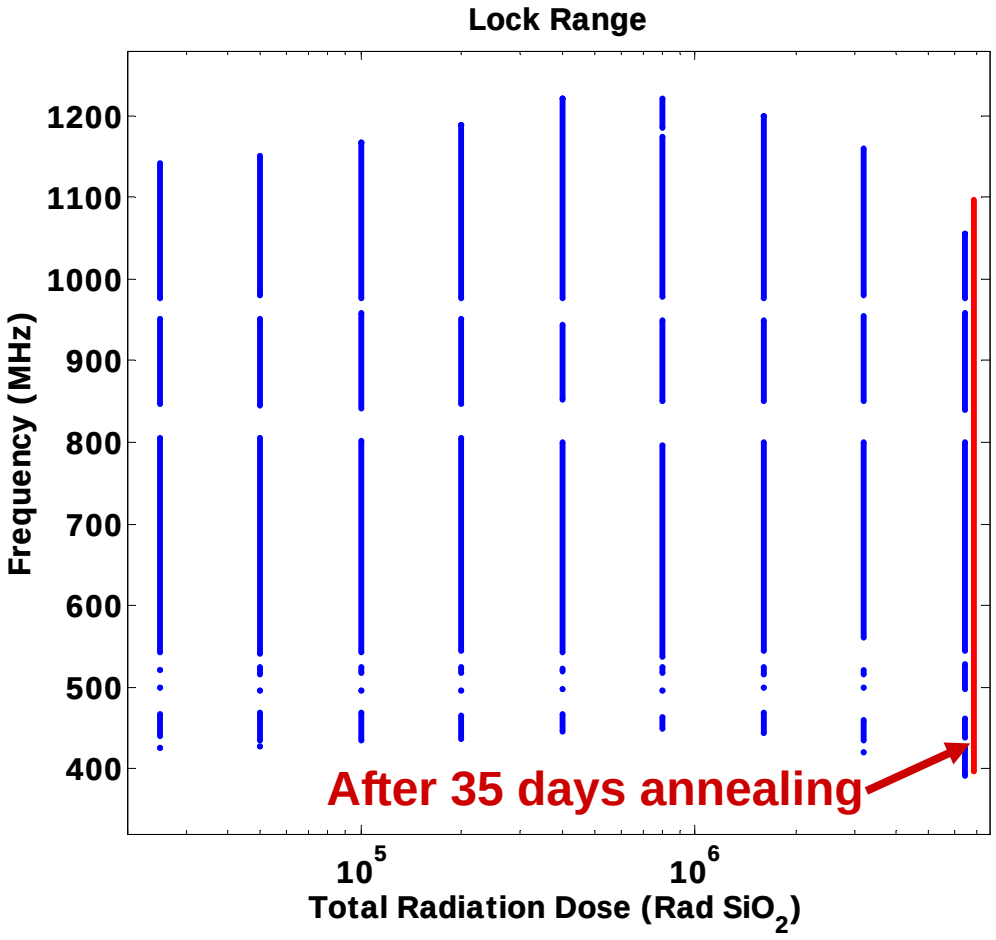

Figure 3.9. Lock range of the PLL versus radiation exposure.

There was a problem with the test setup at the AFRL that was preventing the PLL from achieving lock at some frequencies in the lock range. This is shown in the plot by the gaps in the lock range lines. We observed a large feedthrough of the oscillator output on the divided output. This was contributing to the problems achieving lock. The buffer for the VCO draws high currents from the power supply at a high speed. Using an improved test setup at OSU for the anneal test, the PLL was able to achieve lock throughout the lock range as expected.

When the test chip was designed, no on-chip bypass capacitors were used. This was done to have the ability of injecting power supply noise without the noise being filtered. We anticipated that the intrinsic capacitance of the metal traces and bondpads would be sufficient to keep the ripple off the supply lines. Silicon-on-Insulator processes, however, have much smaller parasitic capacitances than bulk processes because the metal layers are separated from the bulk by an insulator. The absence of bypass capacitors on the chip caused considerable power supply noise to exist. Although this did not prevent any of the blocks from functioning, it caused the performance of the blocks to deteriorate.

Simulations have been performed to estimate the effect of the package inductance with and without on-chip filter capacitors. A 4nH inductor was placed in series with the power supply of one of the Lee/Kim oscillators to model the bondwire. More complex bondwire and package models were simulated and the single inductor produced the most significant effect regardless of the rest of the model. Simulations were performed to examine the effect of on-chip capacitance on supply ripple. Figure 3.10 shows a schematic of the simulation setup. Simulation results for several values of on-chip capacitance are plotted in Figure 3.11. We can see that supply noise can be a big problem unless we have 10pF or more of on-chip decoupling. The second test chip benefits from this analysis.

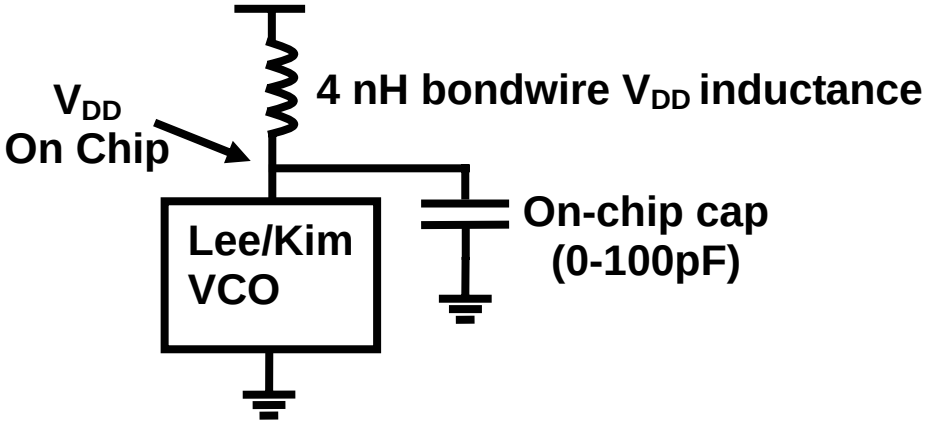

Figure 3.10. Schematic of power supply ripple simulation setup.

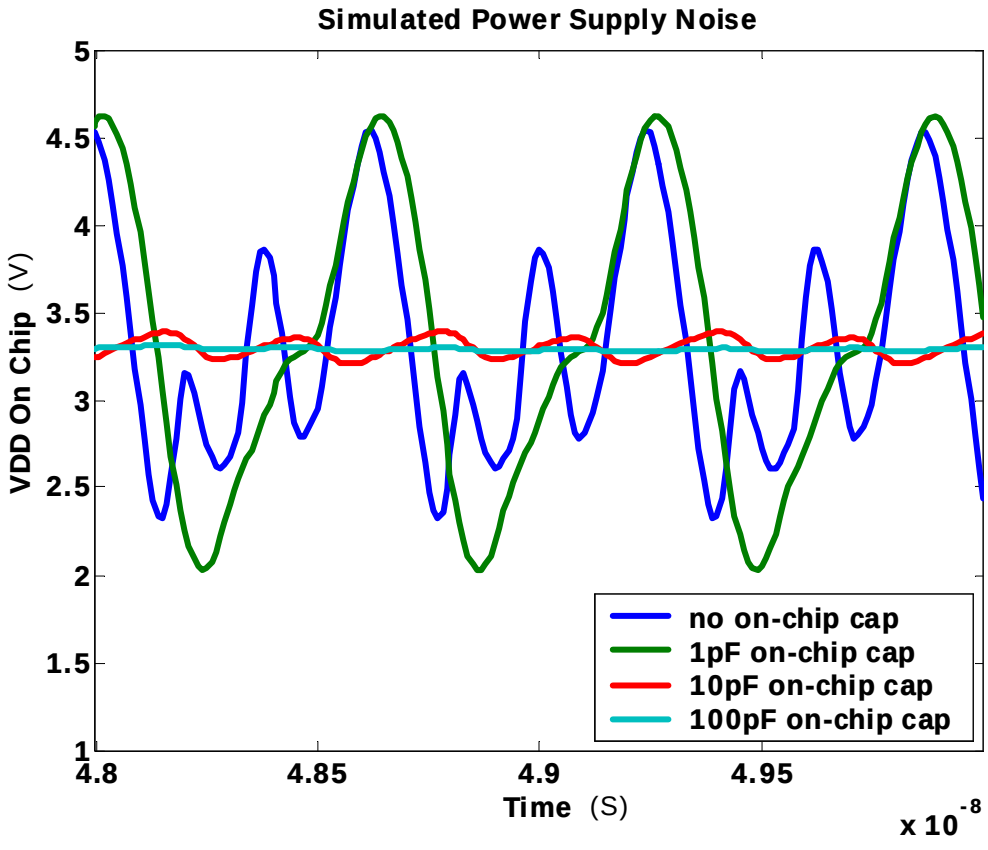

Figure 3.11. Simulation results for power supply ripple.

4. DIGITALLY CONTROLLED ANALOG OSCILLATOR

Digital PLLs (DPLLs) may provide increased resistance to space radiation [22], [23]. A digitally controlled analog oscillator (DCAO) is a key component of a DPLL. It is similar to a traditional voltage controlled oscillator except that the input is a digital word instead of an analog voltage.

4.1. DCAO Design

The DCAO is implemented as a three stage differential ring oscillator. The key specification for this design was frequency resolution. For high performance, the digital PLL needs the DCAO to produce frequencies with as many bits as possible. The differential delay elements are Lee/Kim type with dual control inputs, which allow for fine and coarse tuning. The schematic of the delay element is shown in Figure 4.1. Two banks of current mirrors allow digital control of the fine and coarse tuning voltages. The tuning circuits convert the two 6-bit words into the analog V_{COARSE} and V_{FINE} voltages. The schematic of the fine tuning circuit is shown in Figure 4.2. The coarse tuning circuit is identical. The operation is as follows: The digital input, DF[0-N], determines which current sources are drawing current from PM1. This sets the voltage at V_{FINE} and controls the speed of the oscillator. Figure 4.3 shows a single fine tuning curve for the DCAO. The resistor R1 determines the unit value of current to be mirrored on the right half of the circuit. This resistor is off-chip to allow control of the trade-off between gain, resolution and tuning range. Figure 4.4 shows the tuning curves using two different resistor values. The configuration of the blue curve has a high gain and high tuning range, but low frequency resolution and a large overlap between adjacent coarse tuning ranges. The configuration of the green curve has better resolution and a smaller overlap, but sacrifices tuning range to achieve this. The resistors can be varied during testing to find the optimal operating point.

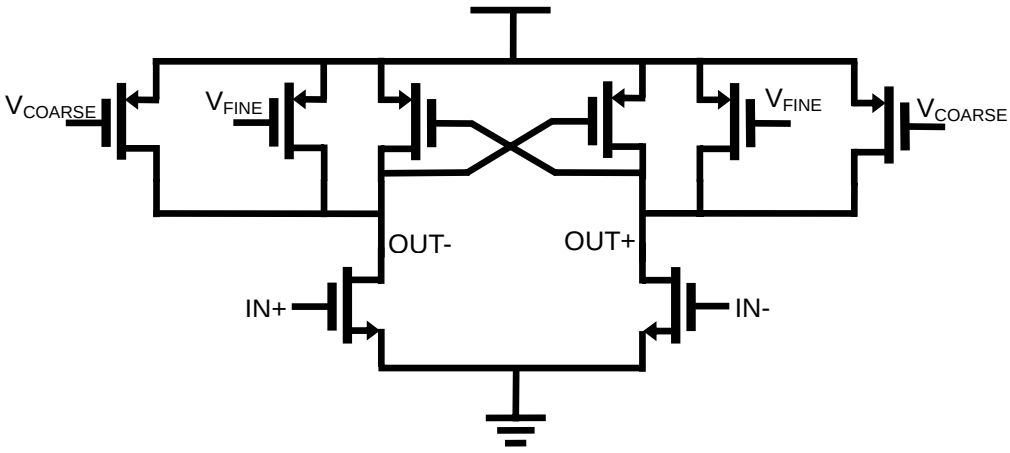

Figure 4.1. Lee/Kim differential delay cell with dual tuning inputs.

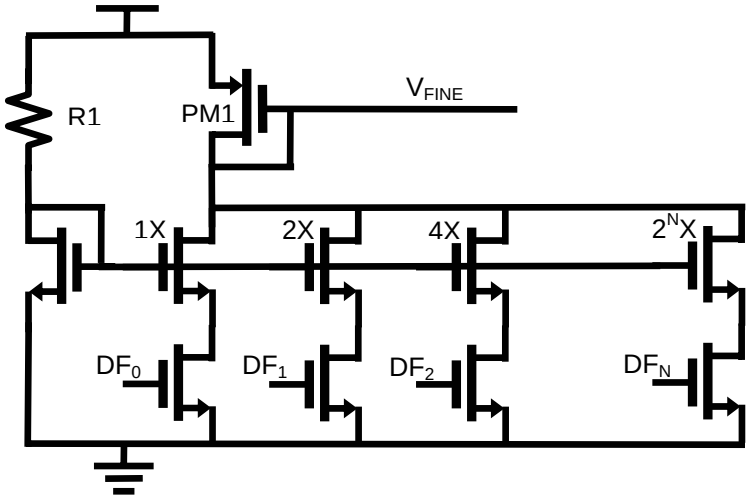

Figure 4.2. Fine tuning control circuit.

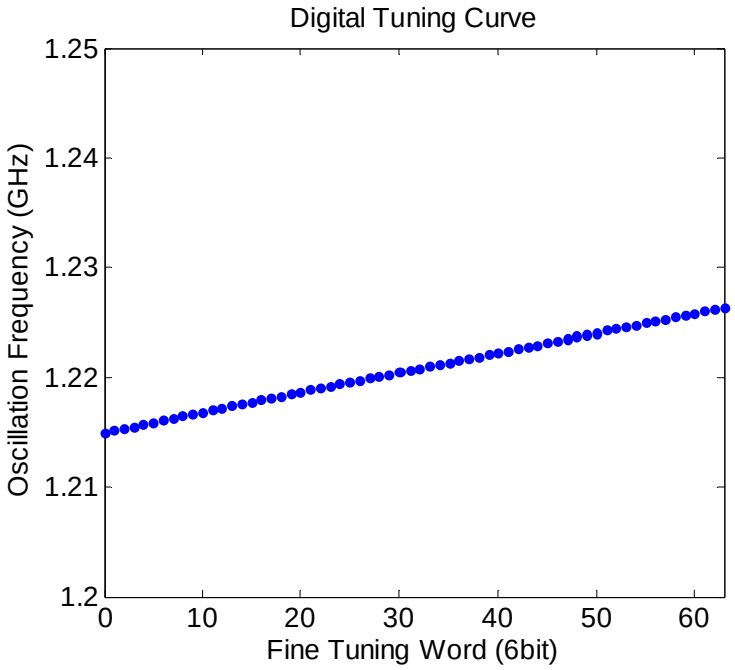

Figure 4.3. Single fine tuning range.

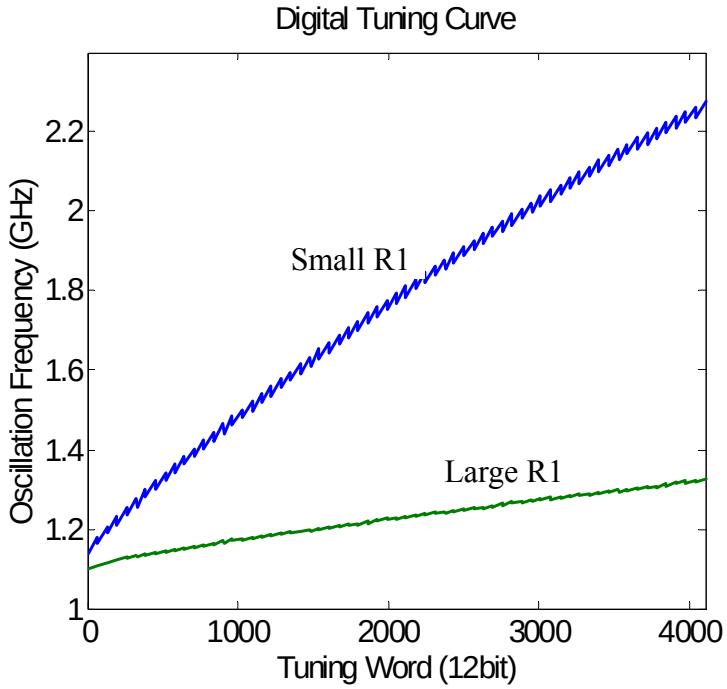

Figure 4.4. Tuning range control with off-chip resistors.

4.2. DCAO Layout

As with the LC VCO layout, the DCAO layout is critical to the performance of the oscillator. Parasitic capacitance on the switching path is critical in determining the speed of oscillation so great care is taken to minimize the size and length of interconnects between stages. The layout should be kept as symmetric as possible to match loading and delays. Dummy paths can be used to match both differential signal paths. Multiple vias and wide traces can lower parasitic resistance. Decoupling caps near the circuit can help prevent spurious tones from entering the oscillator through the power supply. The core of the DCAO measures only 125µm by 40µm. A image of the layout is shown in Figure 4.5. The chip was sent for fabrication.

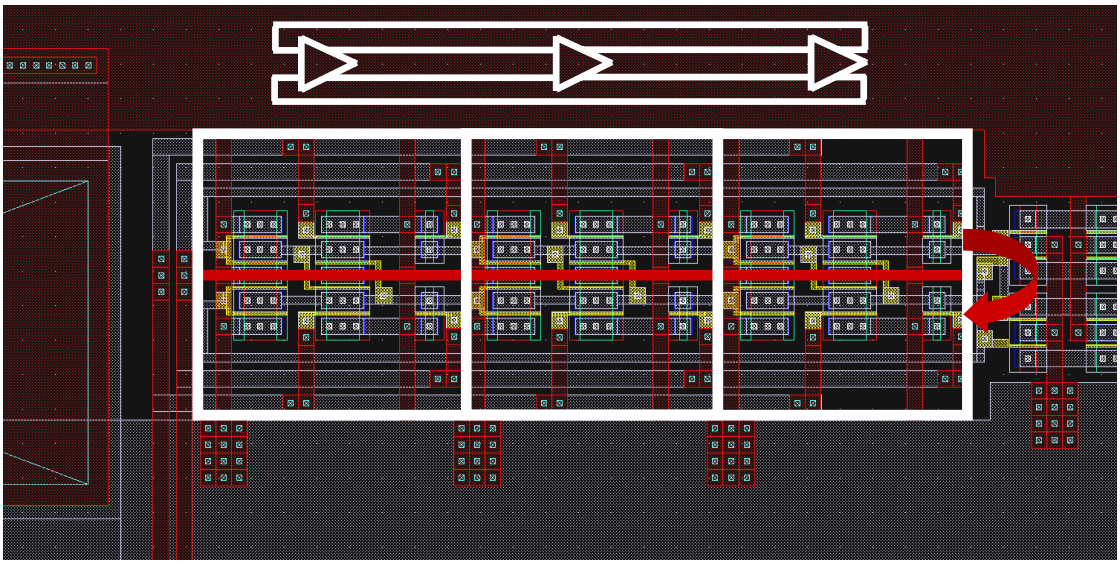

Figure 4.5. Layout of the DCAO core.

5. CONCLUSION

This thesis gave details on the design and testing of phase locked loops for applications which will encounter radiation. A test chip was designed and fabricated in a 0.35µm SOI CMOS process. The test chip included two PLLs, 8 ring VCOs, 6 LC VCOs, and a number of other test structures. The design of the LC VCOs was detailed in this thesis and the test results of all the structures were also described. The tuning range of the VCOs was shifted due to the total dose radiation. The ring VCOs saw a much greater shift than the LC VCOs. The ring PLLs tuning range was also shifted from the radiation. It was able to achieve lock even after the highest dose of 6.2Mrad. The LC PLL was unable to lock in all the tests.

As space exploration and development matures, electronic systems of increasing complexity are required to power and control spacecraft. In addition, as silicon transistors scale to smaller and smaller sizes, the effects of radiation can become more and more pronounced. These two factors ensure that radiation tolerant electronics will require development long into the future.

Rising costs and complexity of state-of-the-art wafer fabrication facilities prevents the use of exotic, radiation hard processes. This guarantees that circuits will need to be *designed* to be radiation hard in standard processes. Future design techniques will likely include converting as much of the circuit to the digital domain as possible. This allows mature mitigation techniques for digital circuits to be used.

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