Low Voltage Switched Capacitor Circuits for Lowpass and Bandpass $\Delta\Sigma$ Converters

by

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To my wife, Nurcan Keskin
and my son, Baha Muammer Keskin

for being with me

Low Voltage Switched Capacitor Circuits for Lowpass and Bandpass $\Delta\Sigma$ Converters

CHAPTER 1
LOW VOLTAGE SWITCHED CAPACITOR INTEGRATORS

1.1 Introduction

State-of-the-art fine-linewidth CMOS technologies allow fully integrated mixed-signal (digital and analog) circuits to be fabricated on the same chip. This drastically increasing level of integration with continuously rising clock frequencies allows the implementation of more sophisticated and powerful digital systems on a single integrated circuit (IC). While this provides very low-cost and small-area ICs, the analog circuit design becomes more and more challenging.

Presently, the most critical issues of the analog circuit processing are: circuit noise, digital noise coupling, high clock rates, low supply voltages and low signal swings [46]. This work is focused on switched-capacitor (SC) circuit design with low-supply voltages (LSVs), which are important for reliability and power dissipation.

The miniaturization of ICs steadily continues three-dimensionally. This brings two critical reliability issues [1]: long-term voltage stress on the gate oxide and short-term junction breakdown due to high voltages.

Supply voltages are lowered in order to reduce power dissipation (PD) of digital circuits contributing to longer battery life. Portable devices are so pervasive that one can see them anywhere. Obviously, extending battery life and using lighter devices are very important considerations for a user. Hence, manufacturers and designers increasingly try to minimize the PD.

In the following sections, first, a common switched-capacitor integrator (SCI) will be explained. Then problems and their solutions with SC circuits with LSV will be discussed.

1.2 Switched-Capacitor Integrator

A SCI is the main circuit block of many data processing systems such as filters, data converters, sensor interfaces, etc. [24]. This circuit allows us to process a signal as sampled data. Sampled data signals and systems are well described by difference equations. In this way, it is easy to model and simulate the SC circuits by common simulation tools such as MATLAB and SWITCAP with ideal circuit conditions. At the circuit level, there are many issues that need special attention. Some of these issues are component mismatches, noise couplings, voltage dependencies, leakage currents, and layout gradient changes.

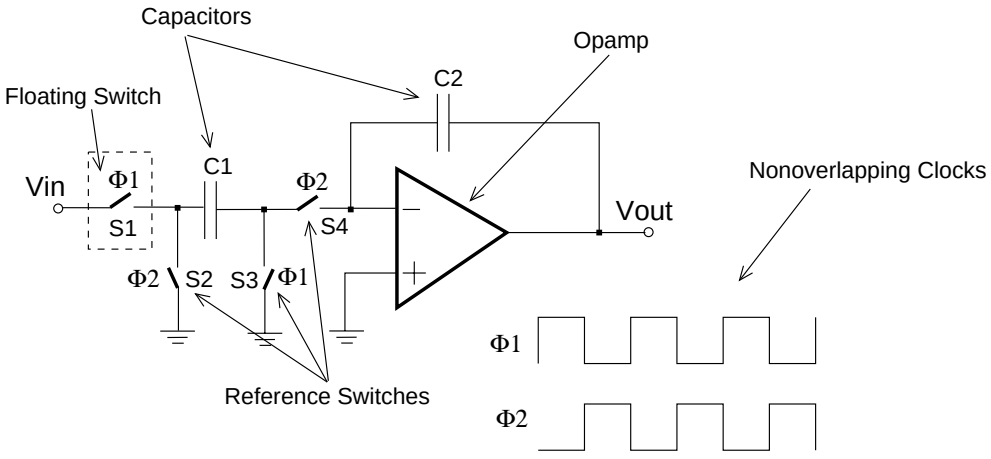

Figure 1.1. A conventional SC integrator.

A basic SCI consists of switches, capacitors, and opamps in Fig. 1.1 [29]. Another element in SCIs are the non-overlapping clock phases created to provide the sampling operation. Linear applications require high-accuracy clock generation.

As mentioned, the difference equations are easily derived for SCIs. In order to have the voltages on capacitors settled, sampling must occur at the end of the phases. The difference equation is:

$$C_2V_o(nT) = C_2V_o(nT - T) + C_1V_i(nT - T/2). \tag{1.1}$$

After taking the z-transform, this becomes:

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}\frac{z^{-1/2}}{1 - z^{-1}}. \tag{1.2}$$

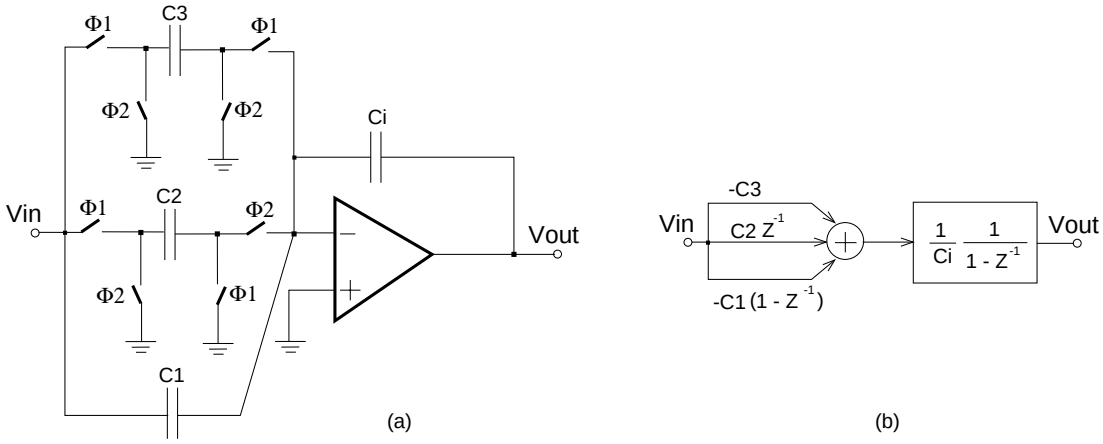

Figure 1.2. A switched-capacitor stage (a) circuit diagram (b) equivalent signal-flow-graph.

Obtaining the transfer function in the z-domain allows for system analysis by using the signal-flow-graph method [29] so that the capacitor branches can be replaced by their discrete-domain counterparts as shown in the example in Fig. 1.2.

The functionality of a capacitor in a SCI is not limited by a LSV. Clock waveforms are not limited since they are generated by digital cells. On the other hand, the other two circuit elements, switches and opamps, are affected by a LSV.

1.3 Switch Operation with a Low Supply Voltage

Fig. 1.3 shows the fundamental problem of switches when supply voltages are decreased. As seen in Fig. 1.3, the NMOS transistor turns on for an input signal from $V_{t,n}$ up to V_{DD} and the PMOS switch turns on from $V_{DD} - |V_{t,p}|$ down to 0 V. The limitation occurs for the supply voltage, which is less than $|V_{t,p} + V_{t,n}|$. In this case, none of the switches will be turned on for some signal values, hence the input signal is no longer connected to the output.

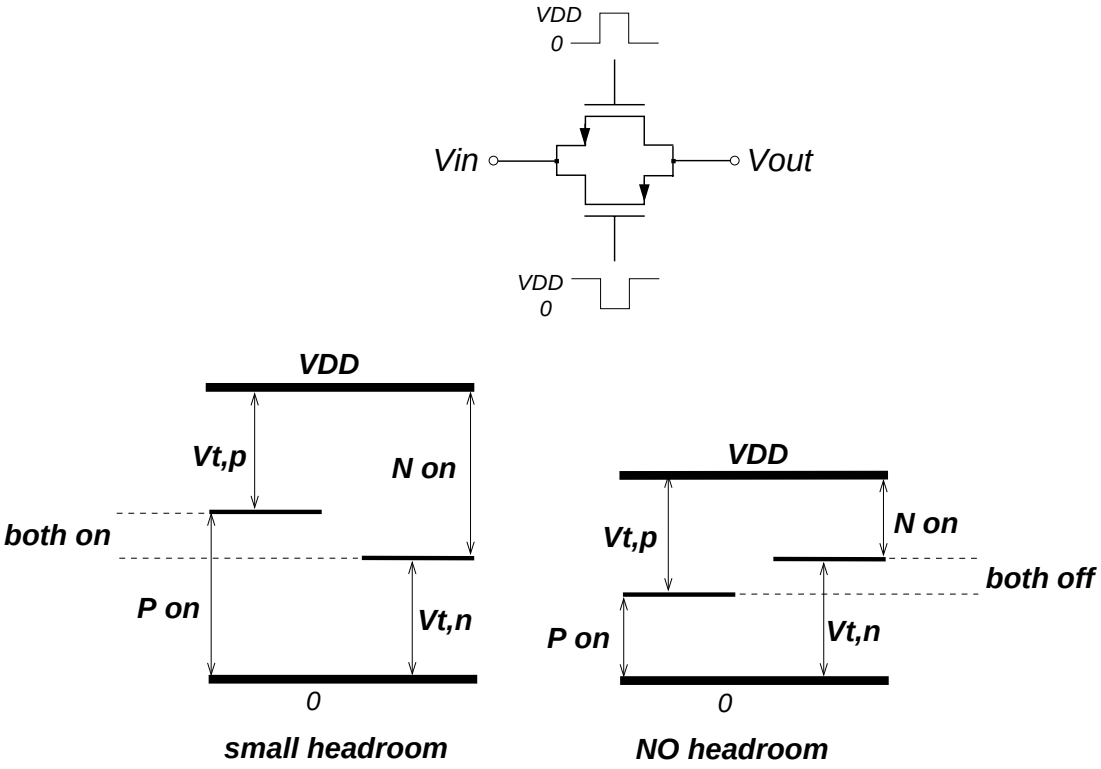

Figure 1.3. Fundamental problem of CMOS switches with low supply voltages.

The conduction requirements of the NMOS transistor are:

$$\begin{aligned} V_{gs,n} &\geq V_{t,n}, \\ V_{DD} - V_{in} &\geq V_{t,n}, \\ \text{and} \quad V_{DD} &\geq V_{t,n} + V_{in}. \end{aligned} \tag{1.3}$$

Similarly, the requirement can be stated for the PMOS device as follows:

$$\begin{aligned} V_{gs} &\leq V_{t,p}, \\ 0 - V_{in} &\leq V_{t,p}, \\ \text{and} \quad 0 &\leq V_{t,p} + V_{in}. \end{aligned} \tag{1.4}$$

These requirements imply that if the supply voltage is decreased to less than $|V_{t,p}| + V_{t,n}$, then there will be a dead interval without signal transmission even for complementary switches [51]. Such a switch is called a floating switch, i.e. its source is connected to neither V_{DD} (for PMOS) nor ground (for NMOS).

A switch is called a reference switch if one of its terminals is connected to either V_{DD} (for PMOS) or ground (for NMOS). This means that if V_{DD} is greater than $|V_{t,p}|$, PMOS switches will be turned on, and if V_{DD} is greater than $V_{t,n}$, NMOS switches will be turned on.

As seen in Fig. 1.1, switch $S1$ is surrounded by dashed rectangular in order to indicate that it is a floating switch in the SCI. The other switches, $S2$ and $S3$, are connected to signal ground while $S4$ is connected to virtual ground. These reference switches except $S1$ are functional with a LSV.

Next prior solutions and our solution to this problem will be introduced.

1.4 Low-Voltage Switched-Capacitor Circuits

There are three known solutions that use charge-pump circuits [25, 45], low-threshold devices [4], or switched-opamp circuits [17, 50].

The first and more common technique, is to employ charge-pump (voltage multiplier) circuits [23, 53] to generate a higher supply voltage on a chip. This technique provides an easy and quick way to design LV SC circuits since it allows whole circuits except the switches to work with LSVs. Since the other circuit parts use LSV, this technique saves power in some parts of the system. On the other hand, the charge-pump circuit by itself consumes area and power. Additionally, modern submicron CMOS technology does not sustain high voltages on chip anymore.

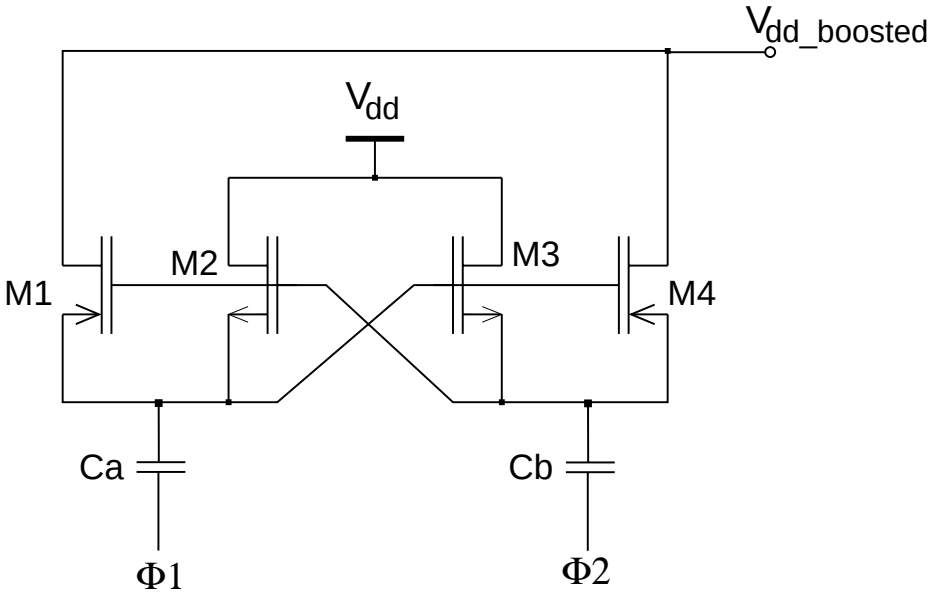

Figure 1.4. A voltage doubler.

An example of this type of circuit is shown in Fig. 1.4. With this voltage-doubler, when $\Phi 1$ and $\Phi 2$ are low, Ca and Cb are charged to V_{dd}, respectively. Then, Ca and Cb provide the boosted voltage when $\Phi 1$ and $\Phi 2$ are high.

There is another technique similar to this charge-pump method. This applies local voltage-boosting (LVB) at the switch gates [3, 20]. An example LVB circuit is shown in Fig. 1.5. During $\Phi 1$, capacitor C is precharged to V_{dd}. During $\Phi 2$, the bottom plate of C is connected to V_{in}. This way, the voltage at the top plate of C will be boosted to $V_{dd} + V_{in}$ at the of $\Phi 2$.

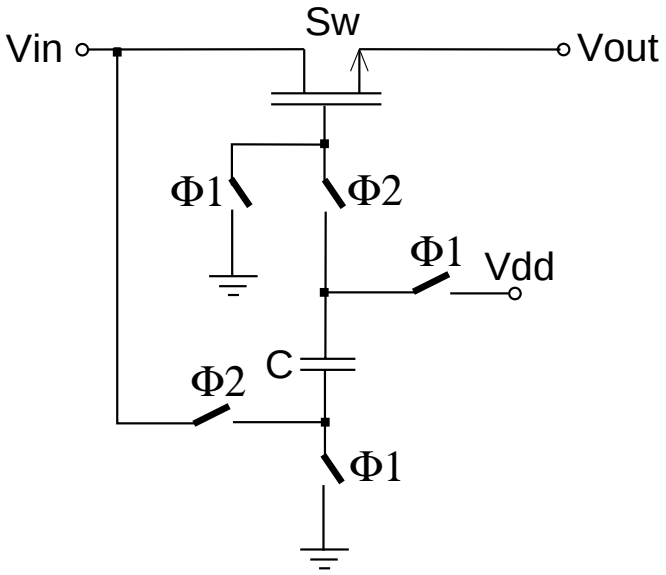

Figure 1.5. A local voltage-booster.

This operation is useful, not only for LV SC circuits, but also helps to reduce nonlinear resistance of the switch Sw [41]. The on resistance of the switch Sw is equal to

$$R_{sw} = \frac{1}{\mu C_{ox} \cdot (W/L) \cdot (V_{gs} - V_{th})} \tag{1.5}$$

where $V_{gs} = V_g - V_s = V_{dd} - V_{in}$ without the LVB circuit. Therefore, the value of R_{sw} depends on the amplitude of the input signal and introduces nonliear distortion.

With a LVB circuit, the gate voltage is boosted to $V_{dd} + V_{in}$, hence V_{gs} is equal to V_{dd}. Since the voltage difference between gate and source terminals does not depend on V_{in}, the linearity performance of the switch is improved. These techniques have proven to be effective means of providing solution to provide switches for LV SC circuits. Nonetheless, they require more switches to replace a single switch and may introduce reliability issues due to oxide breakdown.

The second technique is the use of a process with low threshold voltages [4], which has an undesired side effect. When the threshold of the device is lowered, the leakage current is increased during the off period of a switch. This is a most undesirable effect, especially for SC circuits, which must preserve the charges. Losing charge causes harmonic distortions. Additionaly, there is a high cost associated with a dedicated low-V_{th} process.

Another prior technique is the switched-opamp (SO) technique [17, 50]. The main idea is to replace the floating switch in Fig. 1.1. The purpose of the floating switch is to provide the input charge to $C1$ during $\Phi1$ and then isolate it from the input signal source during $\Phi2$. The functionality of this floating switch is replaced by a switchable opamp as shown in Fig. 1.6.

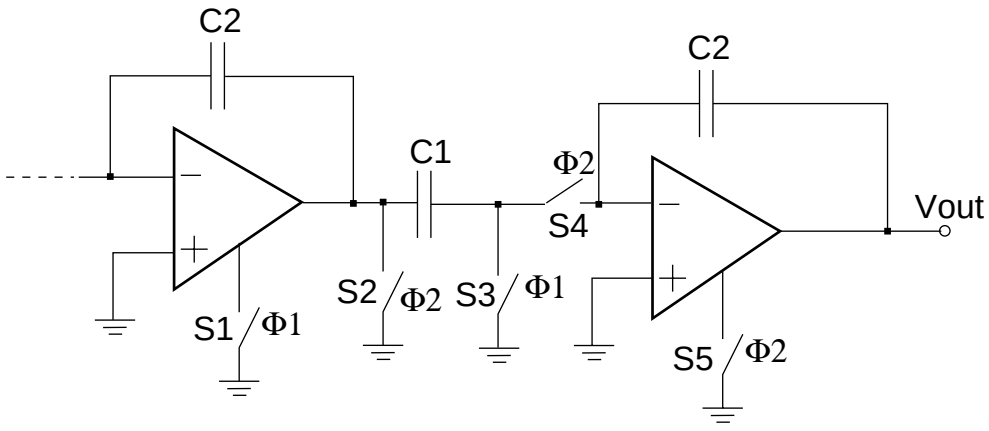

Figure 1.6. A switched-opamp integrator.

The opamp at the previous stage is switched on and off during Φ1 and Φ2, respectively. This operation successfully replaces the floating switch and allows for a lower supply voltage. The SO technique is suitable for submicron CMOS technology because none of circuit components require high supply voltages. Since the opamps are turned off every half clock cycle, SOs suffer from a speed limitation due to the transients introduced by the required time for power-up/power-down cycling. This will limit the clock frequency to only few MHz. There are ongoing efforts to increase the frequency range of SO circuits [13, 15]. In order to reduce the speed limitation, this technique still needs improvement.

Our solution to this problem is a new technique, which is conceptually similar to the switched opamp. In this technique, the opamp is kept on while the floating switch is eliminated as shown in Fig. 1.7. This will eliminate the transient time limitation of SOs, hence, the circuit will be functional with higher clock frequencies. The new structure is named the Reset-Opamp (RO) technique since the opamp is reset during one phase [10, 11, 31, 54, 55]. This architecture is also suitable for modern submicron CMOS processes.

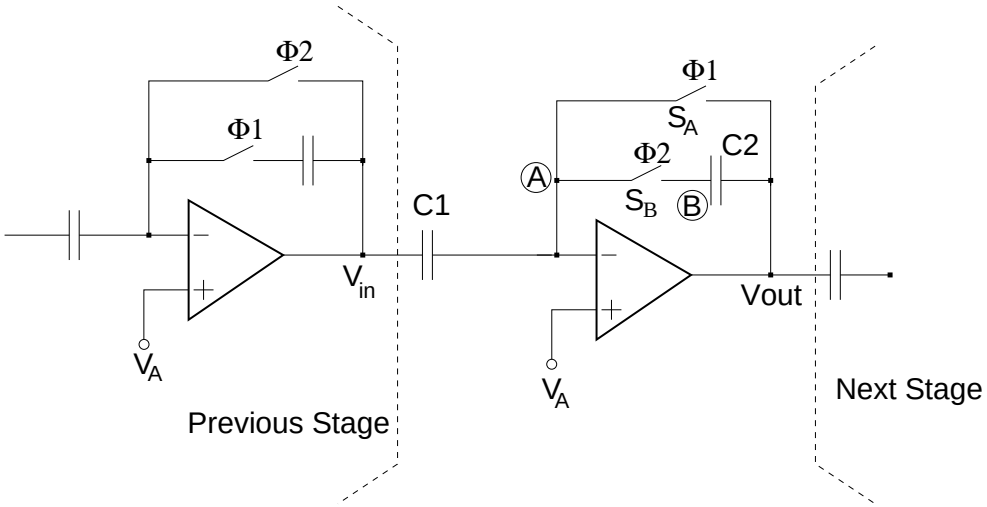

Figure 1.7. A reset-opamp SC integrator.

A straightforward implementation of the stage would introduce a practical problem due to forward-biased p-n junctions in the S_B switches. The operation of the circuit, and this problem, will be described in the following section.

1.5 Reset-Opamp Low-Voltage Integrators

It is clear that when $\Phi 2 = 1$, the circuit in Fig. 1.7 satisfies the appropriate equation for an inverting delay-free integrator. Notice that v_{in} is the output voltage of the preceding stage, which has the same architecture. Hence, if the preceding stage has the same switching sequence as the one analyzed, then $v_{in}(n - 1/2) = V_A$, where $v_{in}(n)$ is the output signal voltage of the preceding stage. If the reset switch (S_A) of the previous stage is closed during $\Phi 2 = 1$, and its feedback switch (S_B) is closed during $\Phi 1 = 1$, then the output voltage of the cascade is inverted and delayed.

Note that, at the cost of two additional switches, the right-hand terminal of *C1* can be disconnected from the virtual ground and grounded during the $\Phi 1 = 1$ period. Also, although some discussions in this paper refer to single-ended circuit realizations, practical implementations are pseudo-differential circuits [31].

As mentioned in the previous section, the simplest realization of the circuit of Fig. 1.7 leads to some practical difficulties. Assume that the analog ground voltage is $V_A = V_{SS} = 0$, as may be the case if the op-amps have PMOS input devices. Then, the conventional realization of the circuit calls for NMOS switches for both S_A and S_B. Assume also that the output voltage at the end of a $\Phi 2 = 1$ period approaches V_{dd}. Then, at the beginning of the next $\Phi 1 = 1$ phase, V_{out} is pulled down to ground by S_A, and the floating node B (between S_B and *C2*) is pulled down to approximately $-V_{dd}$ by *C2*. Since node B is connected to the n+ source diffusion region of S_B, the source-to-substrate junction of S_B will be forward biased, and *C2* will lose charge to the substrate. In what follows, several techniques for avoiding the forward-biased junction problem will be described.

1.5.1 Reset-Opamp Using a PMOS Switch

A possible solution to the junction leakage problem is illustrated in Fig. 1.8. This circuit uses an NMOS implementation for S_A, as before, but now uses a PMOS device for S_B. Now, the voltage drop from 0 to $-V_{dd}$ at node B will cause the source-to-well junction of S_B to be reverse biased, not forward biased. Hence, charge loss from *C2* is avoided.

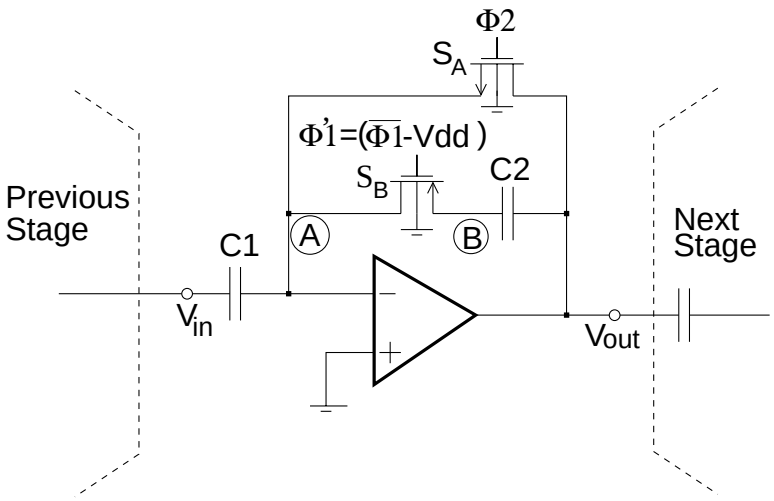

Figure 1.8. Reset-Opamp Integrator Using a PMOS Switch and Level-Shifted Clock.

The remaining issue is that the grounded PMOS switch device requires a negative clock voltage for conduction. A level-shifting circuit which can realize this is shown in Fig. 1.9.

It is a variant of the widely-used Nakagome clock-booster stage [22] and provides a clock signal varying between 0 and $-V_{dd}$. At power-up, the first few samples will be positive, leading to charge pumping into the well from the sources of the PMOS switches. This should not be a problem as long as the well is adequately grounded. After the third or fourth clock periods, the samples of V1 and V2 become negative, and the charge pumping stops.

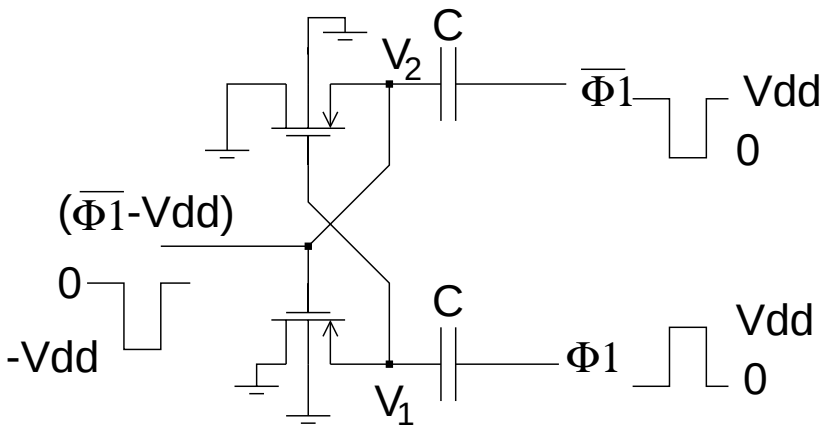

Figure 1.9. Level-shifted clock generator.

As an illustration of the integrator operation, Fig. 1.10 shows the simulated input, clock, and output voltages of the circuits of Figs. 1.8 and 1.9, under the following test conditions: $C1 = 1$ pF, $C2 = 0.5$ pF and V_{dd}=1 V, f_{in}=2.5-kHz, V_{in}=20-mVp-p square wave, and f_{clock}=200 kHz. A simple macromodel that consists of a dc gain of 3000 and a unity-gain bandwidth of about 2 MHz was used for the op-amp. More realistic Level 13 HSPICE models were used for the switches. Fig. 1.11 shows the simulated output waveform for a 10-kHz, 20-mVp-p sine-wave input signal, under the otherwise same conditions. The waveform includes the power-up transient affects near $t = 0$ s.

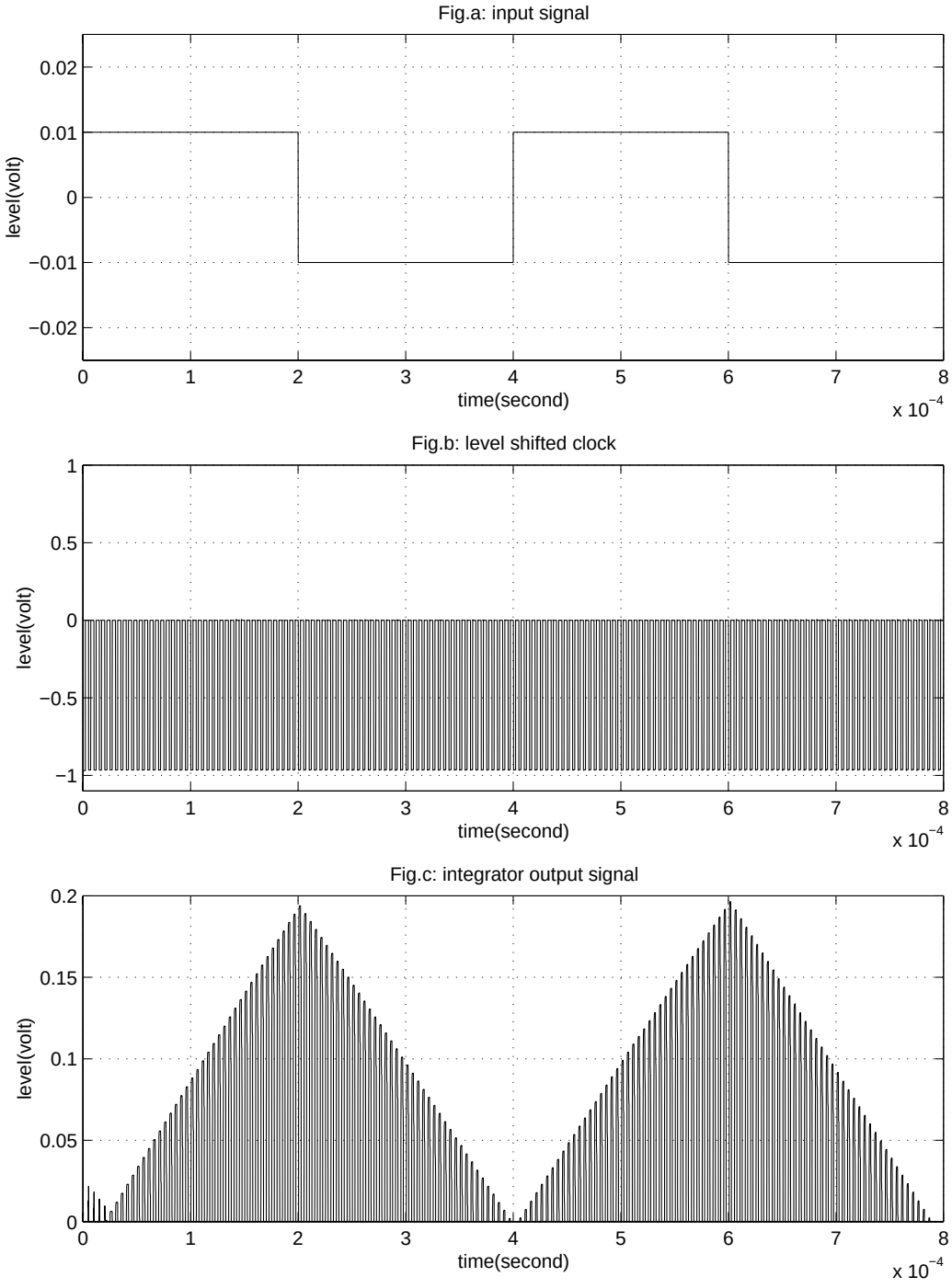

Figure 1.10. Simulated voltages in the integrator of Fig. 1.8: (a) input, (b) clock, and (c) output voltage.

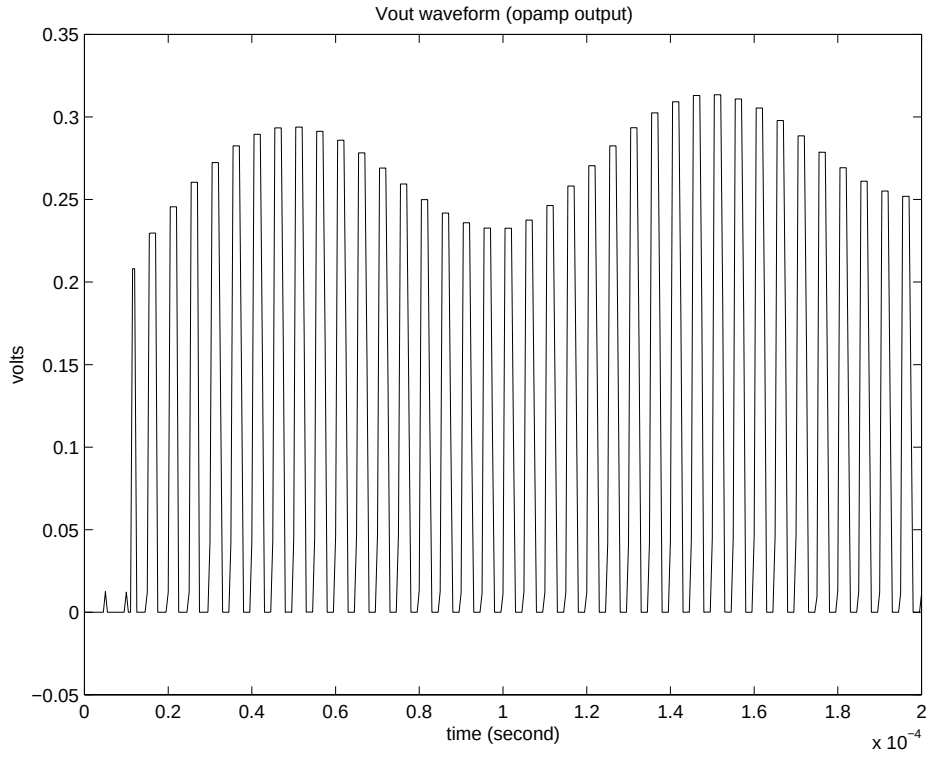

Figure 1.11. Simulated output waveform of the integrator in Fig. 1.8 for a sinusodial input.

1.5.2 Reset-Opamp Using a Floating Voltage Supply

An alternative realization, which also avoids charge leakage, is shown conceptually in Fig. 1.12. This circuit can be implemented using only NMOS switches, since when the reset switch (S_A) closes the output voltage rises to V_{dd}, rather than drop to 0 V as in the previous realization, and hence the voltage at node B cannot fall below 0 V. Thus, the source-to-substrate junction of the feedback switch (S_B) remains reverse-biased under all conditions. A more detailed circuit diagram, showing also the implementation of the floating V_{dd} source in the form of the switched capacitor *C3*, is illustrated in Fig. 1.13. It is also possible to implement a floating voltage source $V_{dd} - V_{DSAT}$, which allows the op-amp to retain a high gain during reset resulting in faster recovery.

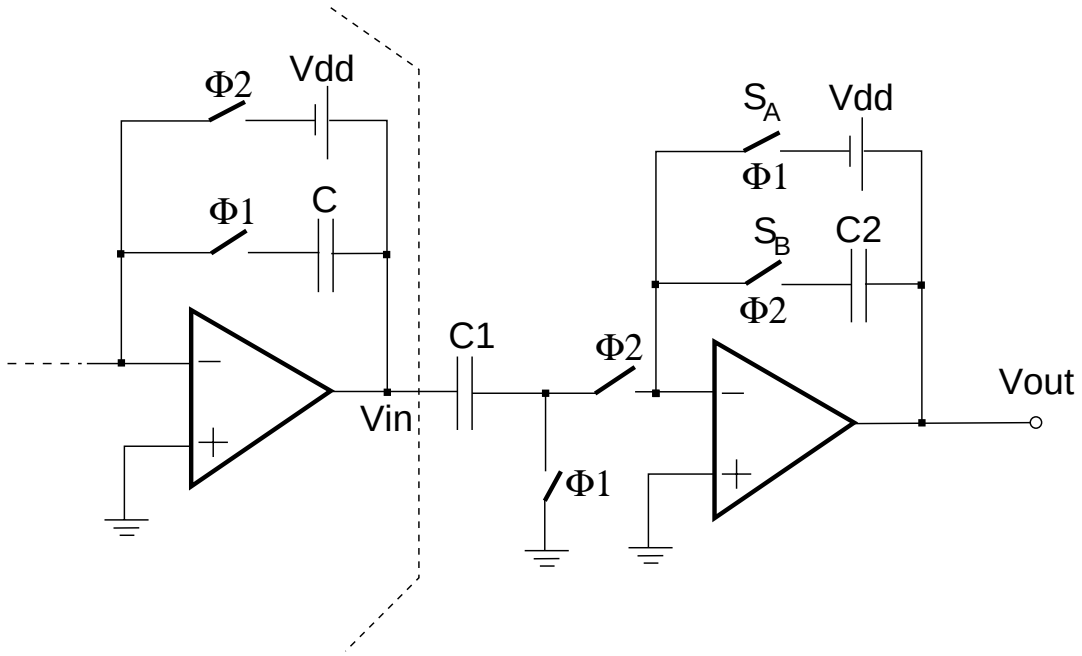

Figure 1.12. The LV SCI with floating supply.

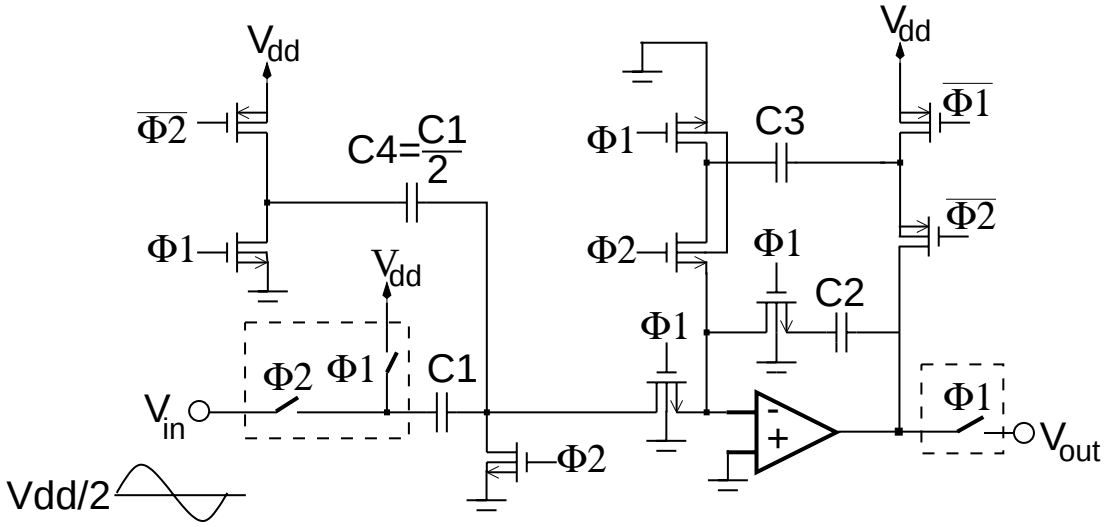

Figure 1.13. A possible implementation of a floating-supply integrator.

Note that the dc bias of the input signal is assumed in Fig. 1.13 to be $V_{dd}/2$, and hence a compensating branch, realized by the SC branch containing *C4*, is needed to prevent the output from ramping down due to the accumulation of charge from this input bias.

Fig. 1.14 shows the simulated time- and frequency-domain representations of the output voltage of the integrator stage of Fig. 1.13 for a 5-kHz, 0.2-Vp-p sine-wave input voltage, under the following conditions: *C1* = 1 pF, *C2* = 2 pF, and V_{dd}=1 V. The same macromodel that consists of a dc gain of 3000 and a unity-gain bandwidth of about 2 MHz was used for the op-amp. Level 13 HSPICE models were used for the switches.

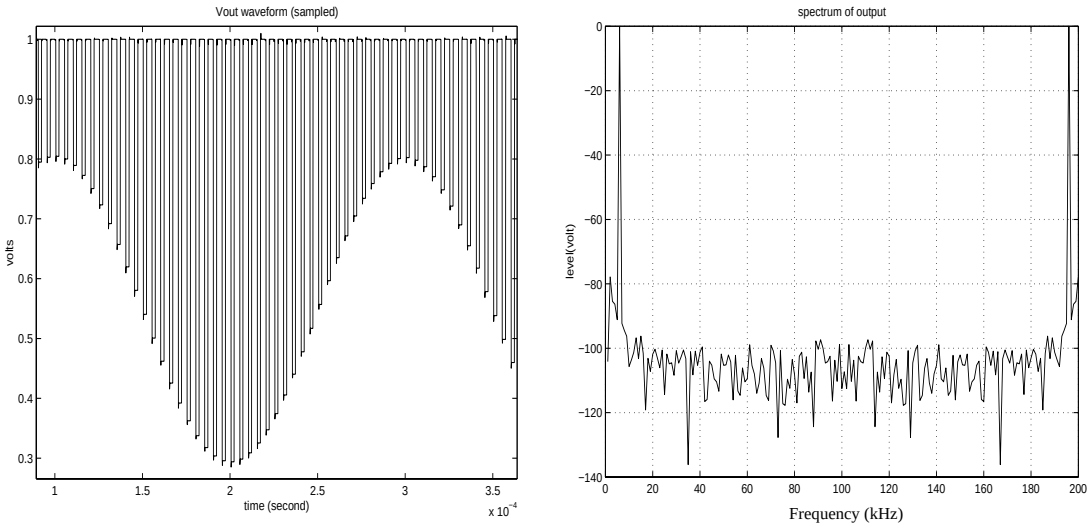

Figure 1.14. Simulated output in the time- and frequency-domain for the floating-supply integrator of Fig 1.13.

1.5.3 Reset-Opamp Using Master/Slave Integrators

Another technique for avoiding charge leakage in the low-voltage integrator of Fig. 1.7 is to use an extra op-amp stage (slave integrator) for storing the charge during the reset phase when the integrating capacitor is floating. Fig. 1.15(a) shows the schematic diagram of the circuit; Fig. 1.15(b) illustrates the clock phases.

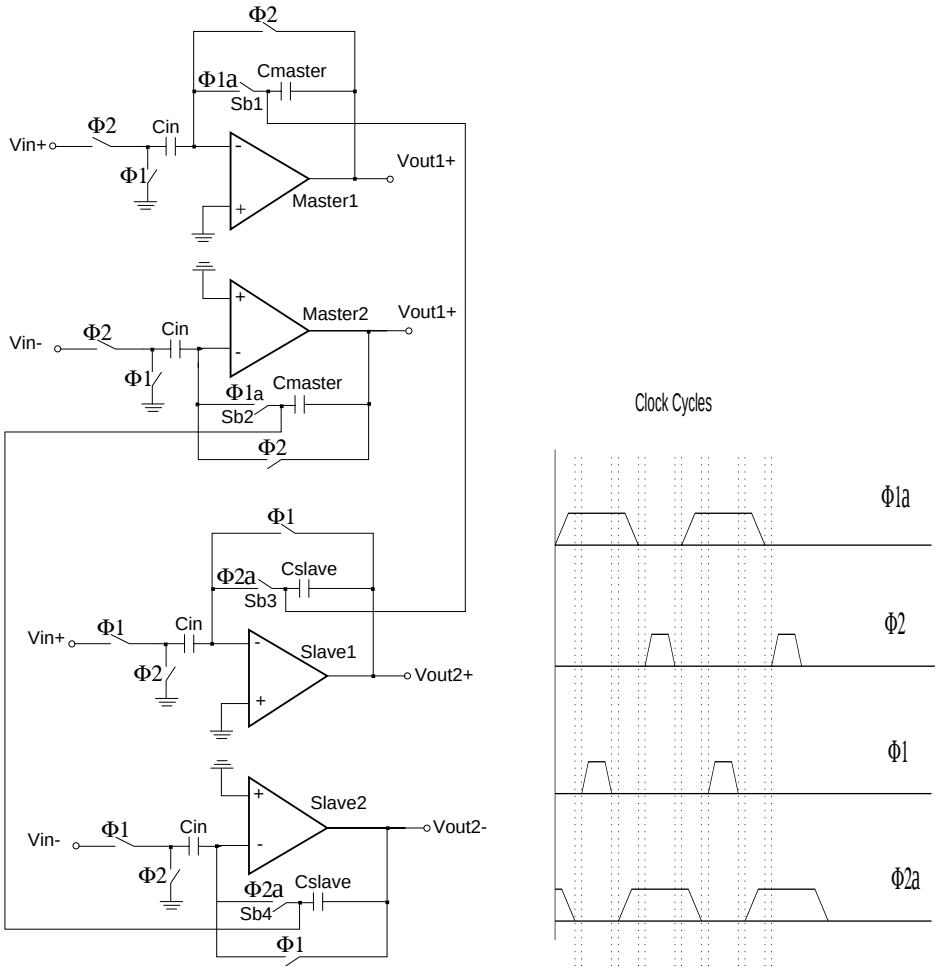

Figure 1.15. Master/slave reset-opamp integrator (pseudo-differential implementation).

The operation is as follows. When Φ2 and Φ2a rise, the signal charge stored in the master storage element C_{master} is transferred into the slave storage capacitor C_{slave}. When clock phases Φ1 and Φ1a rise, the charge is returned to C_{master}. The nodes A and B are kept at or near the analog ground thereby preventing charge leakage. This stage can use single-channel (NMOS) switches everywhere, since all switches operate at analog ground potential.

A drawback of the master-slave structure is the need for the second integrator stage. However, it is possible to operate the structure in a double-sampling mode, in which both integrators receive input charges in alternating clock periods. For such a "ping-pong" circuit, the sampling rate can be doubled without increasing the op-amp bandwidth.

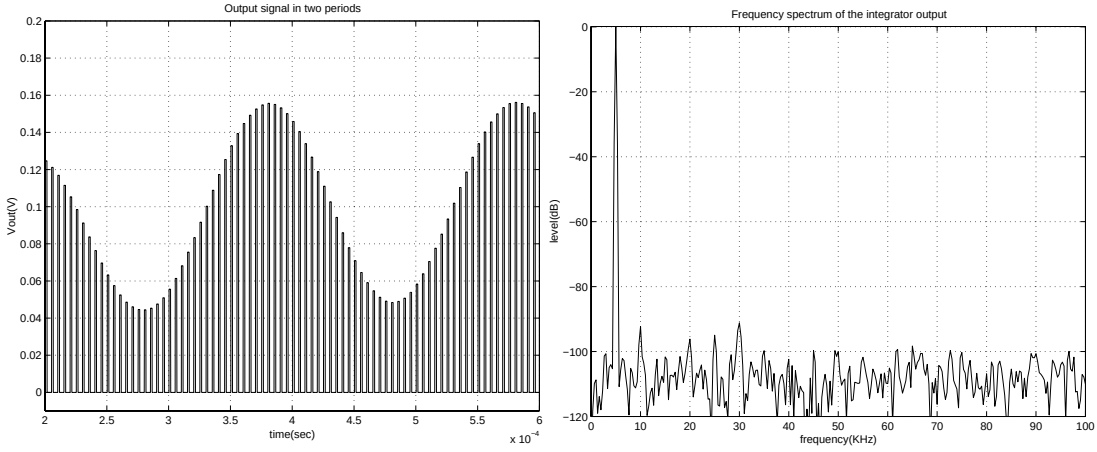

Figure 1.16. Simulated output in the time- and frequency-domain for the master/slave integrator of Fig 1.15.

The performance of this integrator was simulated using HSPICE. A macro model, corresponding to a dc gain of 80 dB and a unity-gain frequency of 100 MHz was used for the opamp. All capacitors were chosen as 2 pF. The switches, of dimensions L=0.6 μm and W=10 μm, were simulated by the Level 13 HSPICE models. The sampling frequency was 200 kHz. A 20-mVp-p 5-kHz sine wave was

used as input signal. Fig. 1.16(a) shows the output voltage over two periods; Fig. 1.16(b) illustrates its frequency spectrum. The low harmonic distortion verifies the absence of charge leakage.

1.6 Conclusions

The drive toward low-voltage operation for analog-circuits, in particular filters and converters, is progressing with increasing strength. Key issues with modern submicron CMOS technology are low-power dissipation, small chip area, and ultimately low cost. At low supply voltages, the key problem with analog circuits is to keep signal-to-noise ratio and dynamic-range as close as possible to that of circuits with higher supply voltages. This is very difficult particularly in mixed-mode systems where digital noise-coupling degrades the performance of the analog systems. The ultimate goal is to keep the voltage swing of signals as large as possible for analog signal processing.

A key problem with the switched-capacitor circuits with low supply voltages to operate MOS switches properly is introduced in this section. Existing circuit configurations designed to cope with this problem are also introduced. During this research, three different reset-opamp integrators were proposed. These circuits are functional with 1-V supply voltage. Additionaly, they are applicable to high-frequency SC applications.

CHAPTER 2
A LOW VOLTAGE LOWPASS $\Delta\Sigma$ MODULATOR

2.1 Introduction

A low-voltage $\Delta\Sigma$ modulator, incorporating unity-gain-reset opamps, is described. Due to the feedback structure, the opamps do not need to be switched off during operation, and hence can be clocked at a very high rate. A test chip, realized in a 0.35-μm CMOS process and clocked at 10.24 MHz, provided a dynamic range (DR) of 80 dB and a signal-to-noise+distortion-ratio (SNDR) of 78 dB for a 20-kHz signal bandwidth, and DR = 74 dB and SNDR = 70 dB for a 50-kHz bandwidth.

The performance of some existing modulators are compared in Table 2.1. This table shows the type, order, technology, power supply voltage (VDD), dynamic range (DR), power dissipation (PD), signal bandwidth (BW), and clock rate (Fclk). There have been different methods used to implement LV $\Delta\Sigma$ modulators such as: switched-capacitor (SC), process with low-threshold devices (LT), switched-opamp (SO), reset-opamp (RO), continuous-time (CT), voltage multiplier (VM) and local clock boosting (LB).

We will discuss the design issues of the RO $\Delta\Sigma$ modulator in the following sections: system level design, building blocks of LV $\Delta\Sigma$, and the overall implementation.

Ref.	Type	Order	Technology	VDD	DR	PD	BW	Fclk
Index			[μm] (C)	[V]	[dB]	[mW]	[kHz]	[MHz]
[44]	SO	3	0.6	0.9	77	0.04	16	1
[6]	SO			1	45	0.24	20	
[8]	SC,LT	1	0.5	1	54	0.1	4	1
[39]	CT,LT	4	0.5	1	58	1.56	192	6.14
[43]	SO			1.5	74	0.1	3.4	
[25]	SC,VM	2	0.6	1.8	94	2	3.5	2
[45]	SC,VM	2+1	1.2	1.8	92	5.4	25	2
[5]	SC,VM	3	1.2	1.95	73	0.34	8	1.024
[52]	CT	4	0.5	2.2	80	0.2	3.4	0.512
[47]	SC,VM	2	0.5	1.5	88	0.55	1	1
[20]	SC,LB	3	0.35	1	88	1	25	5
[31]	**SC,RO**	**2**	**0.35**	**1**	**80**	**5**	**20**	**10**

Table 2.1. Performance of state of the art SC low-voltage lowpass $\Delta\Sigma$ modulators.

2.2 System Level Design of Lowpass $\Delta\Sigma$ Modulators

One common converter is a second-order single-bit switched-capacitor $\Delta\Sigma$ modulator [12]. This simple modulator, shown in Fig. 2.1, is chosen to show the basic functionality of the proposed LV SC integrator.

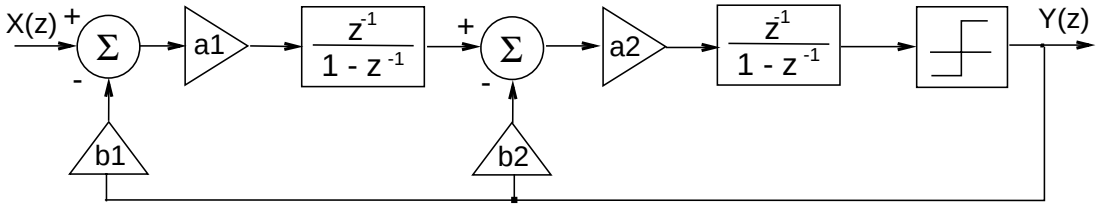

Figure 2.1. A common second-order single-bit $\Delta\Sigma$ modulator.

As shown, there are two full-delay integrators in the forward path and two feedback paths that ensure stability. The integrator gain factors $a1$ and $a2$ can be adjusted in order not to saturate the outputs of the opamps. The feedback gain factors $b1$ and $b2$ should be calculated to provide stability and the desired signal and noise transfer functions [34].

2.2.1 Signal and Noise Transfer Functions

In order to calculate noise and signal transfer functions, first, the quantizer should be replaced with a linear model. It is modeled by a gain stage and added quantization noise (q) as shown in Fig. 2.2.

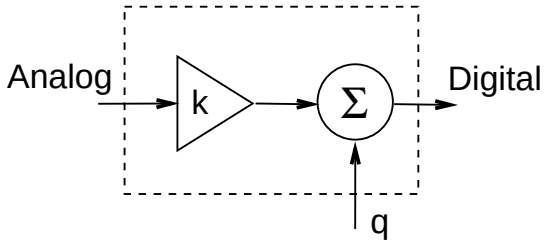

Figure 2.2. Linear model of a quantizer.

The transfer functions can be derived by assuming q as white and uniformly distributed additive noise. The z-domain equation of the modulator output in Fig. 2.1 is shown in Eqn. 2.1.

$$Y(z) = ka_2\frac{z^{-1}}{1-z^{-1}}\Big[-b_2Y(z) + a_1\frac{z^{-1}}{1-z^{-1}}\Big(-b_1Y(z) + X(z)\Big)\Big] + q(z). \quad (2.1)$$

The signal-transfer-function (STF) and noise-transfer-function (NTF) are given in Eqn. 2.2 and 2.3, respectively.

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{ka_2a_1z^{-2}}{1+(a_2b_2k-2)z^{-1}+(1-a_2b_2k+a_1a_2b_1k)z^{-2}} \quad (2.2)$$

$$NTF(z) = \frac{Y(z)}{q(z)} = \frac{(1-z^{-1})^2}{1+(a_2b_2k-2)z^{-1}+(1-a_2b_2k+a_1a_2b_1k)z^{-2}} \quad (2.3)$$

The ideal transfer functions of a second-order single-bit $\Delta\Sigma$ modulator are

$$STF(z)_{ideal} = \frac{Y(z)}{X(z)} = z^{-2} \quad \text{and} \quad NTF(z)_{ideal} = \frac{Y(z)}{q(z)} = (1-z^{-1})^2 \quad (2.4)$$

The coefficients in Eqn. 2.2 and 2.3 can be computed by setting them equal to those of Eqn. 2.4. This will result in these coefficient equations:

$$\begin{aligned} 1 - a_2b_2k + a_1a_2b_1k &= 0, \\ a_2b_2k - 2 &= 0, \\ \text{and} \quad ka_2a_1 &= 1. \end{aligned} \quad (2.5)$$

The above equations can be used to adjust the coefficients for the best performance without changing the pole and zero locations of the transfer functions as in STF and NTF.

2.2.2 Signal-to-Noise Ratio

The signal-to-quantization-noise ratio can be calculated by using the NTF as follows:

$$|NTF(z)|^2 = |(1-z^{-1})^2|^2 \qquad z = e^{jwT_s} \tag{2.6}$$

$$= |cos(wT_s) - 1 + jsin(wT_s)| \tag{2.7}$$

$$= 2\,[3 - 4cos(w) + cos(2w)]. \tag{2.8}$$

where $T_s = 1$ in a normalized domain. The quantization noise at the output is calculated by multiplying with the squared version of the NTF. This noise, at the output of the modulator is integrated in order to compute total noise power over the desired signal band as follows:

$$P_{noise} = \int_0^{w_b} |NTF(z)|^2 PSD_q(w)dw \tag{2.9}$$

$$= \frac{2{\sigma_n}^2}{\pi} \int_0^{\frac{\pi}{R}} \Big[3 - 4cos(w) + cos(2w)\Big]dw \tag{2.10}$$

$$= \frac{2{\sigma_n}^2}{\pi}\Big[\frac{3\pi}{R} - 4sin(\frac{\pi}{R}) + \frac{1}{2}sin(\frac{2\pi}{R})\Big] = \frac{\pi^4\sigma_n^2}{5R^5} \tag{2.11}$$

The signal-to-noise ratio (SNR) is given by

$$SNR = 10log_{10}\Big(\frac{P_u}{P_{noise}}\Big) = 20log_{10}\frac{A_u}{A_{max}} + 6.02N + 50log_{10}(R) + 11.14 \tag{2.12}$$

where A_u and A_{max} are the peak value of the signal and peak value of the noise amplitude. As seen from the equation above, every doubling of the oversampling ratio R will increase the SNR by 15 dB. In other words, the number of converted bits will be increased by 2.5 bits for every doubling of the OSR.

2.2.3 The Low Voltage ΔΣ System

Common ΔΣ modulators use full-delay integrators in the forward path of the modulators. On the other hand, our *reset-opamp* technique uses half-delay integrators. The ΔΣ loop needs two more half-delays either in the forward path or in the feedback path in order to ensure stability. Introduction of a half-delay in the analog domain can be difficult and may require some extra area and power consuming components. This can be avoided by using half-delay RS flip-flops in the digital domain. By all means, this will save area and power, without degrading performance. The modified configuration is shown in Fig. 2.3. System level MATLAB simulation result is shown in Fig. 2.4.

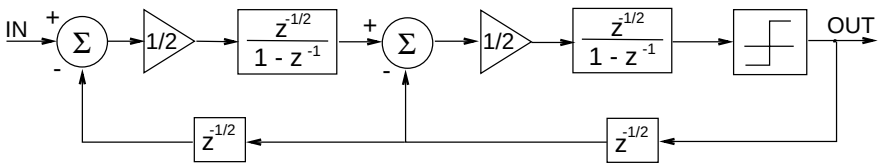

Figure 2.3. Low-voltage ΔΣ modulator.

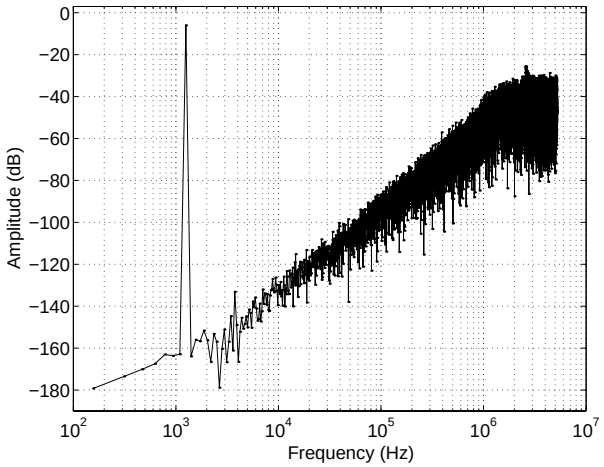

Figure 2.4. Frequency spectrum of the digital output stream of the LV ΔΣ modulator simulated in MATLAB.

2.2.4 Scaling the Dynamic Range of Integrators

The output signal levels of the integrators are important in this LV design and have to be approximately between 0.2 V and 1.0 V, in order to keep the opamps functional. These voltage limits are defined by the saturation boundaries of the output components of the LV opamp as follows:

$$V_{ds,sat,n} \leq V_{out} \leq V_{dd} - V_{ds,sat,p} \tag{2.13}$$

The output histograms of the integrators of the modulator in Fig. 2.3 with the coefficients, $a_1 = a_2 = 1/2$ and $b_1 = b_2 = 1$, are plotted in Fig. 2.5.

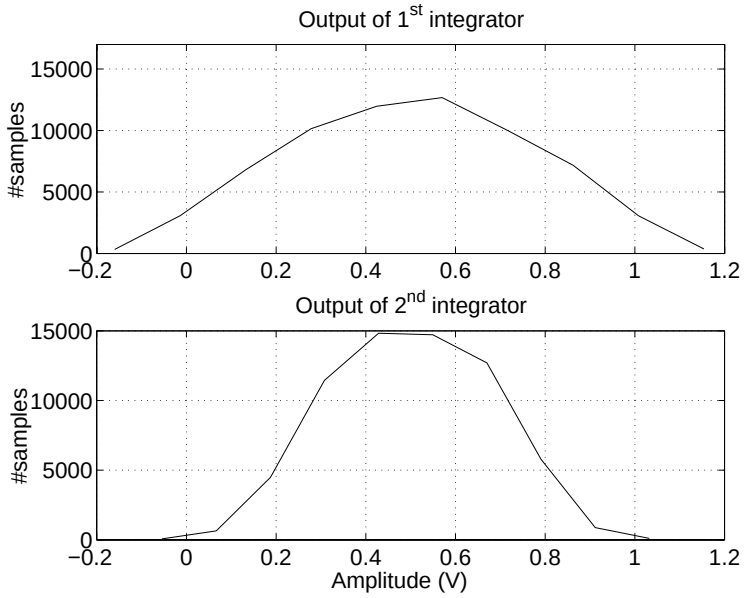

Figure 2.5. Histograms of the integrator outputs for the $\Delta\Sigma$ modulator with the coefficients: $a_1 = a_2 = 1/2$ and $b_1 = b_2 = 1$.

As shown, neither of the integrators could satisfy the desired range. Hence, gain coefficients need to be adjusted in order to scale the dynamic range of the opamps. They have been chosen to be $a_1 = 1/4$, $a_2 = 1/2$, $b_1 = 1$, and $b_2 = 1/2$ satisfying Eqn. 2.6. The MATLAB simulation results are shown in Fig. 2.6.

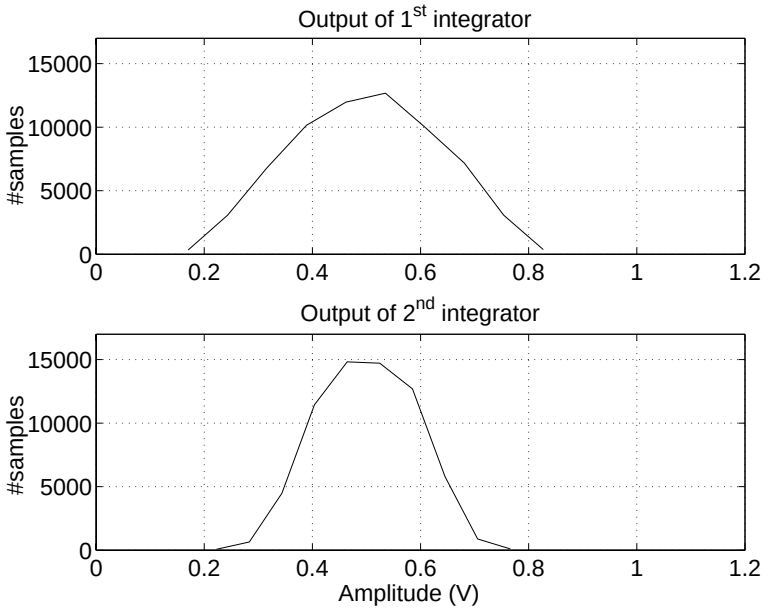

Figure 2.6. Histograms of the integrator outputs for the $\Delta\Sigma$ modulator with coefficients $a_1 = 1/4$, $a_2 = 1/2$, $b_1 = 1$, and $b_2 = 1/2$.

2.3 Low-Voltage Opamp

Several opamp design factors must be considered such as DC gain, unity-gain-bandwidth, slew rate, phase margin, input and output impedance, common-mode voltage levels at the input and the output, common-mode rejection, voltage swing, and linearity. Some of these design factors are more important than others, depending on the particular application. In this research, the most important opamp design issues are the low supply voltage, voltage swing, and bandwidth.

It is not feasible to connect more than four transistors between supply rails with a LSV. This assumes that all of the transistors are in saturation and only have $V_{ds,sat}$ across their source and drain. This limits the number of cascoded devices, therefore a multistage architecture is preferable. Cascaded structures provide high DC gain, but need frequency-compensation circuits to keep large bandwidths. However, multistage opamps have the advantage of design flexibility.

Common-mode signal levels at the input and the output are also design factors. Depending on the circuit topology, different common-mode signal levels can be chosen for the input and the output of the opamp.

Another design issue with LV opamps is the limited output signal swing. In order to maximize the signal swing, the number of stacked transistors should be minimized at the output since each transistor requires at least a voltage drop of $V_{ds,sat}$.

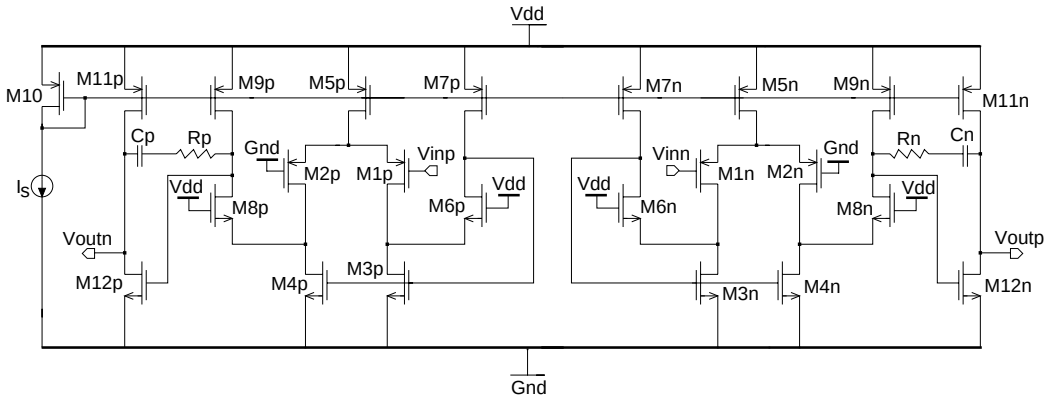

Figure 2.7. The LV pseudo-differential opamp.

Theoretically, the gain of the opamp should be higher than the oversampling ratio [41]. Hence, a two-stage Miller-compensated opamp will satisfy the gain requirement in this particular design. Based on the above considerations, the LV opamp is designed as shown in Fig. 2.7.

This opamp has a pseudo-differential structure, chosen to ease the implementation of the common-mode feedback (CMFB) circuit. Each half contains a PMOS differential input pair and an NMOS inverting output stage with an RC compensation branch between them. The input stage uses a LV current mirror [44]. The transistor sizes of the first and second stage opamps are shown in Table 2.2.

	1^{st} Stage	2^{nd} Stage
Components	W/L [μm]	W/L [μm]
M1-M2	100/0.5	80/0.5
M3-M4	60/0.5	50/0.5
M6-M8	20/0.5	10/0.4
M7-M9	150/1	75/0.75
M5	300/1	150/0.75
M10	15/0.5	15/0.5
M13-M14	20/0.5	20/0.5
M11	525/0.5	255/0.5
M12	275/0.5	165/0.5

Table 2.2. Transistor sizes of the LV opamp employed in the lowpass modulator.

The minimum supply voltage needed for linear operation is given by

$$V_{dd,min} = max\,[\,3V_{ov}, V_{th} + 2V_{ov}\,]. \tag{2.14}$$

In addition to the above low voltage supply considerations, settling time and slew rate are also important design criteria in this application. Although this application is for digital audio, we increased the clock frequency to 10 MHz range in order to show the effectiveness of the *reset-opamp* technique. The simulated performance parameters of the opamp with a load of 3.5 pF are summarized in Table 2.3.

Simulation results of the LV opamp with a 0.35 μm CMOS process are shown in Fig. 2.8, Fig. 2.9 and Fig. 2.10.

Adc	fu	PM	Tsettling	Slew Rate
68 dB	170 MHz	70°	20 ns	100 V/μs

Table 2.3. Simulated performance of the LV opamp.

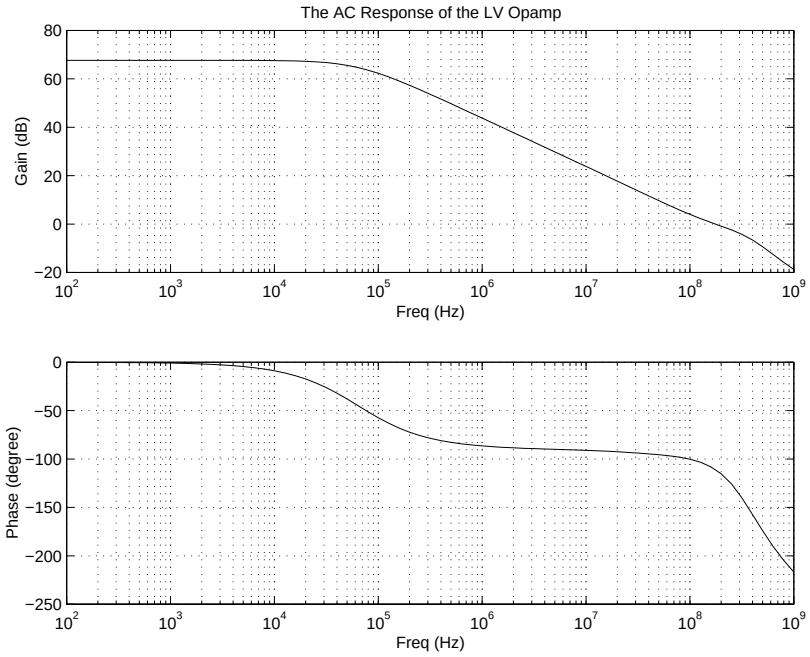

Figure 2.8. Frequency response of the LV opamp.

2.4 Switched-Capacitor Level Shifting Circuit

A charge-domain dc level shifter is required to maintain the appropriate input and output common-mode voltages (CMVs) for the opamps. At the outputs of the opamps, the CMV is set to middle of the supply rails ($V_{dd}/2$) while at the input of the opamps it is set to 0 V. For this reason, the dc charges coming from the previous stage will be cancelled out at the input of the next stage. This is realized by using two switches and one capacitor for each path as shown in Fig. 2.11.

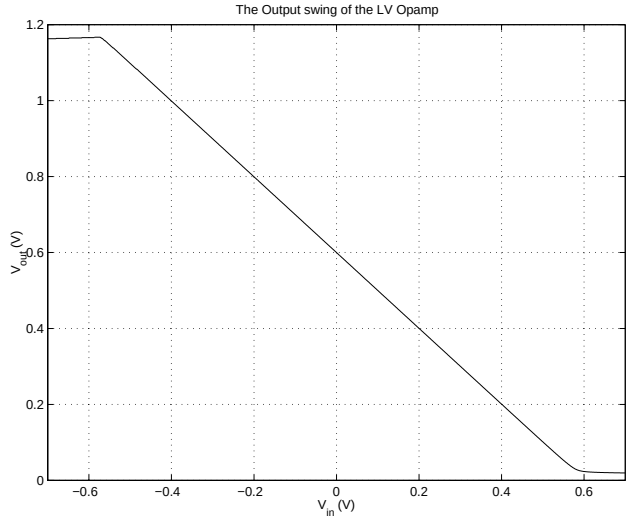

Figure 2.9. Output voltage swing of the LV opamp.

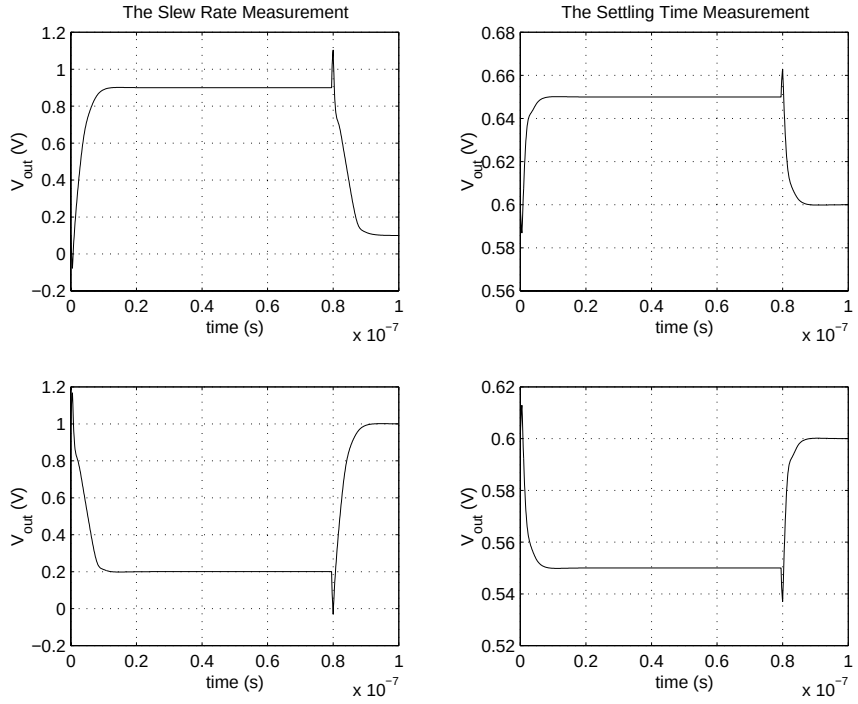

Figure 2.10. Slew rate and settling time response of the LV opamp.

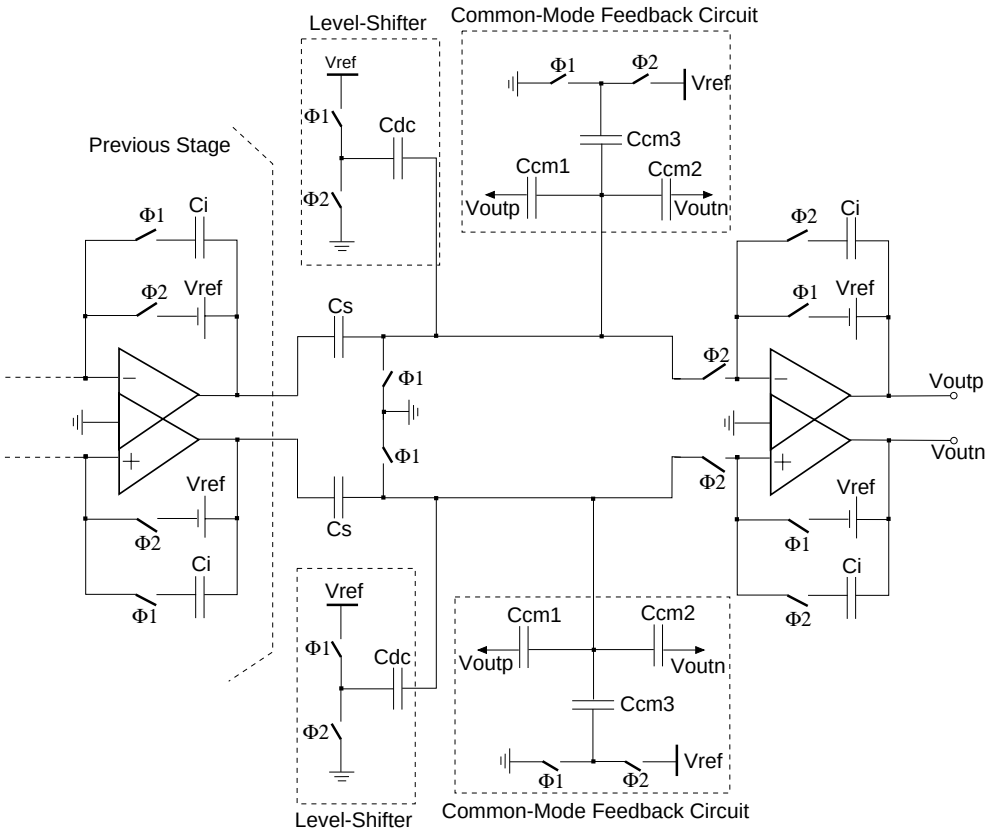

Figure 2.11. The pseudo-differential integrator with level shifting and common-mode feedback circuits.

The input charge Q_{in} provided to the LV integrator is calculated as follows:

$$Q_{in} = C_s(V_{dd} - V_{common} - v_{in}) = C_s(V_{dd}/2 - v_{in}). \tag{2.15}$$

As seen from the above equation above the amount of DC charge, to be cancelled out, is equal to $C_s \cdot V_{dd}/2$ when V_{common}=$V_{dd}/2$. At the same time, C_{dc} introduces DC charge according to

$$Q_{dc} = (-V_{dd})C_{dc} = -V_{dd} \cdot C_s/2 \tag{2.16}$$

where the size of C_{dc} is half that of C_s. Eventually, DC charges from Cdc and Cs are of the same magnitude, but, of opposite polarity. Therefore, integrating capacitor C_i receives only AC signal charges, not DC.

Circuit components are never perfectly matched, which causes uncancelled charge from input offset voltages and from switches, these uncancelled DC charges will be constantly integrated in every clock cycle. Over time, the opamp will eventually saturate either to the negative or positive supply rails without a common-mode feedback circuit.

2.5 The Common-Mode Feedback Circuit

The common-mode feedback circuit (CMFB) [54] is used in order to control the DC level of the output voltage shown in Fig. 2.11. The continuous-time CMFB circuit must power-up and settle within one clock phase, due to the resetting mechanism during the other clock phase. Pseudo-differential architectures were succesfully used before in SC filter applications without CMFB circuits. These circuits accomodate a larger signal swing, therefore, relax the requirements of the CMFB circuits. This leads us to using pseudo-differential structures.

During phase Φ_1, the common node of the three capacitors, labelled C_{cm}, is pulled to ground, while opamp outputs are set to V_{ref}. During phase Φ_2, the average of the opamp outputs is set to $V_{DD}/2$ if there is no common-mode offset error. Due to this shift, C_{cm1} and C_{cm2} inject a negative charge into the virtual ground of the opamps. Then the capacitor C_{cm3} neutralizes this charge. On the other hand, if there is any common-mode error accumulation at the opamp outputs, the net value of the charges moving to the inputs of the opamps will act to correct for the error.

An HSPICE simulation was performed in the context of a $\Delta\Sigma$ modulator and a small amount of common-mode error introduced at the beginning of the transient simulation is shown to be corrected in Fig. 2.12.

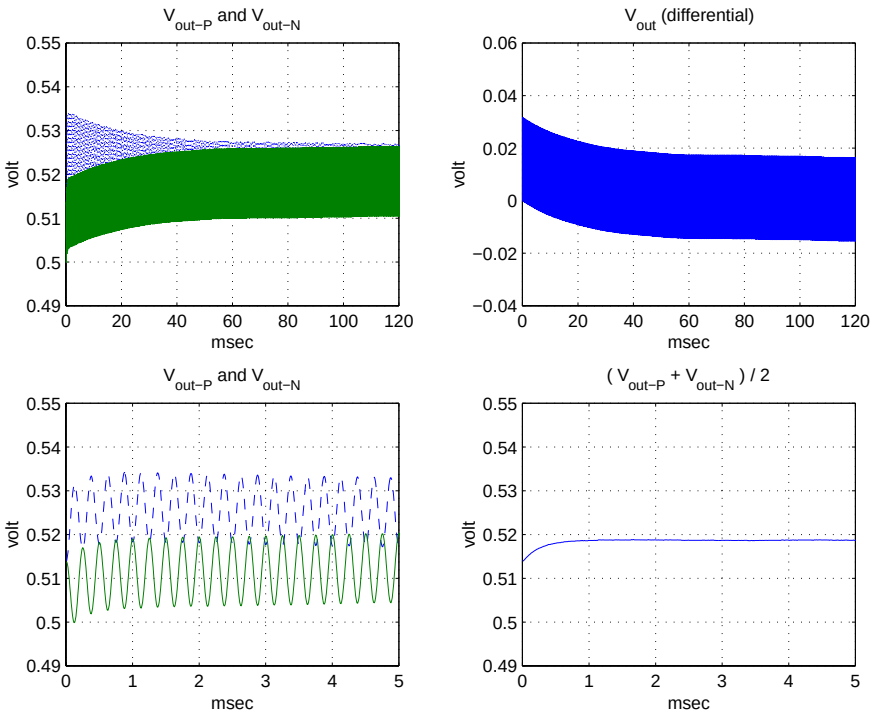

Figure 2.12. Transient time simulation results showing the settling behaviour of the CMFB in the pseudo-differential integrator of Fig. 2.11

2.6 Low-Voltage Comparator

The low-voltage comparator used is shown in Fig. 2.13. A PMOS input differential pair and an NMOS regeneration latch are used. This comparator requires DC level shifters at the inputs to set the input common-mode voltage to ground. The reset switches set both latch outputs to 0 V since floating reset switches cannot be used. The simulated transition speed of the comparator is 12 ns.

The conversion time has two components. The first, is the time it takes to go from the start of a comparison (when reset switches are turned off) to the metastable state for both outputs. Second, is the time it takes for both outputs to diverge. Time domain simulation results are shown in Fig. 2.14.

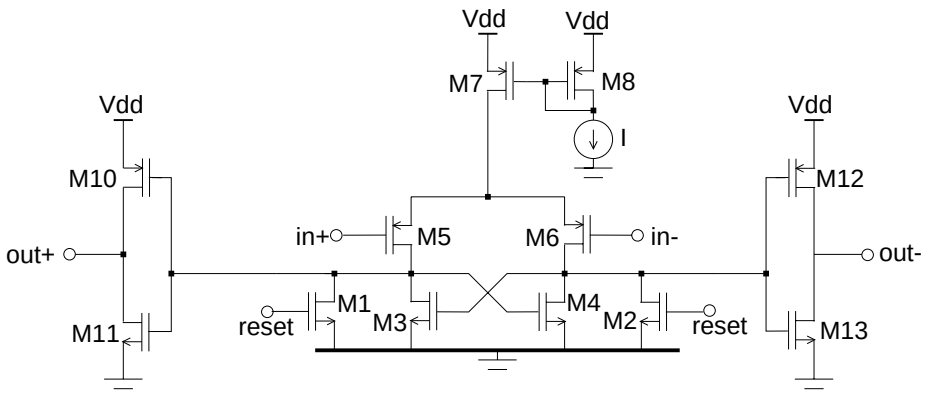

Figure 2.13. LV comparator.

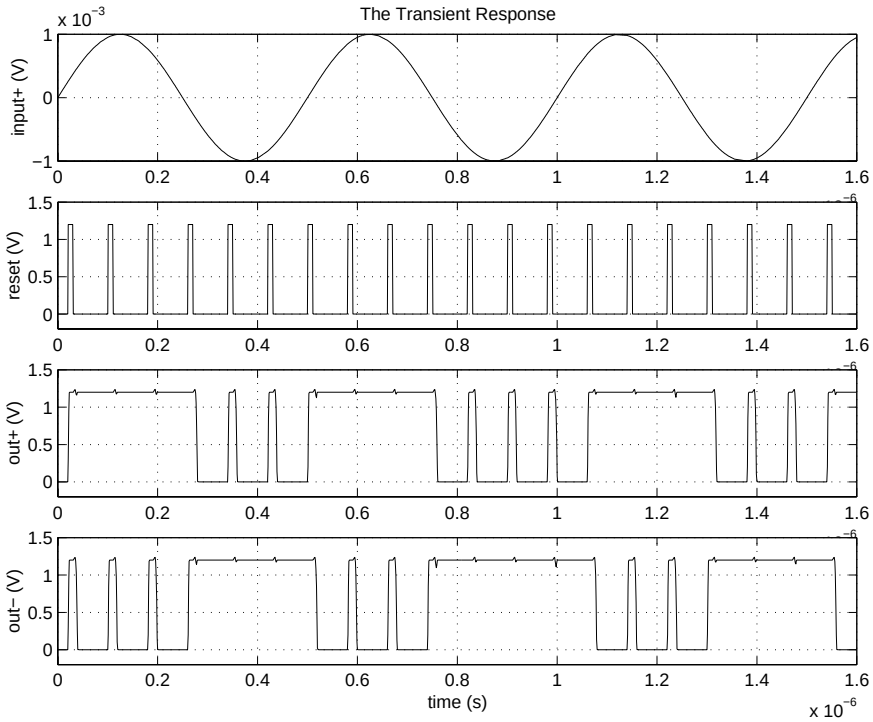

Figure 2.14. Transient time simulation results of the LV comparator in Fig. 2.13

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2.7 DAC Feedback Branches

The circuit diagram of the DAC feedback branches is shown in Fig. 2.15. The switches operate at ground or V_{dd}. The common-mode voltage of the DAC signal is cancelled by the level-shifting circuit at the opamp inputs as described in Sec. 2.4.

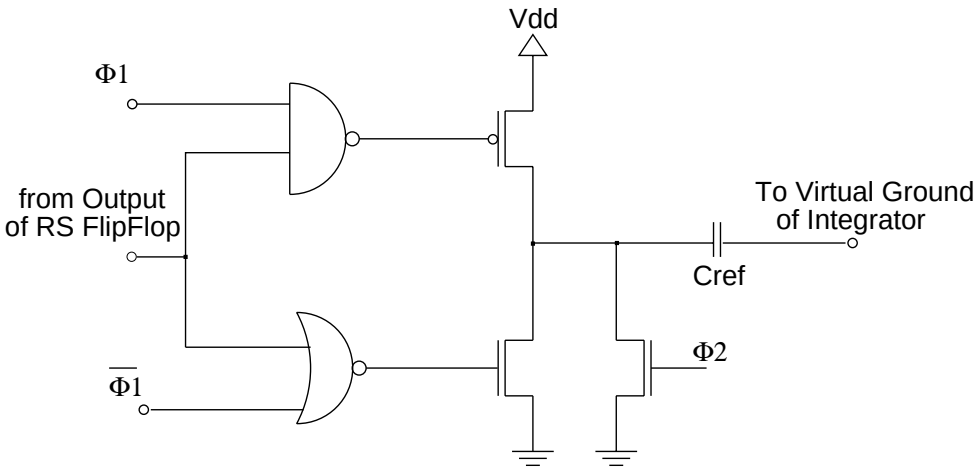

Figure 2.15. Low-voltage DAC feedback branch.

2.8 Low-Voltage Input Sampling Circuit

The input integrator is a special case, since its input capacitor is not connected to the output of a RO. An input stage [2] is used to feed the first integrator of the filter. The input sampling circuit is shown in Fig. 2.16 and is similar to the buffers described in Refs. [2], [27]. It is basically a track-and-reset (T/R) circuit used as an input-sampling switch. During phase Φ_2, it provides the inverted input signal to the input capacitor of the first stage. During phase Φ_1, the opamp is in a unity-gain-reset configuration, providing V_{dd} to the first stage.

Simulation results in the time domain are shown in Figure 2.17.

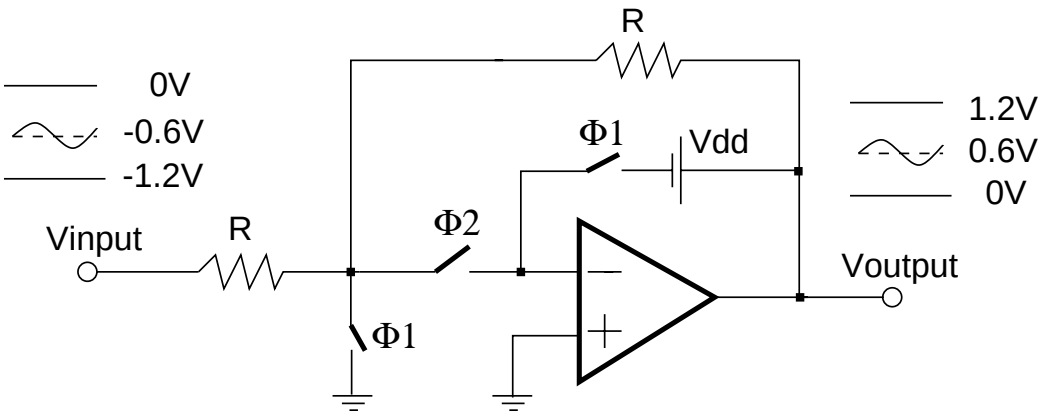

Figure 2.16. LV input sampling circuit.

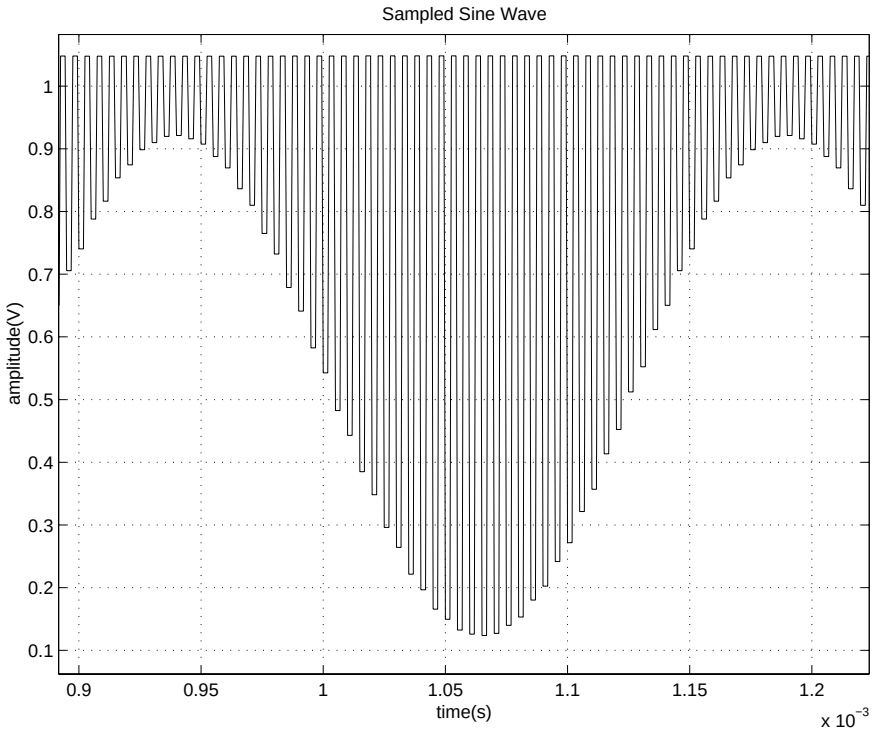

Figure 2.17. Simulated output of the input-sampling circuit.

2.9 Overall circuit diagram

The whole circuit of the $\Delta\Sigma$ modulator is shown in Fig. 2.18, with the CMFB circuits and input buffers omitted for clarity. The double-triangle opamp symbol implies that even if pseudo-differential amplifiers are used, fully-differential symmetry is always maintained both in the circuit design and the chip layout in order to obtain the best performance.

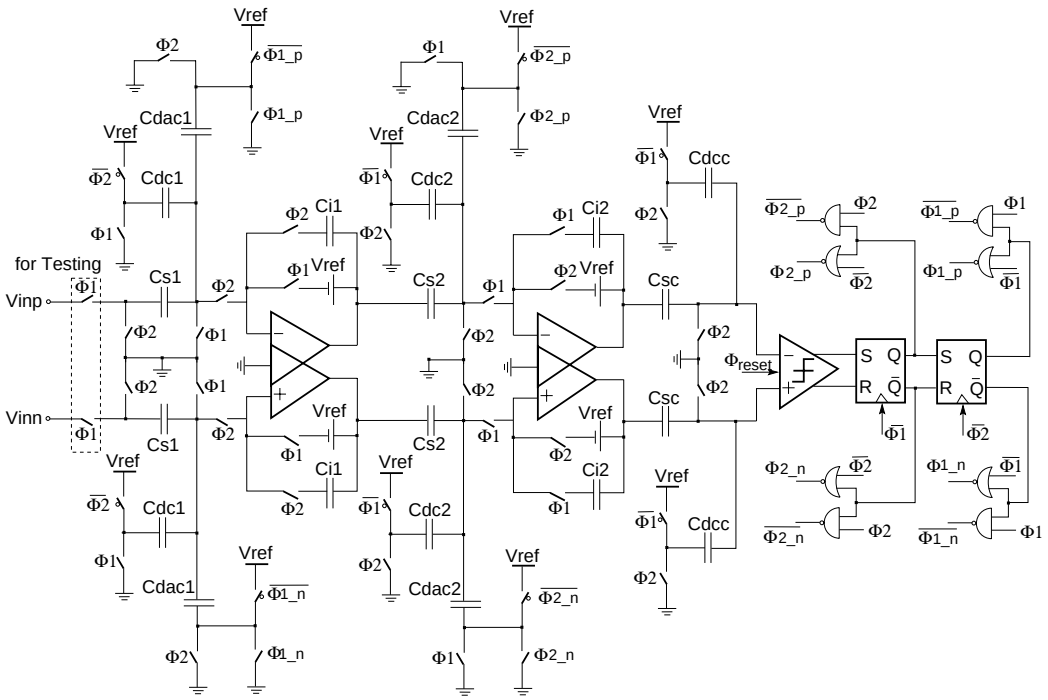

Figure 2.18. LV second-order $\Delta\Sigma$ modulator with CMFB and input sampling circuits are omitted.

2.10 Capacitor Values and Noise Considerations

Thermal noise is generated by the on resistance of the switches and is sampled by the input capacitors of an integrator. The noise is transferred to the integrator output by multiplying it with the particular transfer function from the specific capacitor to the integrating capacitor. The total noise is then calculated at the integrator output. The noise contributions by either the first integrator or second integrator shown in Fig. 2.18 is given by

$$P_{n,C_s} = \frac{2kT}{C_s R}\left(\frac{C_s}{C_i}\right)^2, \tag{2.17}$$

$$P_{n,C_{dac}} = \frac{2kT}{C_{dac} R}\left(\frac{C_{dac}}{C_i}\right)^2, \tag{2.18}$$

$$\text{and} \quad P_{n,C_{dc}} = \frac{2kT}{C_{dc} R}\left(\frac{C_{dc}}{C_i}\right)^2, \tag{2.19}$$

$$\tag{2.20}$$

where R, k, and T are the oversampling ratio, Boltzman constant, and absolute temperature, respectively.

The total noise power is given by

$$P_{n,output} \;=\; P_{n,C_s} \;+\; P_{n,C_{dac}} \;+\; P_{n,C_{dc}}. \tag{2.21}$$

This noise will be divided by the transfer function from output to input in order to calculate the SNR at the input of the modulator:

$$P_{n,input} = \frac{P_{n,output}}{|H|^2} \tag{2.22}$$

$$P_{n,input} = P_{n,output}\left(\frac{C_i}{C_s}\right)^2 = \frac{2kT}{C_s R}\left(1 + \frac{C_{dc}}{C_s} + \frac{C_{dac}}{C_s}\right). \tag{2.23}$$

The noise contribution of the first integrator is the main concern. The noise of the second integrator is first-order shaped when it is referred to the input of the

$\Delta\Sigma$ modulator. The sampling capacitors are chosen to obtain 15 bits of dynamic range performance based on Eqn. 2.23.

The capacitor values are given in Tab. 2.4. The value of the sampling capacitor at the first stage was obtained considering kT/C noise. The other capacitors are scaled accordingly.

Cs1	2 pF	Cs2	0.8 pF	Csc	0.4 pF
Cdac	2 pF	Cdac2	0.4 pF	Cdcc	0.4 pF
Cdc1	1 pF	Cdc2	0.12 pf		
Ci1	8 pF	Ci2	1.6 pF		

Table 2.4. Capacitance values.

2.11 Layout and Floor Plan

Fig. 2.19 shows the die photo of the prototype IC, realized in a 0.35 μm double-poly triple-metal CMOS technology. Digital and analog circuits are separate, with the opamps located at the maximum distance from the digital stages. Well and substrate guard strips and rings were used to shield the sensitive analog elements from substrate noise. By using enable/disable switches, it was possible to allow operation using either the input stage of Fig. 2.16 or a floating input transmission gate at the front-end. This allows for operation even if the actual threshold voltages of the fabricated chip are different from the values used in the simulation. The total chip area (excluding the input buffer) is 0.41 mm^2.

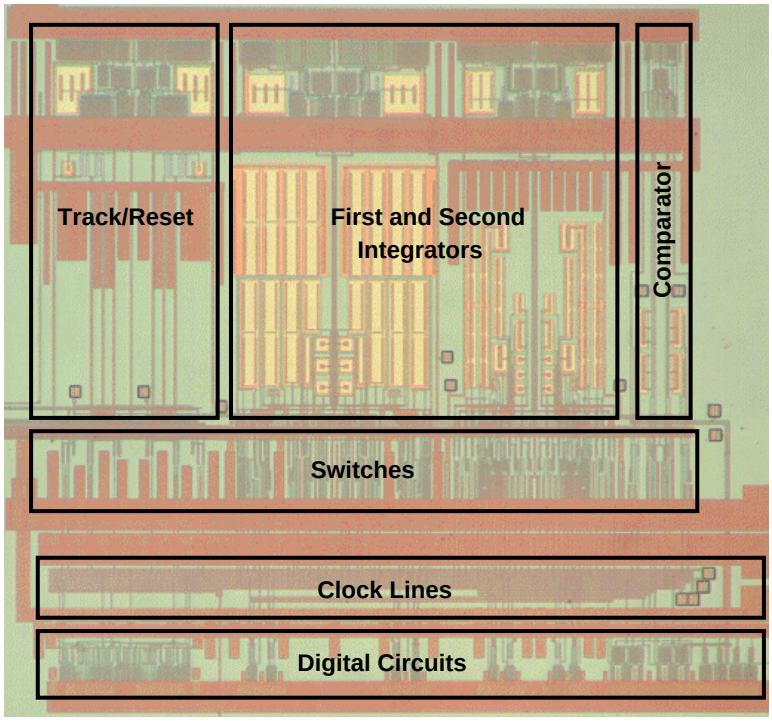

Figure 2.19. LV second-order $\Delta\Sigma$ modulator die photograph.

2.12 Test Setup

The two-layer printed-circuit-board (PCB) was designed to test the chips as shown in Fig. 2.20. Analog ground and digital ground were connected at one point only under the chip. Large (47μF) and small capacitors (0.1μF) are connected from the reference lines to ground in order to filter out power supply noise at the banana connectors. Additional small (0.1μF) capacitors are connected to the voltage reference lines just next to the chip. A high precision differential input test signal was generated by an Audio Precision signal generator. The clock is generated by a HP frequency synthezier. The digital one bit data stream was captured by a Tektronix logic analyzer and the data was transferred to MATLAB for further signal processing analysis. The DC value of the digital bit stream was eliminated and then a hamming window was applied. Finally, SNR, SNDR, and

DR were calculated inside the 20 kHz and 50 kHz band intervals. More analyses were completed in order to observe the chip performance under different conditions such as with different clock-frequencies, supply-voltages, and signal-amplitude variations.

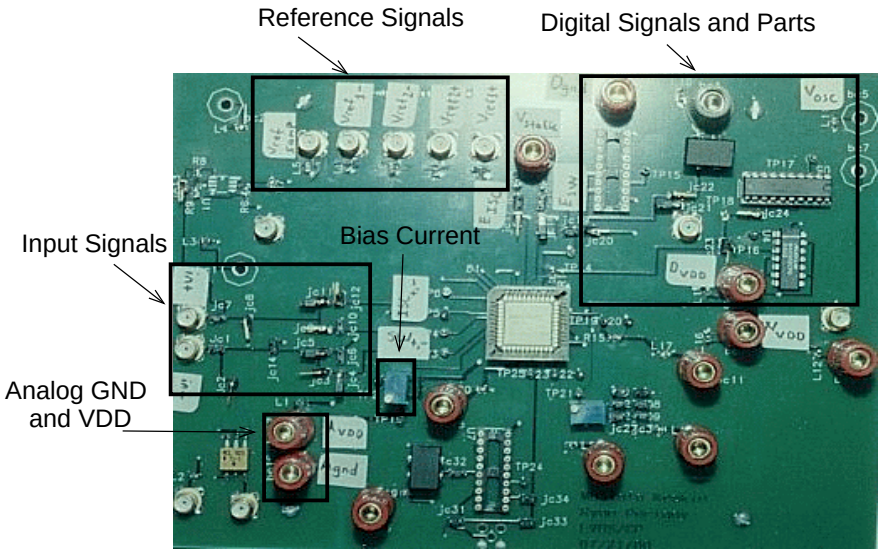

Figure 2.20. Test board for the LV second-order $\Delta\Sigma$ modulator.

2.13 Test Results

A summary of the measured results is shown in Table 2.5. For audio band (300 to 20 kHz) operation, a true 13-bit accuracy resulted. Extending the input frequency range to 300-50 kHz yielding an effective number of bits (ENOB) = 12.5 bits. The chip remained operational down to a 0.95 V supply voltage, but with an ENOB = 10.5 bits.

The fabricated chip was tested with supply voltages varying from 1.05 to 1.2 V and with varying clock frequencies. Results are shown in Fig. 2.21 and Fig. 2.22. The SNDR and SNR vs dynamic range (DR) for a 2.5 kHz input sine wave are shown in Fig. 2.23. A typical measured spectrum of the digital output stream is illustrated in Fig. 2.24 without detectable harmonics.

Signal Bandwidth	20 kHz	50 kHz
Sampling Frequency	10.24 MHz	10.24 MHz
Max. Diff. Input	1.2 Vpp	1.2 Vpp
Dynamic Range	80 dB	74 dB
Peak SNR	78.6 dB	70.6 dB
Peak SNDR	77.8 dB	70.4 dB
Power Consumption	5.6 mW	5.6 mW
Supply Voltage	1.05 V	1.05 V
Chip Core Area	0.41 mm^2	0.41 mm^2
Technology	0.35 μm	0.35 μm

Table 2.5. Measured performance of the second-order $\Delta\Sigma$ ADC.

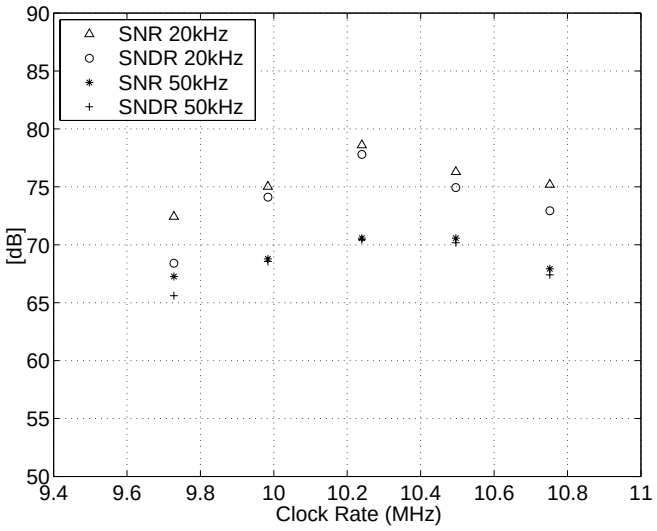

Figure 2.21. SNR and SNDR variations with different clock frequencies.

Threshold voltages differed from the simulation models to the actual chips. The simulation models assumed $V_{thn} = 0.55$ V and $|V_{thp}| = 0.55$ V, while for the actual chips V_{thn} ranged from 0.486 V to 0.563 V, and $|V_{thp}|$ from 0.422 V

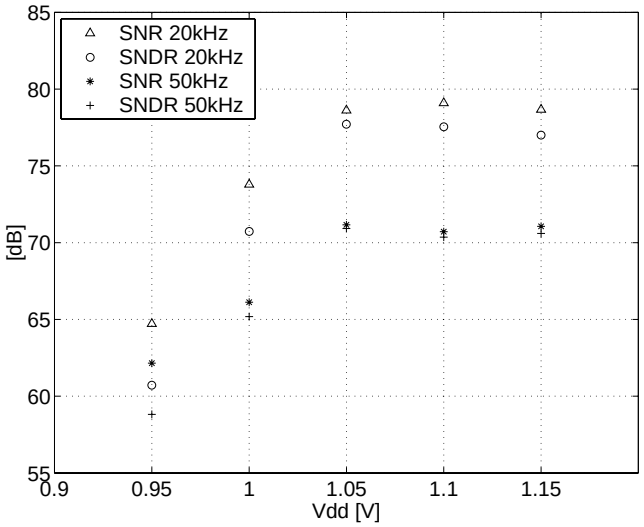

Figure 2.22. SNR and SNDR variations with different supply voltages.

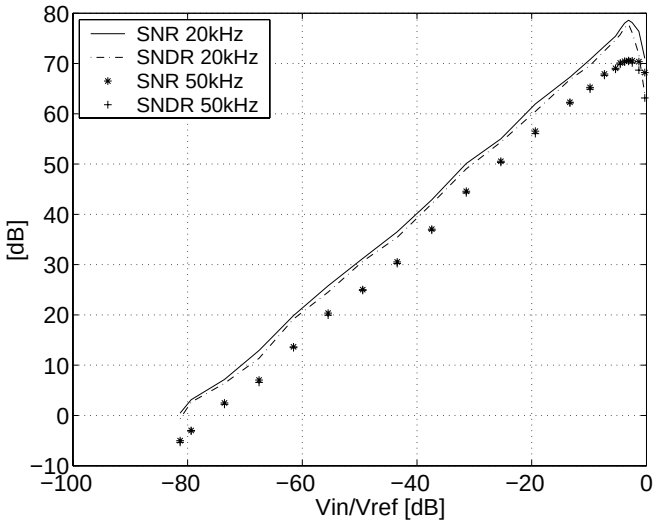

Figure 2.23. SNR and SNDR for 20 kHz and 50 kHz bandwidths.

to 0.486 V. Some chips had low-threshold voltages, which allowed activation of the floating input switch. The chips with high threshold devices required that the input buffer had to be used. Performance did not vary significantly between these two modes of operation.

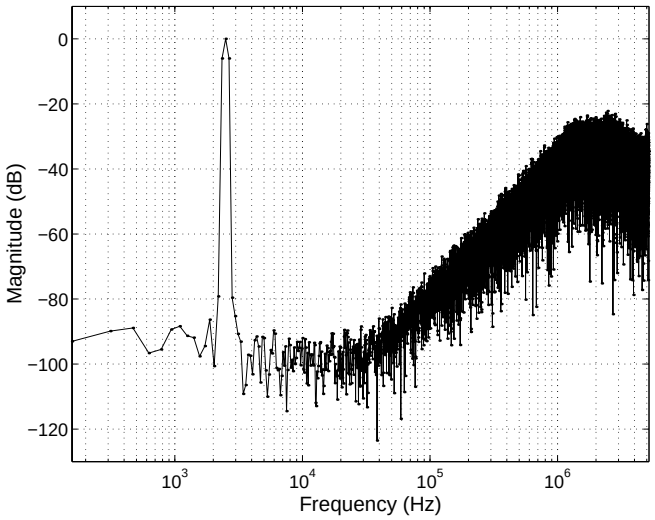

Figure 2.24. Spectrum of the digital output bit stream.

2.14 Conclusions

A low-voltage, high clock-frequency, delta-sigma ADC was designed, fabricated, and tested. This design uses unity-gain-reset opamps, which do not require the turning on and off associated with switched-opamps. Test results indicate that this circuit architecture is suitable for high-speed high-accuracy operation with only 1 V or lower supply voltages. Expected dynamic range and peak SNR are about 90 dB from simulations. However, these values were measured to be approximately 80 dB. These discrepancies may be due to more digital noise coupling and reference voltage variations than accounted for in the simulations. These novel integrators can be used as the main blocks of future SC circuits and systems with low supply voltages. The speed of these integrators is also better than existing switched-opamp integrators. Hence, higher SNR and DR can be obtained with lower orders and higher clock frequencies.

CHAPTER 3
SWITCHED CAPACITOR RESONATORS

3.1 Introduction

Bandpass analog-to-digital-converters (ADCs) are among the key circuit blocks in wireless communication systems. They are used to digitize the received analog signal at an intermediate center frequency. Such converters are used for digital FM or AM radio applications and in portable communication devices, such as cellular phones. The main circuit block in these converters is the resonator, which is tuned to a particular frequency. A resonator must be designed such that it has a sharp resonant peak at a specific center frequency. However, because of physical circuit imperfections, the resonance peak gain and/or the center frequency are degraded in existing architectures.

There exist many resonator circuits to implement SC bandpass $\Delta\Sigma$ modulators and filters for high-frequency communication applications, such as : the 'lossless-discrete integrator' (LDI) and 'forward-Euler' (FE) types [28, 48, 16, 38], 'two-delay loop' (TDL) [37, 7], low-pass filter [49], high-pass filter based [42] and 'pseudo-two-path' (P2P) type [36]. The most recent ones use P2P and TDL techniques, with double sampling to increase the sampling frequency. In these previous implementations, the minimum available power supply voltage was 3 V. Very recent publication has showed the functionality of a second-order SC bandpass $\Delta\Sigma$ modulator with a 1 V supply voltage [13].

In this chapter, five different resonators are analyzed based on finite opamp gain and bandwidth. Simulation results are also shown.

3.2 Analog Circuit Imperfections in Resonators

The typical resonator transfer function with unit delay from input to output is given by

$$H(z) = \frac{z^{-1}}{1 + z^{-2}}. \tag{3.1}$$

This corresponds to the time-domain relation

$$v_{out}(n) = v_{in}(n-1) - v_{out}(n-2) \tag{3.2}$$

which involves a delay by $2T$ and an inversion of v_{out}.

There are two basic requirements for high-accuracy charge transfer using an opamp. First, one must allocate enough time to ensure that both capacitor voltages are settled to the desired accuracy level. Second, the opamp must have enough gain in order to steer the charges in the desired direction and to act as a linear voltage source. Therefore, ideally, the gain of the opamp, A_{dc}, from its input to its output should be infinite, as well as its bandwidth (f_u) in order to have the charge transferred perfectly. In reality, it is impossible to obtain these conditions. Hence, opamps are designed to meet required specifications. It is possible to over design opamps to maximize these parameters, but this is not advisable due to power consumption issues.

The ideal transfer function given in Eqn. 3.1 can be modified to reflect these practical nonidealities, yielding

$$H(z) = \frac{z^{-1}}{(1-a) + bz^{-1} + (1-c)z^{-2}}. \tag{3.3}$$

The peak gain is reduced due to the error terms a and c and the shift in center frequency is introduced by the error term b. The effects of these terms are separately shown in Fig. 3.1, Fig. 3.2, and Fig. 3.3.

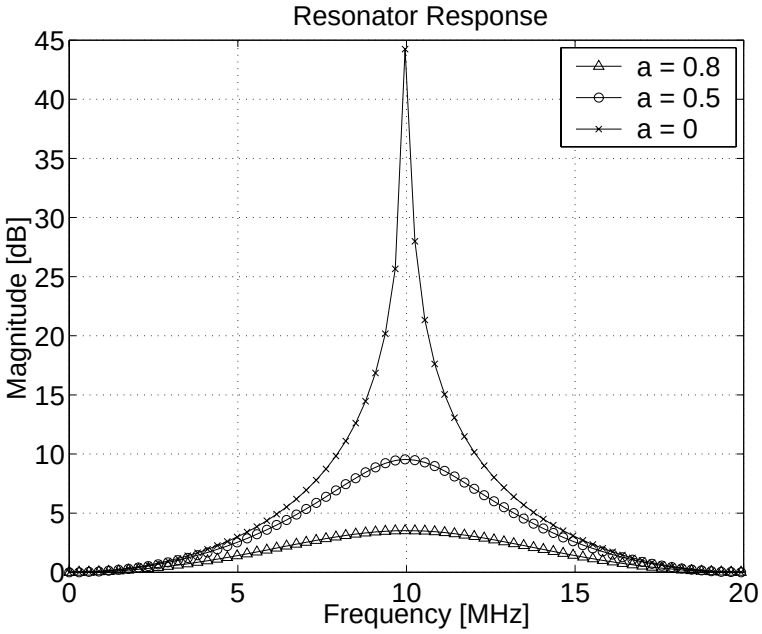

Figure 3.1. Simulation results with different values of error term 'a'.

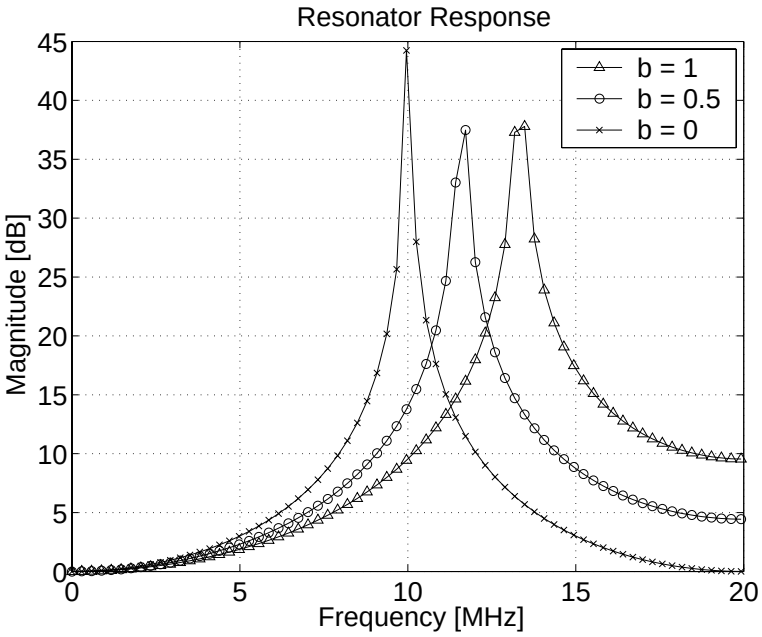

Figure 3.2. Simulation results with different values of error term 'b'.

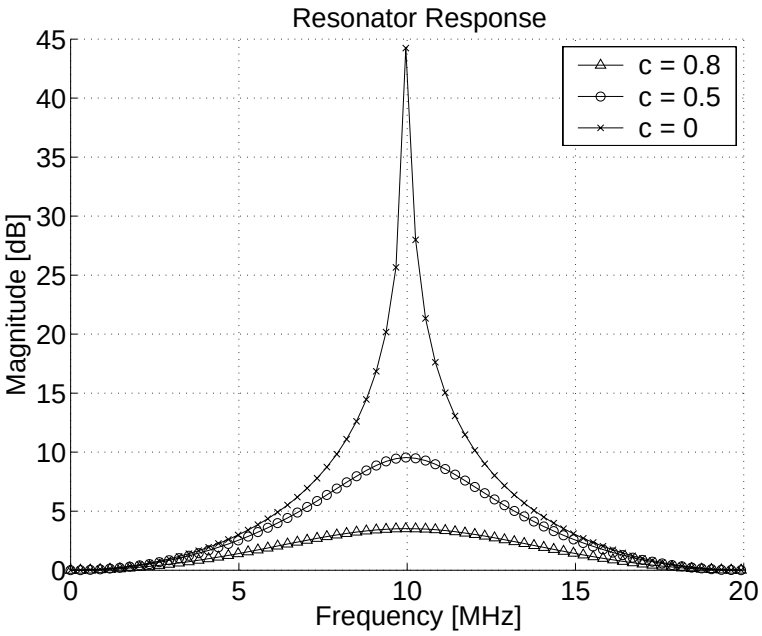

Figure 3.3. Simulation results with different values of error term 'c'.

We discuss finite gain and bandwidth effects in detail in the following sections for the the LDI, TDL, P2P, I2P, and DCT-PNP resonators.

3.3 Lossless Discrete Integrator Type Resonator

A lossless-discrete integrator (LDI) resonator, implemented with two cascaded half-delay integrators in a positive feedback loop, is shown in Fig. 3.4. The circuit is shown in a single-ended configuration for illustration purpose only, it will usually be fully- or pseudo-differential when realized.

An integrator with nonideal conditions will be analyzed next since an integrator is the basic block of the LDI resonator.

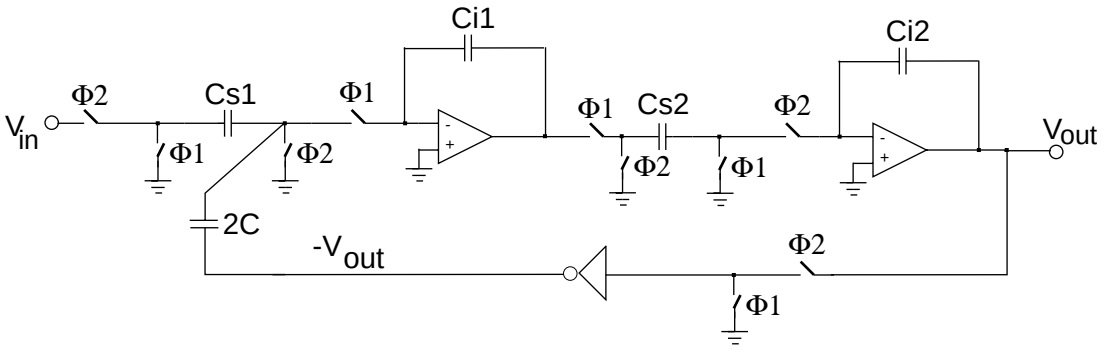

Figure 3.4. Single-ended low-voltage LDI resonator

3.3.1 Analog Imperfections in a Lossless-Discrete-Integrator

In the presence of finite operational amplifier gain (A_{dc}), the half-delay SC integrator will have the transfer function

$$H(z) = m\frac{z^{-1/2}}{1 - p \cdot z^{-1}} \tag{3.4}$$

where m is the actual integrator gain and p is the shifted pole. These coefficients are given by

$$m = \frac{(\frac{C_s}{C_i})}{1 + \frac{1}{A_{dc}}(1 + (\frac{C_s}{C_i}))} \quad \text{and} \quad p = \frac{1 + \frac{1}{A_{dc}}}{1 + \frac{1}{A_{dc}}(1 + \frac{C_s}{C_i})} \tag{3.5}$$

where C_s and C_i are the sampling and integrating capacitors of the integrator, respectively, and A_{dc} is the DC gain of the opamp used.

The finite bandwidth of an operational amplifier introduces a gain error in an ordinary integrator, making the transfer function:

$$H(z) = \frac{C_s}{C_I}(1 - g)\frac{z^{-1/2}}{1 - z^{-1}} \tag{3.6}$$

where the gain error term is $g = e^{-T/\tau}$, and τ is the settling time constant.

The analysis can be easily performed by utilizing the signal-flow-graph method. Fig. 3.5 shows the error terms caused by the effects mentioned above.

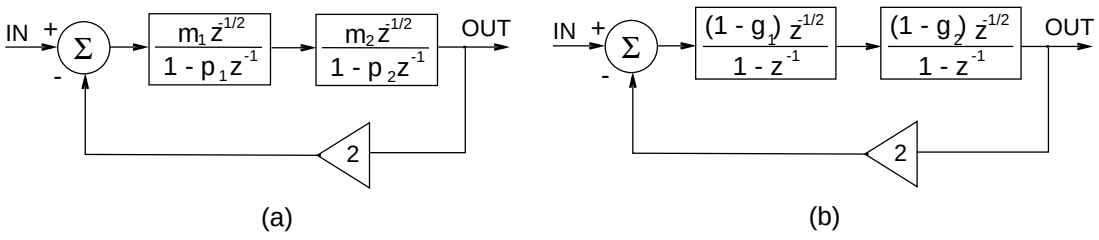

Figure 3.5. Signal-Flow-Graph diagrams of an LDI resonator including error terms caused by (a) finite opamp-gain (b) finite opamp-bandwidth.

3.3.2 Finite Opamp Gain Effects for LDI Resonators

The effect of the finite opamp gain is severe with LDI resonator circuits. The resonator shown in Fig. 3.4 not only suffers from gain error but also from a center frequency shift making the overall transfer function

$$H(z) = \frac{(m_1 m_2)z^{-1}}{1 + (2m_1 m_2 - p_1 - p_2)z^{-1} + (p_1 p_2)z^{-2}} \tag{3.7}$$

where m_1 and p_1 refer to the first integrator and m_2 and p_2 refer to the second integrator. There is z^{-1} term in denominator of this transfer function, that will shift out-of-band noise into the signal band in the context of bandpass $\Delta\Sigma$ modulator. At the same time, the coefficient of the z^{-2} term is equal to $(p_1 p_2)$ instead of "1" as for the ideal case. Therefore, a gain reduction will also be introduced.

3.3.3 Finite Opamp-Bandwidth Effects for LDI Resonators

The effects of the finite bandwidth are included in the transfer function

$$H(z) = \frac{G(1 + g_1 g_2 - g_1 - g_2)z^{-1}}{1 - (2g_1 + 2g_2 - 2g_1 g_2)z^{-1} + z^{-2}}. \tag{3.8}$$

Limited bandwidth shifts the center frequency. At the same time, it sets an upper limit on the sampling frequency, because g increases with it and severely affects the shift. An LDI resonator was simulated in SWITCAP with different DC

gains and bandwidths for f_s=40 MHz. The simulation results show the serious effects of these parameters on this type of resonators in Fig. 3.6.

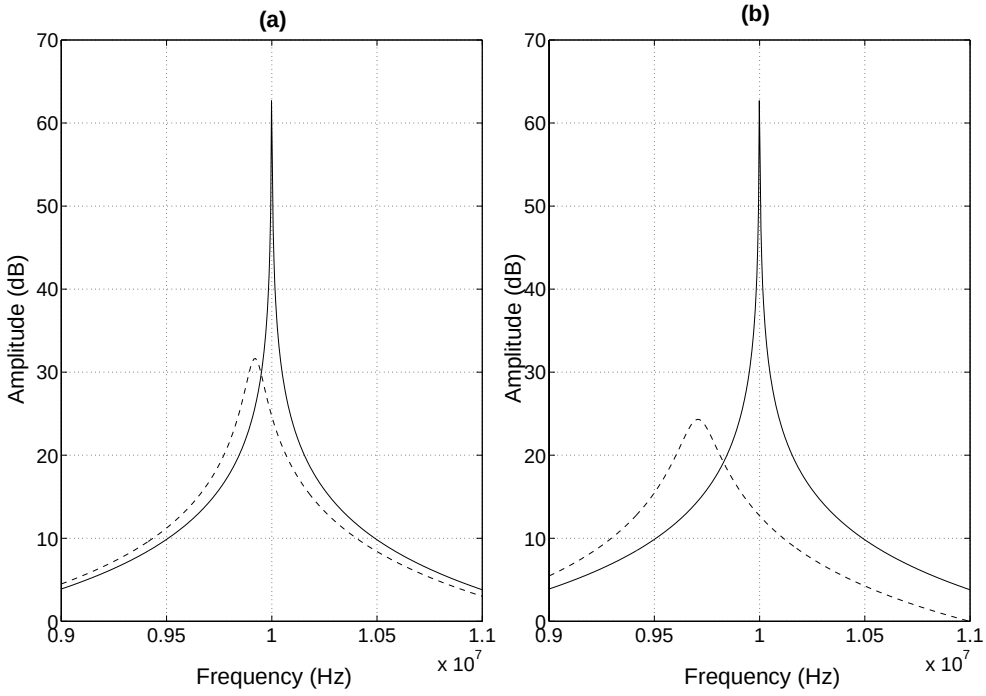

Figure 3.6. SWITCAP simulation results of an LDI resonator with f_{clock}=40 MHz (a) for different opamp DC gains: A_{dc}=120 dB (continuous line), 50 dB (dashed) (b) for different opamp bandwidths: $f_u = \infty$ (continuous line), f_u=160 MHz (dashed).

3.4 Two-Delay-Loop Resonators

The two-delay-loop (TDL) resonator is preferred over LDI resonator because of its relaxed settling time requirements [37, 7]. The TDL resonator architecture is shown in Fig. 3.7. In this circuit, a half-clock-cycle ($T/2$) delay is provided by the sample-and-hold (S/H) circuit. Hence, a full clock-cycle (T) delay is introduced by the two cascaded S/Hs in the forward path. To insure the resonator operation, the feedback capacitors C_{f1} and C_{f2} alternately keep the charge for a full clock cycle, and hence add a full clock delay in the feedback path.

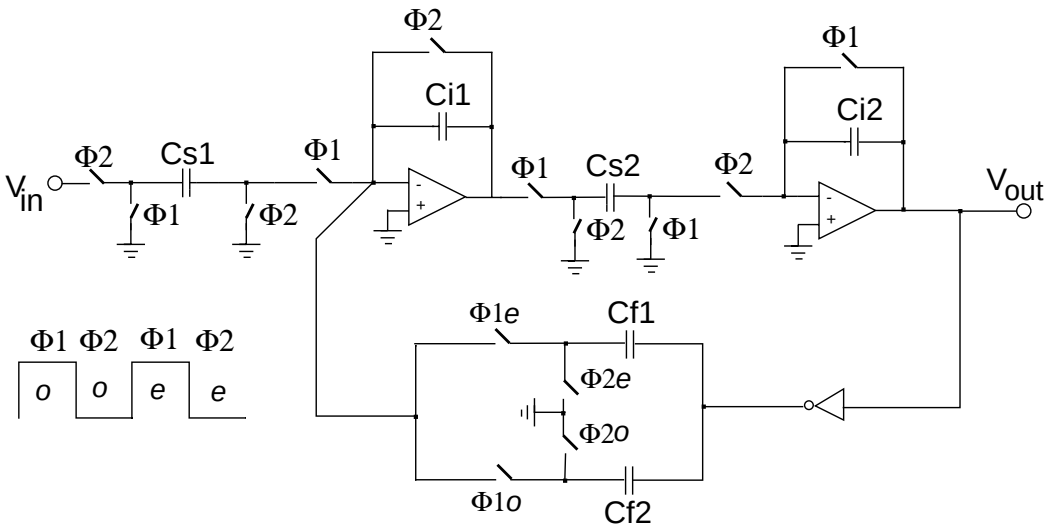

Figure 3.7. A single-ended TDL resonator.

3.4.1 Analog Imperfections in a Delay Circuit

In the presence of finite opamp gain (A_{dc}), the half-delay SC circuit will have the transfer function:

$$H(z) = mz^{-1/2} \tag{3.9}$$

where m is the actual gain of the half-delay cell and is given by

$$m = \frac{(\frac{C_s}{C_i})}{1 + \frac{1}{A_{dc}}(1 + (\frac{C_s}{C_i}))} \tag{3.10}$$

where A_{dc} is the DC gain of the opamp used, C_s and C_i are the sampling and integrating capacitors of the delay cell, respectively. The error term (m) of the LDI and the delay cell are the same. There is no pole error in a delay.

The finite bandwidth of an operational amplifier introduces a gain error in a delay cell

$$H(z) = \frac{C_s}{C_I}(1 - g)z^{-1/2} \tag{3.11}$$

where the gain error term is $g = e^{-T/\tau}$, and τ is the settling time constant. Fig. 3.8 shows signal-flow-graph of the TDL resonator with the error terms caused by these effects.

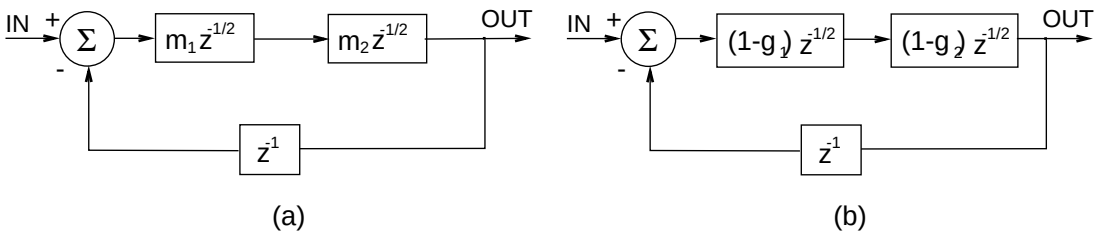

Figure 3.8. Signal-Flow-Graph diagrams of the TDL resonator with error terms caused by (a) finite opamp-gain and (b) finite opamp-bandwidth.

3.4.2 Finite Opamp Gain Effects of TDL Resonators

The finite opamp gain of the TDL resonator only introduces gain error at the resonance peak. This transfer function with error terms is

$$H(z) = \frac{(m_1 m_2)z^{-1}}{1 + (m_1 m_2)z^{-2}} \tag{3.12}$$

where m_1 refers to the first delay cell error and m_2 refers to the second delay cell error.

There is no center frequency shift in TDL resonators. The coefficient of the z^{-2} term is equal to $(m_1 m_2)$ instead of "1" as for the ideal case. Therefore, a gain drop will be introduced.

3.4.3 Finite Opamp Bandwidth Effects for TDL Resonators

The effect of finite opamp bandwidth can be calculated using the diagram in Fig. 3.8(b). The transfer function becomes

$$H(z) = \frac{(1 + g_1 g_2 - g_1 - g_2)z^{-1}}{1 + (1 + g_1 g_2 - g_1 - g_2)z^{-2}} \tag{3.13}$$

Limited opamp bandwidth causes similar results to those of limited gain. The TDL resonator was simulated in SWITCAP for different DC gains and bandwidths. Simulation results show these effects for f_s=40 MHz in Fig. 3.9.

As also shown in the simulation results, the z^{-1} term in the denominator of the transfer function is eliminated. Hence, due to second-order effects, there is very little shift in the center frequency location. On the other hand, the resonant gain is degraded by almost 36 dB. This configuration requires opamps with high DC gain since the opamps are used as buffers.

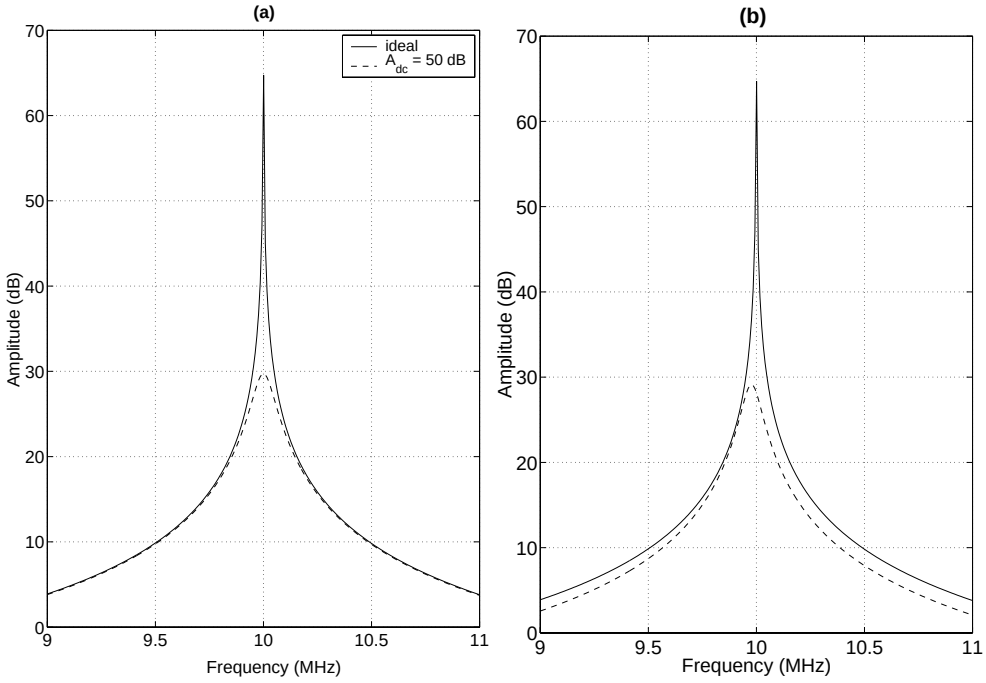

Figure 3.9. Simulation results of the TDL resonator from SWITCAP with f_{clock}=40 MHz (a) for different opamp DC gains: A_{dc}=120 dB (continuous line), 50 dB (dashed); (b) for different opamp bandwidths: $f_u = \infty$ (continuous line), f_u=160 MHz (dashed).

3.5 Pseudo-N-Path Resonators

N-path filters ideally have passbands centered at frequencies determined by the clock rate and the circuit structure rather than by component values. This allows the realization of narrow-band filters with very low sensitivity to component value variations. Unfortunately, clock feedthrough and path mismatch in these circuits will cause spectral tones located at the center of the passband. To eliminate this effect, pseudo-N-path (PNP) SC filters have been proposed [26, 9, 19, 56]. In some PNP filters, each path charge follows exactly the same route through the circuit, hence there cannot exist any path asymmetry. A charge-mode PNP resonator is shown in Fig. 3.10 [26, 9, 36],

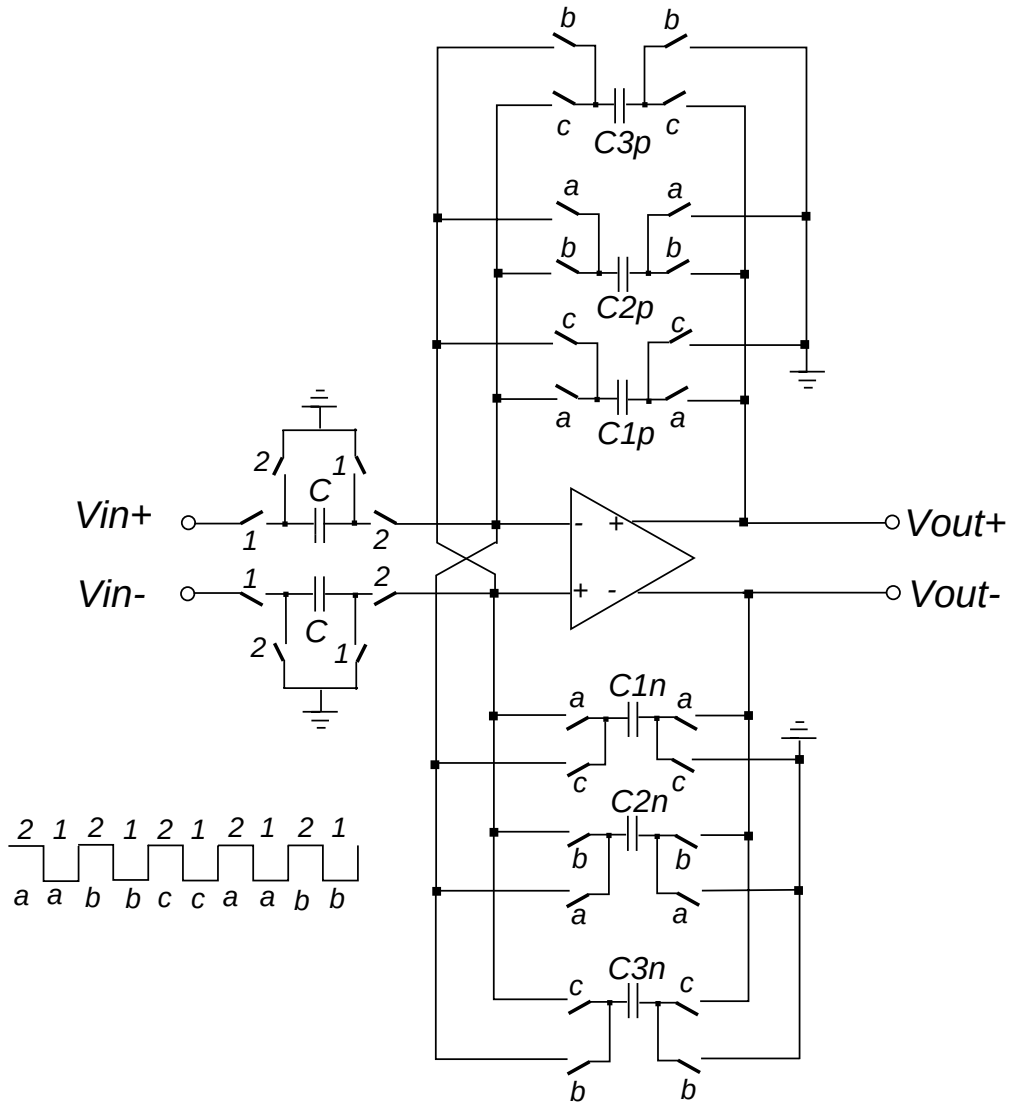

Figure 3.10. Charge-mode pseudo-N-path SC circuit.

In this structure, the differential output voltage is provided by two capacitors, say $C1p$ and $C1n$ during clock phase 'a'. This output voltage is stored on the same capacitors for two clock periods. Then $C1p$ and $C1n$ are interchanged, and they transfer their charges to the new feedback capacitors, $C3p$ and $C3n$ during clock phase 'c'. This operation provides the delayed output as a charge.

3.5.1 Finite Opamp-Gain Effects for PNP Resonators

With this resonator, the analysis is performed in the time domain first. The equation is then converted to the z-domain in Eqn. 3.14. Fig. 3.11 shows the P2P architecture during phase 'a'.

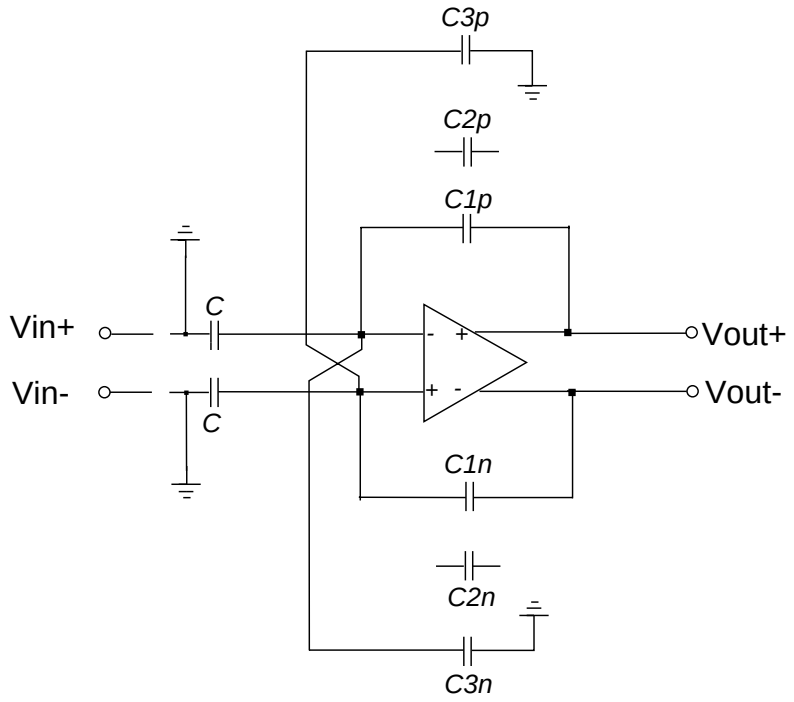

Figure 3.11. Charge-mode pseudo-N-path SC circuit during phase 'a'.

For a finite opamp gain A_{dc}, charge conservation gives

$$C1\Big(V_o(n)+\frac{V_o(n)}{A_{dc}}\Big)=-C1\frac{V_o(n-1)}{A_{dc}}+C3\Big(-V_o(n-2)-\frac{V_o(n-2)}{A_{dc}}\Big) \\ -C1\frac{V_o(n)}{A_{dc}}+C\Big(V_{in}(n-1/2)-\frac{V_o(n)}{A_{dc}}\Big). \quad (3.14)$$

Ideally, $C1$ is equal to $C2$ and $C3$. For simplicity, they will be denoted by Ci. Then, from Eqn.3.14,

$$V_o(z)\Big(1+\frac{2+C/C_i}{A_{dc}}+\frac{z^{-1}}{A_{dc}}+\frac{(A_{dc}+1)\cdot z^{-2}}{A_{dc}}\Big)=\frac{C}{C_i}V_{in}(z)\cdot z^{-1/2} \quad (3.15)$$

$$H(z) = \frac{C/C_i \cdot A_{dc} \cdot m \cdot z^{-1/2}}{1 + m \cdot z^{-1} + (1 + A_{dc}) \cdot m \cdot z^{-2}} \tag{3.16}$$

where error term m is equal to

$$m = \frac{1}{2 + A_{dc} + C/C_i}. \tag{3.17}$$

As seen from the above, there is both a center frequency shift and a resonance gain loss in the PNP resonator architecture due to the circuit imperfections.

3.5.2 Finite Opamp-Bandwidth Effects for PNP Resonators

The finite bandwidth effects of the opamp can also be calculated using time-domain equations. Incomplete linear settling can be modelled by multiplying the input charges by $(1 - g)$, where the gain error term is $g = e^{-T/\tau}$, and τ is the settling time constant. Also, there is some charge kept by the $C1$ capacitors from one clock cycle before due to incomplete settling. The time-domain equation is

$$C1 \cdot V_o(n) = (1-g)\Big(C \cdot V_{in}(n-1/2) - C3 \cdot V_o(n-2)\Big) - g \cdot C1 \cdot V_o(n-1). \tag{3.18}$$

When $C3$ and $C1$ are replaced by C_i, the equation can be written in the s domain as

$$C_i \cdot V_o(z)\Big(1 + (1-g) \cdot \frac{C}{C_i} z^{-2} + g \cdot z^{-1}\Big) = (1-g) \cdot C \cdot V_{in}(z) \cdot z^{-1/2}. \tag{3.19}$$

The transfer function becomes

$$H(z) = \frac{C}{C_i} \frac{(1-g) \cdot z^{-1/2}}{1 + g \cdot z^{-1} + (C/C_i) \cdot (1-g) \cdot z^{-2}} \tag{3.20}$$

where the gain error term is $g = e^{-T/\tau}$, and τ is the settling time constant. Hence, there is both gain loss and center frequency shift in the PNP resonator when the finite-bandwith of the opamp is considered. SWITCAP simulation results are shown in Fig. 3.12.

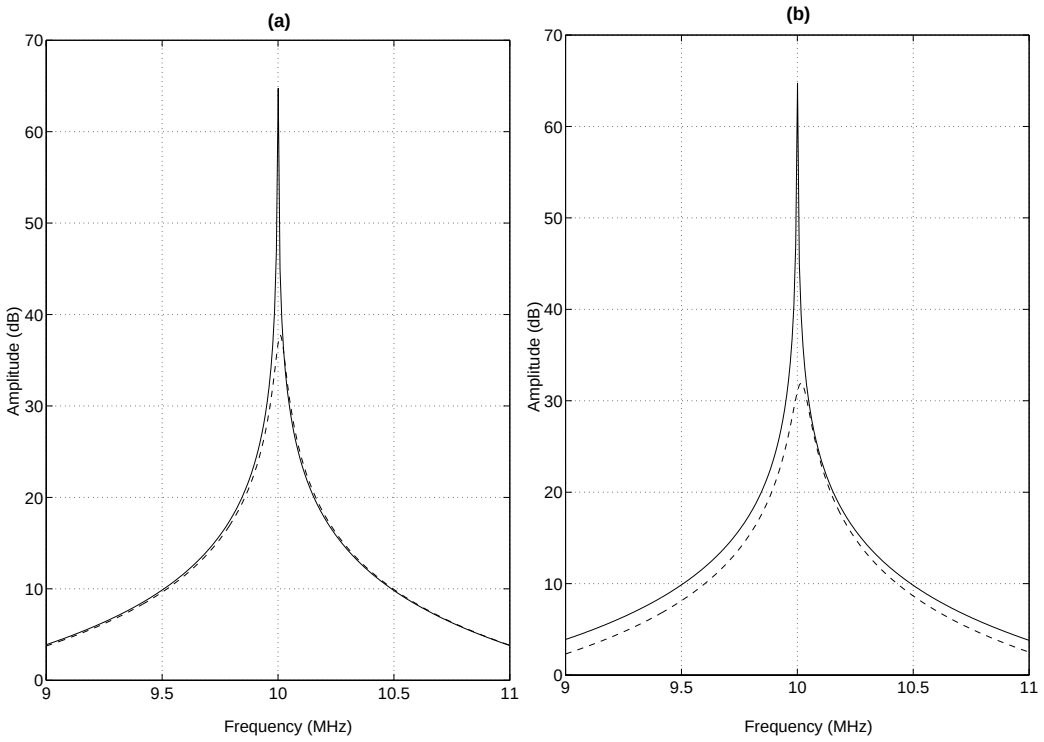

Figure 3.12. Simulation results of PNP resonator from SWITCAP with f_{clock}=40 MHz (a) for different opamp DC gains: A_{dc}=120 dB (continuous line), A_{dc}=50 dB (dashes); (b) for different opamp bandwidths: f_u=∞ (continuous line), f_u=160 MHz (dashes).

3.6 Integrating-Two-Path Resonators

With the I2P structure [32, 33], the output voltage, which occurs two clock periods earlier, is stored in the C_1 capacitors during odd clock phases as shown in Fig. 3.13. Then, this pair is interchanged in the next clock phase to realize the resonator input-output relation. The same operation is done by the other pair, C_2, in even clock phases. This operation prevents the introduction of odd-order terms into the denominator of H(z), since no error signal delayed by only one clock period can occur.

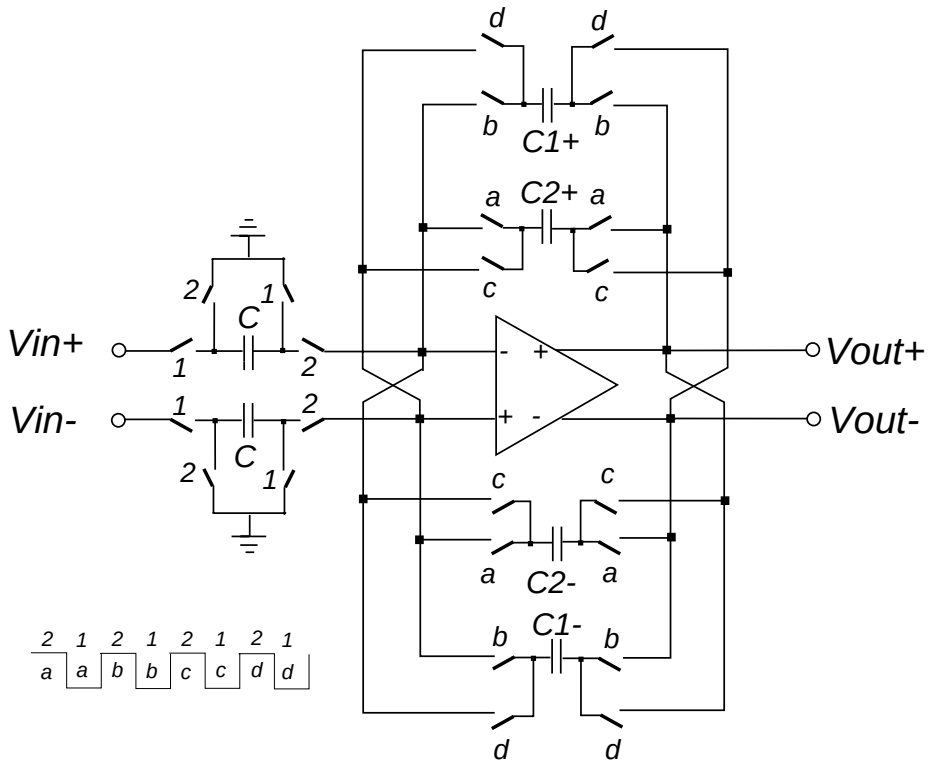

Figure 3.13. Proposed integrating-2-path resonator.

The feedback loop of an I2P resonator is similar to that of a double delayed integrator. Therefore, simple analysis shows that the same error terms as that of the lossless-discrete integrator are included in the transfer function

$$H(z) = m\frac{z^{-1/2}}{1 + pz^{-2}} \tag{3.21}$$

where m is the actual resonator gain and p is the resonant gain error. These error terms are given by

$$m = \frac{(\frac{C_s}{C_i})}{1 + \frac{1}{A_{dc}}(1 + \frac{C_s}{C_i})} \quad \text{and} \quad p = \frac{1 + \frac{1}{A_{dc}}}{1 + \frac{1}{A_{dc}}(1 + \frac{C_s}{C_i})} \tag{3.22}$$

where C_s and C_i are the sampling and feedback capacitors, respectively. C_1 and C_2 are denoted by C_i. The mismatch issues will be explained in Chap. 4.

The finite bandwidth of the operational amplifier introduces a gain error in an I2P resonator. This is reflected in the transfer function

$$H(z) = \frac{C_s}{C_i}(1-g)\frac{z^{-1/2}}{1+z^{-2}} \tag{3.23}$$

where the gain error term is $g = e^{-T/\tau}$, and τ is the settling time constant.

As shown in the SWITCAP simulation results in Fig. 3.14, the integration of the error terms are eliminated. Additionally, this resonator is less sensitive to the opamp imperfections.

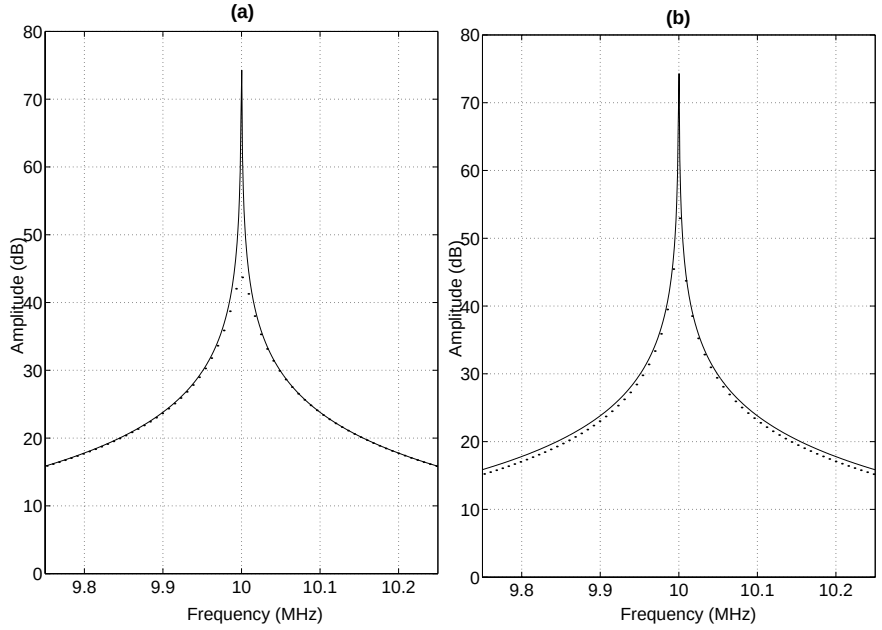

Figure 3.14. Simulation results of an I2P type resonator from SWITCAP2 with f_{clock}=40 MHz (a) for different opamp DC gains: A_{dc}=120 dB (continuous line), A_{dc}=50 dB (dots); (b) for different opamp bandwidths: f_u=∞ (continuous line), f_u=160 MHz (dots).

3.7 Direct-Charge Transfer Pseudo-N-Path Resonator

The proposed new PNP [30] circuit is shown in Fig. 3.15. In this structure, $C1p$ and $C1n$ hold the differential output voltage $v_{out}(n)$ during clock phase 'c'. At the same time, $C3p$ and $C3n$ are connected between the output and the input of the resonator, and hence they are charged to $v_{out}(n) - v_{in}(n)$. Two clock periods later, the $C3$ capacitors are interchanged and connected as feedback capacitors during clock phase 'b', thus providing $v_{out}(n+2)$. There is no center frequency shift because this operation does not integrate any error charge.

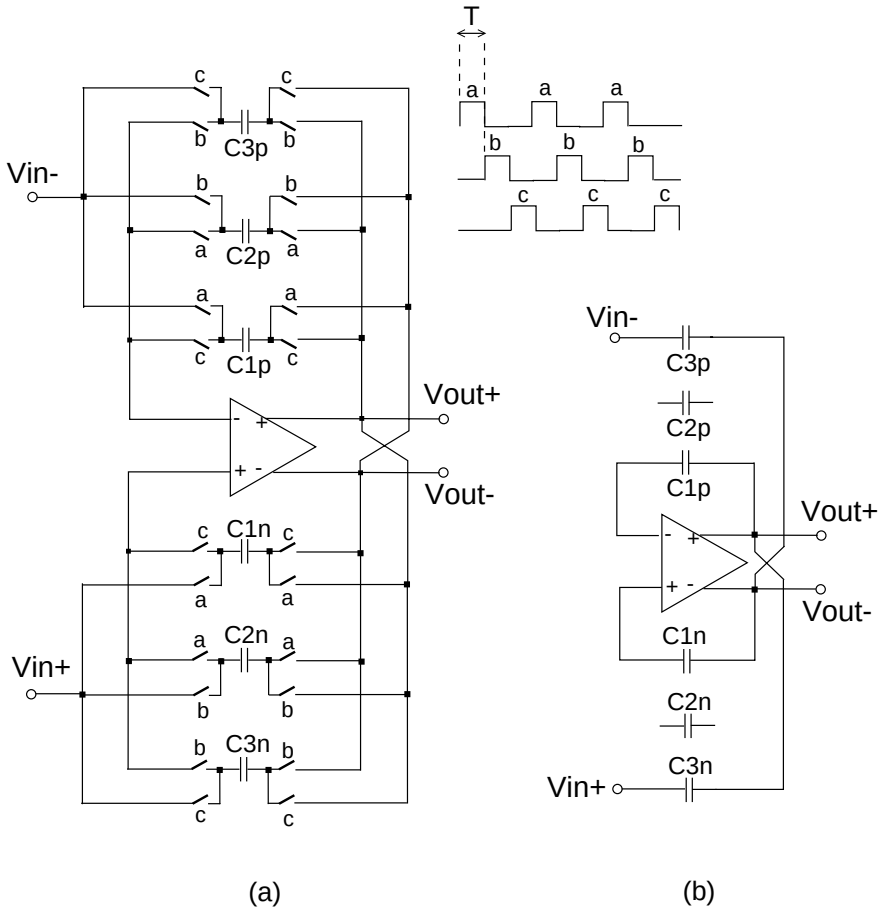

Figure 3.15. The direct-charge-transfer pseudo-N-path SC resonator: (a) circuit diagram; (b) circuit during clock phase 'c'.

In this *direct-charge-transfer (voltage-mode)* pseudo-N-path (DCT-PNP) resonator , there is no charge transfer needed through the virtual ground to realize the resonator transfer function. Therefore, the finite bandwidth of the opamp does not affect the accuracy of the resonating frequency. The finite gain of the opamp will introduce only a reduction of the 'Q' of the resonator as shown by

$$H(z) = \frac{z^{-2}}{1 + (1 - p) \cdot z^{-2}}. \tag{3.24}$$

where p is the resonance gain error and is given by

$$p = \frac{1}{A_{dc}}. \tag{3.25}$$

The DCT-PNP resonator needs opamps with high gain since the opamps are used as voltage buffers.

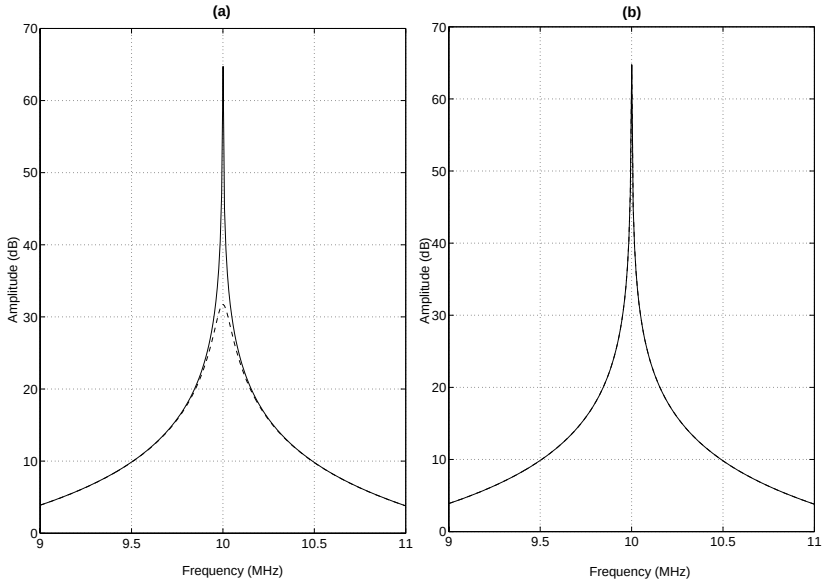

Figure 3.16. Simulation results of DCT-PNP type resonator from SWITCAP with f_{clock}=40 MHz (a) for different opamp DC gains: A_{dc}=120 dB (continuous line), A_{dc}=50 dB (dashes); (b) for different opamp bandwidths: f_u=∞ (continuous line), f_u=160 MHz (dashes).

3.8 Simulation Results:

The performances of I2P and DCT-PNP resonators are compared in Fig. 3.17 and Fig. 3.18 with those of three other well-known SC resonator structures, namely the pseudo-N-path (PNP), the two-delay-loop (TDL), and the lossless-discrete-integrator (LDI). In Fig. 3.17, the peak resonances of five resonators are obtained at 10 MHz for the nearly ideal case where the unity-gain-bandwidth (f_u=∞) and the gain (A_{dc}=120 dB) of the opamp used do not limit the performance.

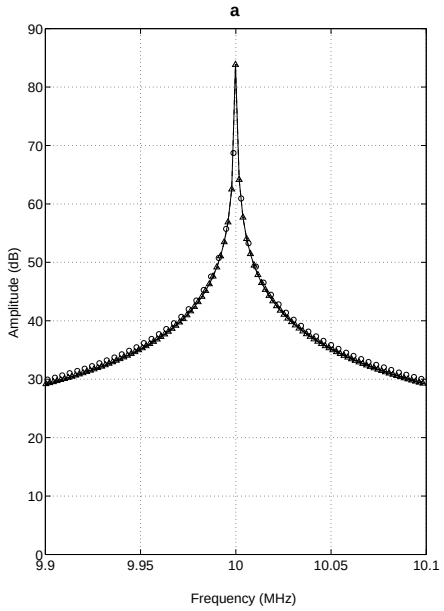

Figure 3.17. SWITCAP simulation results from for I2P (triangles), PNP (dashes), TDL (dots), LDI (circles), and DCT-PNP (continuous line) resonators for A_{dc}=120 dB and $f_u = \infty$.

In Fig. 3.18(b), the effects of the finite gain limitation of the opamp are shown, for $f_u = \infty$ and A_{dc}=60 dB. DCT-PNP and I2P have some gain loss, but less than the other architectures. The PNP circuit exhibits both a gain loss and a frequency shift. The LDI simulation exhibits the worst performance with a serious gain drop and a center frequency shift. The TDL has severe gain loss as

well. In Fig. 3.18(c), the effects of the finite bandwidth limitation of the opamp are shown, for f_u=100 MHz and A_{dc}=120 dB. DCT-PNP has no gain loss or any shift in the center frequency, while the PNP and the TDL have almost 40 dB gain loss. At the same time, the I2P has an 8 dB gain loss. The LDI configuration again exhibits the worst case performance.

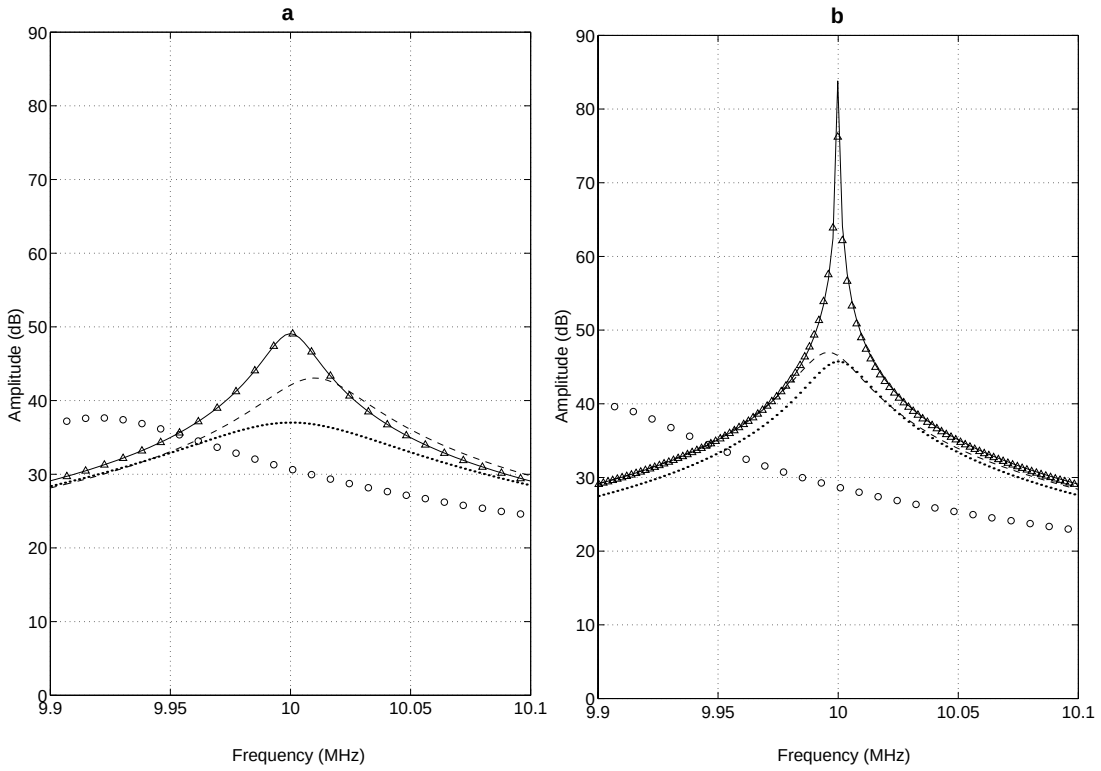

Figure 3.18. SWITCAP simulation results for I2P (triangles), PNP (dashes), TDL (dots), LDI (circles), DCT-PNP (continuous line) resonators for (a) A_{dc} = 60 dB and $f_u = \infty$ (b) A_{dc}=120 dB and f_u =80 MHz.

As seen from the simulations, both of our architectures are very robust with respect to finite gain and finite bandwidth limitations. Their response to the finite bandwidth is particularly excellent. This allows a reduction of f_u, which is an important improvement since it means reducing current consumption, and hence the power consumption, of the circuit.

3.9 Conclusions

There are several drawbacks to the existing SC resonator circuits. First of all, both TDL and LDI resonators need two opamps, since each integrator or delay-cell requires one opamp. Thus, the nonidealities discussed before affect the transfer functions of the SC resonators twice as much as that of the basic SC integrator or delay cell. Additionally, these error terms are integrated over time and multiplied each other.

As seen from both simulation results and analysis, these architectures cannot compensate for the imperfections (errors) originating from the basic blocks. The PNP resonator uses only one opamp; on the other hand it also introduces the integration of error terms.

The other issue is related to the required center frequency for some wireless communication systems. Especially for the SC bandpass converter, the second intermediate frequency (10.7 MHz) of a superheterodyne receiver is difficult to achieve. This makes the SC resonator implementation a very difficult task. The previous architectures would have shown better performances if circuit elements were more nearly ideal. This is not likely to happen in future CMOS technology. Hence, there is strong need for architectures such as ours, which allow relaxed requirements for the circuit components, and enable the production of high quality and robust products for future communication devices.

CHAPTER 4
A LOW-VOLTAGE BANDPASS $\Delta\Sigma$ MODULATOR

4.1 Introduction

The primary motivation for the development of bandpass A/D converters is that they allow for simple and accurate processing of narrow-band signals. Such signal processing is needed for wireless communication systems, spectrum analyzers, and special-purpose instrumentation using narrow frequency-band sources. These are very important for high-volume consumer applications, which are rapidly expanding every year. Since advanced modulation schemes need digitally implemented modem technology, additional applications are emerging for cellular phones and digital audio broadcast.

There are two common methods of A/D conversion used in superheterodyne receivers. One method is to digitize at baseband with lowpass ADCs as shown in Fig. 4.1(a). The other method is to digitize at a certain intermediate frequency (IF) with a bandpass ADC as shown in Fig. 4.1(b).

The bandpass ADC has several advantages over the baseband ADC. Specifically, demodulation is done in the digital domain with perfect gain and phase matching. Secondly, the bandpass A/D converter is insensitive to DC offset and low frequency noise. Thirdly, if a $\Delta\Sigma$ ADC is used for this purpose, then a relatively small bandwidth, compared to its central frequency, allows high level of noise shaping. The design of a LV SC bandpass $\Delta\Sigma$ modulator for digital radio or GSM receiver applications will be discussed in the following sections.

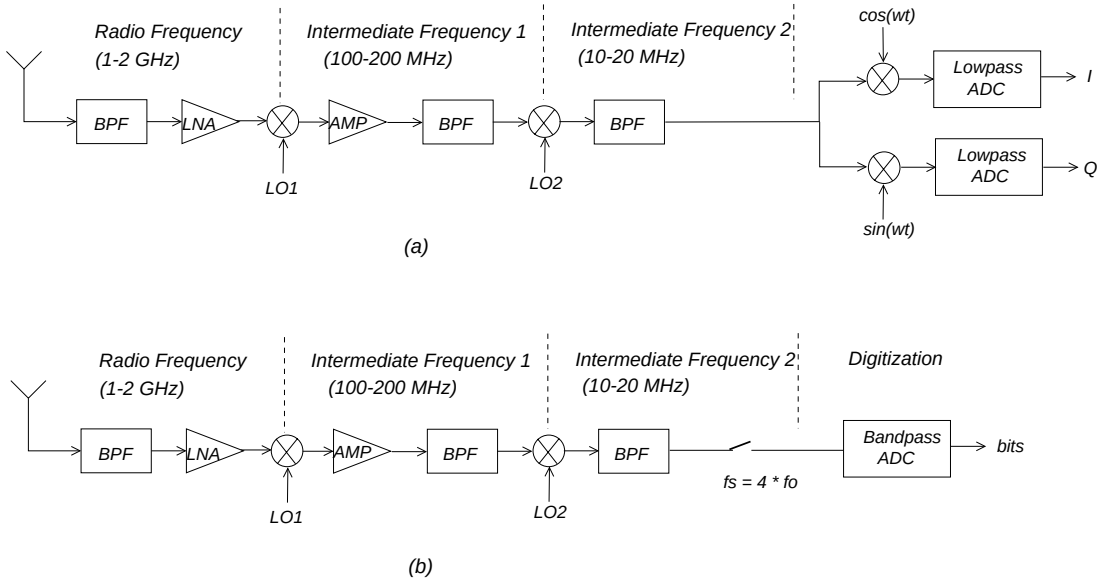

Figure 4.1. Receiver architecture with (a) lowpass and (b) bandpass A/D converters.

4.2 Background and Specifications

The first discrete-time bandpass $\Delta\Sigma$ ADCs have been recently implemented [28]. Table 4.1 summarizes the performance characteristics of state-of-the-art SC bandpass $\Delta\Sigma$ ADCs.

We have previously shown LV implementations of SC ADCs and low-pass filters [10] based on the *Unity-Gain-Reset* (UGR) technique. Compared to the switched-opamp technique [44], the UGR technique is suitable for operating at higher speeds, by keeping the opamp in its active operating region at all times. The following sections will discuss system level issues, a proposed LV UGR resonator circuit, its bandpass $\Delta\Sigma$ implementation, and simulation results.

Ref. index	Order	Area $[mm^2]$	VDD [V]	SNR [dB]	SDR [dB]	PD [mW]	Fclk [MHz]	Fo [MHz]	BW [kHz]
[28]	4^{th}	24.5	+/-5	63	55	480	1.85	0.455	8
[37]	4^{th}	—	5	80	—	—	7.2	1.8	30
[48]	2^{nd}	—	5	57	—	60	42.8	10.7	200
[49]	4^{th}	1	3.3	56	56	0.8	8	2	30
[42]	4^{th}	2.73	3.3	72	70	72	40	20	200
[16]	4^{th}	4.84	+/-2.5	57	—	—	0.8	0.2	2
[16]	6^{th}	—	+/-2.5	80	—	—	0.5	0.125	1
[7]	4^{th}	1.1	3	47	40	65	80	40	1.25 [1]
[38]	8^{th}	1.7	+/-2.5	59	—	157	14.3	10.6	200
[36]	4^{th}	—	3.3	62	—	5.5	5	2.5	30
[14]	2^{nd}	1.3	1	—	42.3	12	21.4	10.7	200
[18]	6^{th}	1	3.3	—	61	76	42.8	10.7	200
[33][2]	$\mathbf{4^{th}}$	**0.88**	**1.2**	**70**	**60**	**7**	**21.4**	**10.7**	**200**

Table 4.1. Performance of state of the art SC bandpass $\Delta\Sigma$ modulators ([1]MHz and [2] expected).

4.3 System Level Design

The bandpass $\Sigma\Delta$ ADC can be easily designed by starting with a lowpass $\Delta\Sigma$ modulator and then performing a lowpass to bandpass transformation. One such transformation is achieved by the following change of variables:

$$z^{-1} \rightarrow -z^{-2}. \tag{4.1}$$

This transformation maps the zeros of the lowpass $\Sigma\Delta$ Modulator to *fs/4* and *3fs/4,* suppressing the quantization noise around those frequencies. Hence, a

fourth-order bandpass $\Sigma\Delta$ modulator is obtained from its second-order lowpass counterpart by applying the above transformation. The resulting transfer function of the bandpass modulator becomes

$$Y(z) = z^{-4}X(z) + (1 + z^{-2})^2 E(z). \tag{4.2}$$

The lowpass [12] and resulting bandpass $\Sigma\Delta$ modulators are shown in Fig. 4.2. One difference is instead of a subtraction, there is an addition on the inner loop. The most important difference is that instead of integrators, there are resonators that realize the loop filters of the bandpass $\Sigma\Delta$ modulators. The frequency spectrum of the digital output bit stream from the bandpass modulator shows the noise shaping at 10-MHz in Fig. 4.3.

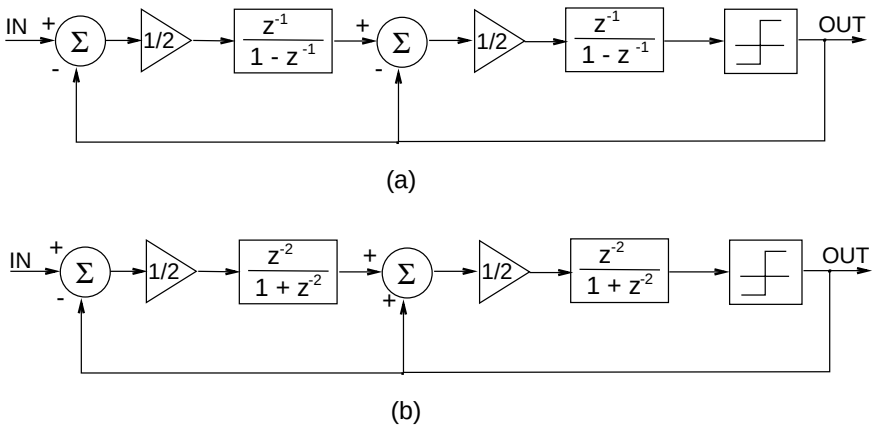

Figure 4.2. Block diagrams of (a) a second order lowpass and (b) a fourth order bandpass $\Delta\Sigma$ modulators.

4.4 Low-Voltage Integrating-Two-Path Resonator

The integrating-two-path (I2P) resonator architecture, already discussed in Sec. 3, in a pseudo-differential configuration for low-voltage operation, [32, 33] is shown in Fig. 4.4. There are two paths from the input to the output in this circuit. The upper two opamps form the first path and one of the pseudo-differential pairs.

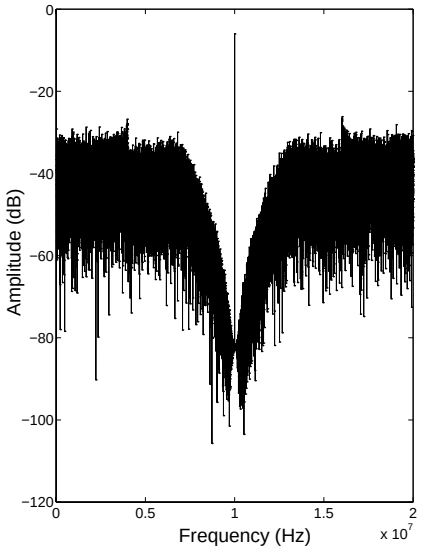

Figure 4.3. Frequency spectrum of a bandpass ΣΔ Modulator from a MATLAB simulation.

The lower two opamps form the second path and the other pseudo-differential pair. The technique used for providing the two clock cycle ($2T$) delay in the previous circuits was to apply positive feedback from the output to the input of a resonator. In all of these circuits, there is charge transferred from the output to the input to realize the resonator transfer function. This charge transfer also integrates some error charges with a delay T. Hence, there is always a z^{-1} term in the denominator of the resonator transfer functions. This creates a center frequency shift of different amounts depending on the particular architecture. These losses are explained in detail in Chap. 3. Additionally, there was severe gain loss in some of the previous implementations.

With this I2P structure, the differential output voltage, delayed by $2T$, is stored in capacitors CA during odd clock phases. Then, the output of the differential pair is commutated to realize the resonator transfer function. The same operation is performed by the other pair containing the CBs in the even clock phases. The commutation operation is done at both the input and the output,

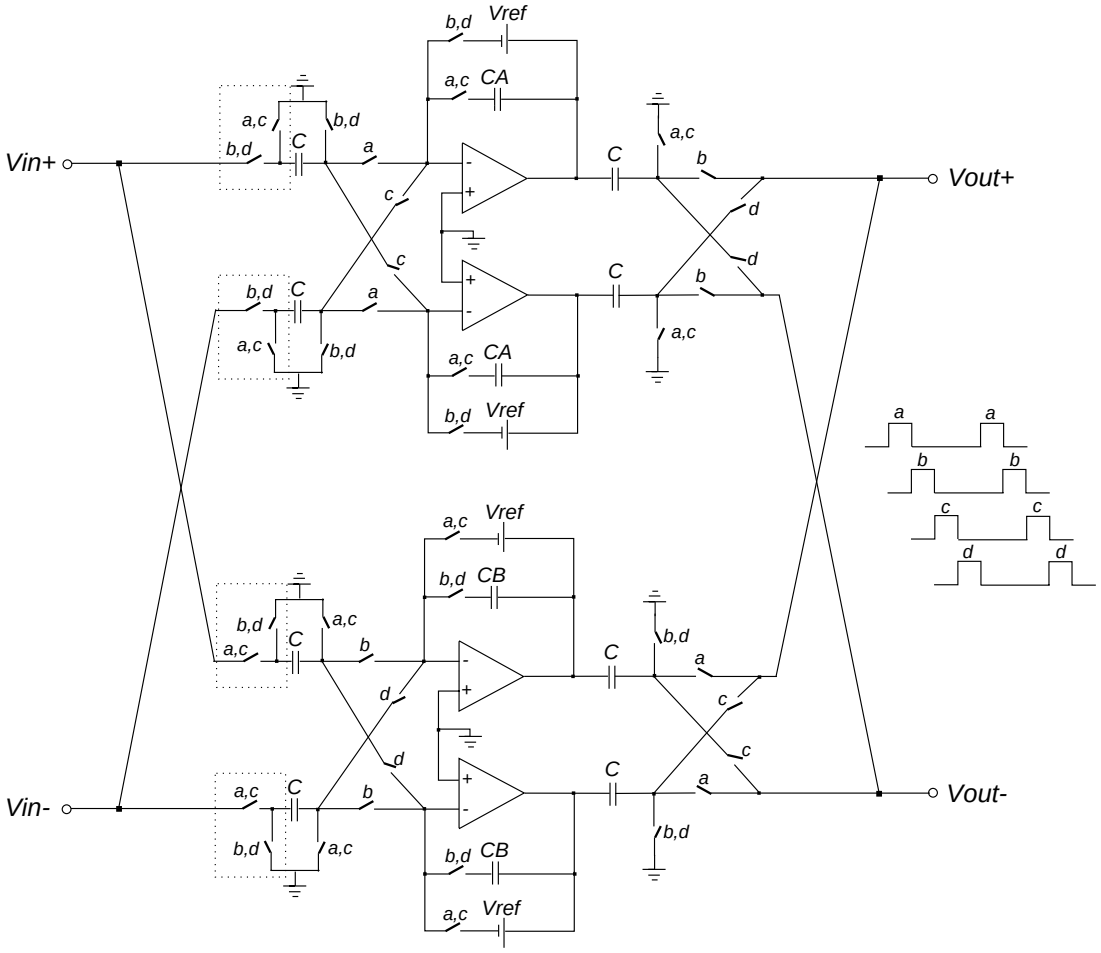

Figure 4.4. The low-voltage I2P resonator.

instead of the feedback branch every second clock cycles, because of the low supply voltage. This will change the sign of the stored voltage on the path and hence effectively introduce positive feedback in the voltage domain.

4.5 Low-Voltage Bandpass $\Delta\Sigma$ Modulator

A fourth-order bandpass $\Delta\Sigma$ modulator using I2P resonators with correlated-double-sampling method is shown in Fig. 4.5. This modulator uses a pseudo-differential configuration for LV operation.

The digital circuit blocks and comparators are omitted for simplicity. The outputs of the upper and lower paths will be interleaved.

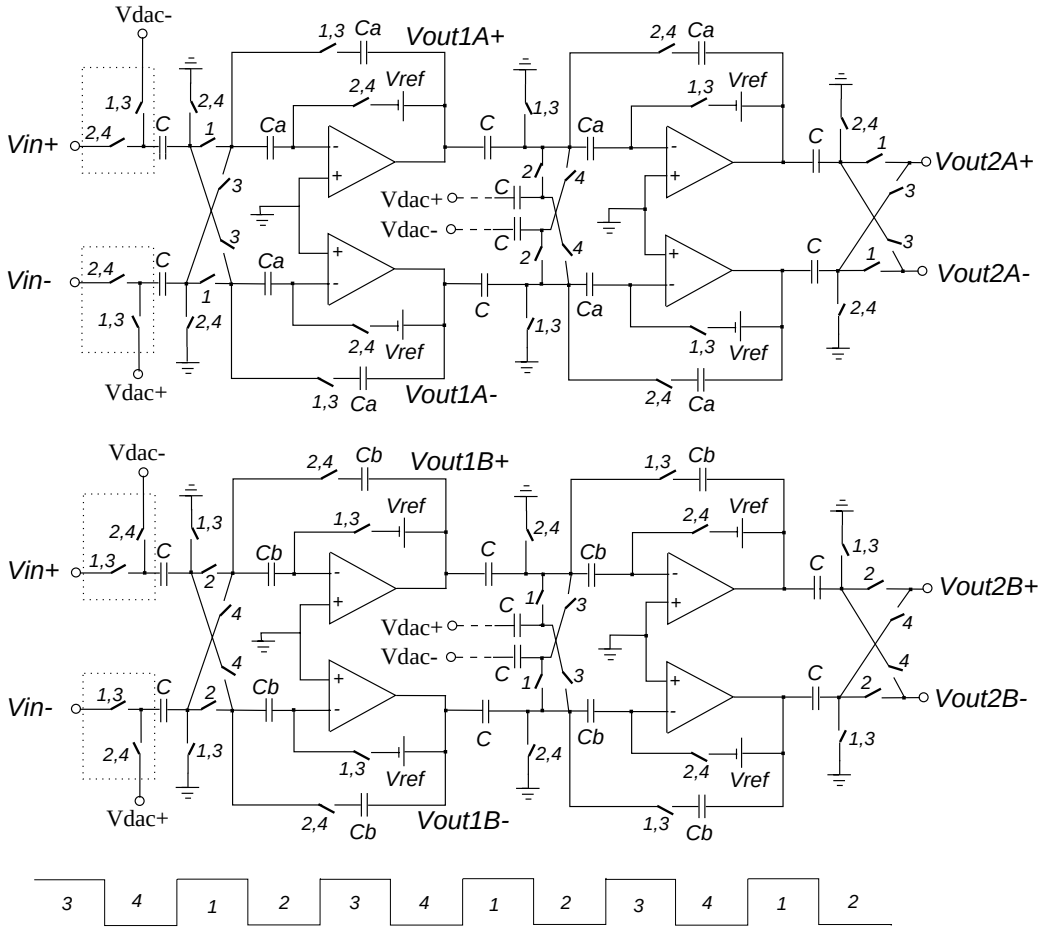

Figure 4.5. A fourth-order bandpass $\Delta\Sigma$ modulator.

Our I2P structure inherently allows an effective double sampling operation because the structure requires four distinct phases (see Fig. 4.4). SWITCAP2 simulation results are shown in Fig. 4.6 for f_{clock}=40 MHz with effective double-sampling (using four phases), and hence realizing f_{center}=20 MHz.

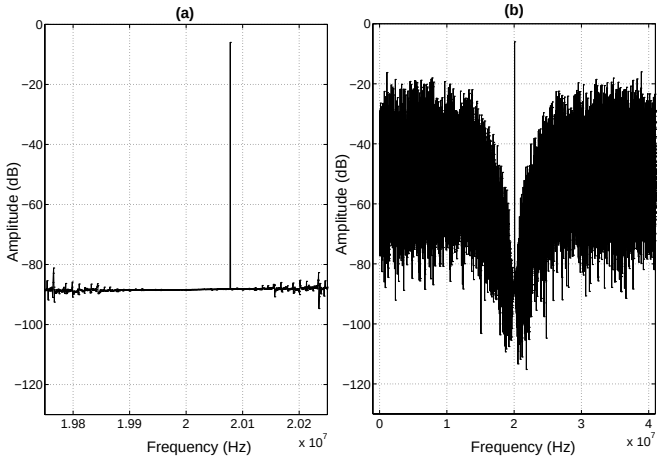

Figure 4.6. Simulation results for the low-voltage fourth-order bandpass $\Delta\Sigma$ modulator (a) within a 500 kHz frequency interval at 20 MHz (b) from DC to $f_{sampling}/2$

4.6 Low-Voltage Opamp

A modified version of the opamp used for the LV lowpass modulator was used for this bandpass $\Delta\Sigma$ modulator as shown in Fig. 4.7. The resistor is eliminated from the compensation branch and the left-side terminal of the compensation capacitor C_c is connected to node A. This way, a fast forward path is introduced. The gate terminal of the pmos mirror $M11$ is also connected to node A. These steps improve the slew-rate performance of the opamp since $M11$ follows the signal. Transistor sizes in the first and second stages are given in Table 4.2. These sizes are scaled down compared to those of the lowpass $\Delta\Sigma$ modulator design, since loading is smaller in this case.

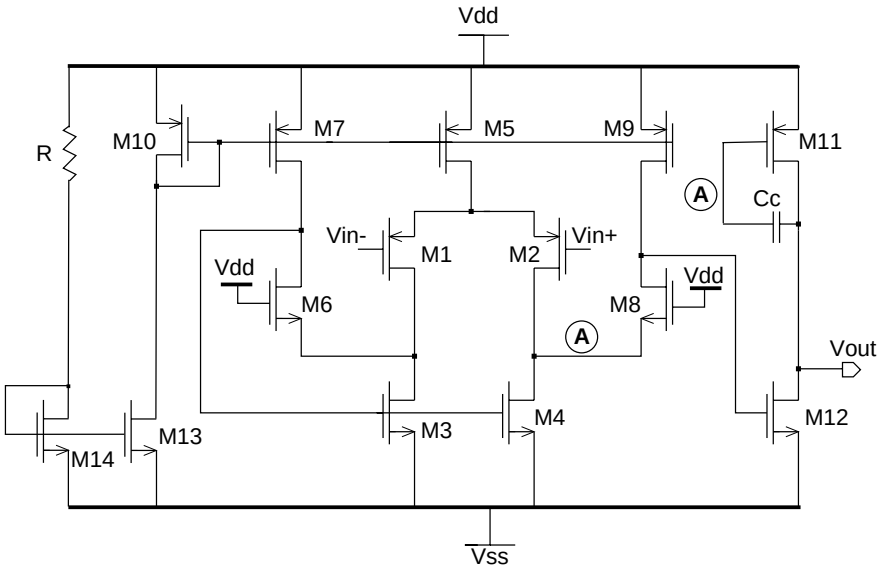

Figure 4.7. The low-voltage opamp for the bandpass $\Delta\Sigma$ modulator.

	1^{st} Stage	2^{nd} Stage
Components	W/L [μm]	W/L [μm]
M1-M2	105/0.5	105/0.5
M3-M4	30/0.5	30/0.5
M6-M8	15/0.5	15/0.5
M7-M9	15/0.5	15/0.5
M5	45/0.5	30/0.5
M10	15/0.5	15/0.5
M13-M14	20/0.5	20/0.5
M11	180/0.4	75/0.4
M12	150/0.35	90/0.35

Table 4.2. Transistor sizes for the low-voltage opamp of the bandpass modulator.

In this particular design, one of the goals is to reduce power consumption using the proposed resonator. The performance of the LV opamp is important when the reference current is reduced. Table 4.3 shows the simulation results when the total bias current is 1.1-mA and 0.75-mA, respectively. This Table also shows the performance of the opamp with different process corners such as worst-case-speed (WCS) and worst-case-power (WCP) These simulations show that the opamp performance is adequate for use in the fourth-order low-voltage bandpass modulator.

Parameters	1^{st}	2^{nd}	WCS	WCP
V_{dd}	1.2-V	1.2-V	1.2-V	1.2-V
A_{dc}	61 dB	63.5 dB	62 dB	55 dB
f_{unity}	204 MHz	110 MHz	165 MHz	240 MHz
Phase-margin	76	80	74	80
$T_{settling}$	8.6 ns	14 ns	9.6 ns	8.1 ns
Slew-rate	140 V/μs	80 V/μs	125 V/μs	178 V/μs
I_{total}	1.1 mA	0.75 mA	0.9 mA	1.4 mA
C_c	0.8 pF	0.8 pF	0.8 pF	0.8 pF
R_c	700	700	700	700
C_{load}	2 pF	2 pF	2 pF	2 pF

Table 4.3. The simulation results from SPECTRES with different operating conditions.

4.7 Mismatch Analysis in Double-Sampling Systems

There are double-sampling bandpass $\Delta\Sigma$ modulator implementations described in previous work [14, 7, 42, 36] but they have mirror image problems because of the mismatch between the paths. Obviously, circuit components never perfectly match each other so this problem is evident in all practical implementations. As seen in the Fig. 4.8(a), if there are more than one path from input to output, the mismatches between these paths create mirror images. The equivalent system is shown in Fig. 4.8(b) with the mismatch term, δ.

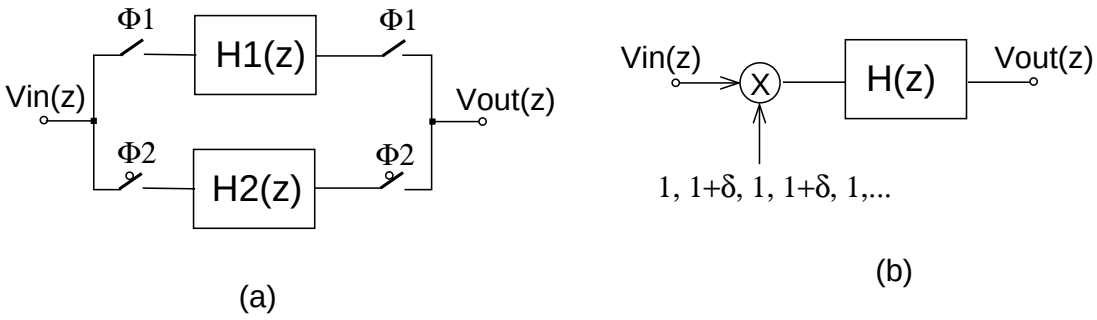

Figure 4.8. A double sampling system with (a) two separate paths and (b) the equivalent system.

This can be described as follows

$$H1(z) = H(z) \tag{4.3}$$

$$H2(z) = (1 + \delta) \cdot H(z) \tag{4.4}$$

where δ is the mismatch term.

The output signal can be expressed as

$$Vout(z) = Vout1(z) + Vout2(z) \tag{4.5}$$

where $Vout1(z)$ and $Vout2(z)$ are the outputs through $H1(z)$ and $H2(z)$, respectively and occur sequentially in an interleaved fashion. The final output with mismatch can be written as

$$
\begin{aligned}
Vout(z) &= Vin_{odd}(z) \cdot H1(z) + Vin_{even}(z) \cdot H2(z) \\
&= Vin_{odd}(z) \cdot H(z) + Vin_{even}(z) \cdot H(z) \cdot (1+\delta) \\
&= \Big[Vin_{odd}(z) + Vin_{even}(z) \Big] \cdot H(z) + \delta \cdot Vin_{even}(z) \cdot H(z) \\
&= Vin(z) \cdot H(z) + \delta \cdot Vin_{even}(z) \cdot H(z) \qquad (4.6)
\end{aligned}
$$

where "$\delta \cdot Vin_{even}(z) \cdot H(z)$" creates the mirror image [7, 42].

Fig. 4.9 shows the sampled signal and the mirror image due to mismatch in the frequency domain. Basically, the sampled signal will appear at $nf_s \mp f_{signal}$

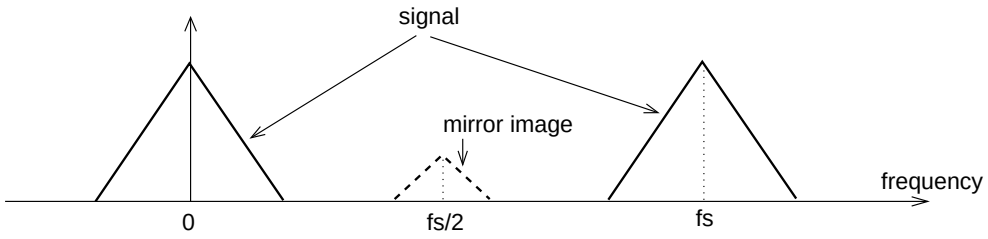

Figure 4.9. Frequency spectrum of the sampled signal showing the mirror image due to path mismatch.

while the mirror images appear at $nf_s/2 \mp f_{signal}$. This mirror image, in the passband of the $\Delta\Sigma$ modulator, is typically 40 dB lower than the fundamental signal.

4.8 Mismatch Issues in the Low-Voltage I2P Structure

With the double-sampling I2P structure, there are four possible mismatch problems: path mismatches, input sampling-capacitor mismatches, sampling clock-edge mismatches, and offset voltage mismatches of the opamps. These mismatch effects will be discussed in the following subsections.

4.8.1 Path Mismatches

Path mismatches occur between the multiple paths from the input to the output. There are two paths in the LV I2P resonator as shown in Fig. 4.4. Component mismatches will create the mirror image in the passband. The mirror image will be suppressed by the gain of the resonator since the mismatches affect the output of the resonator.

4.8.2 Input Sampling-Capacitor Mismatches

Input sampling-capacitor mismatch is reduced by using the same capacitor for both input signal sampling and DAC feedback. This enables us to shift mismatch of the input capacitor mismatch inside the $\Delta\Sigma$ loop. In this way, 20 dB of additional mirror image supression is achieved.

Simulations were done with 1% capacitor mismatch between the paths. Fig. 4.10(a) shows the Fourier transform of the output signal when input sampling capacitor of path A is equal to $(1 - 0.01) \cdot C$ and input sampling capacitor of path B is equal to $(1 + 0.01) \cdot C$. Simultaneously, both of DAC capacitors are equal to C. Fig. 4.10(b) shows the fourier transform of the output signal when input sampling capacitor of path A is $(1 - 0.01) \cdot C$ and input sampling capacitor of path B is $(1 + 0.01) \cdot C$. DAC feedback signals are applied through the input sampling capacitors during the next phase. Therefore better performance is obtained since the mismatch error is generated inside, and thus suppressed, by the loop.

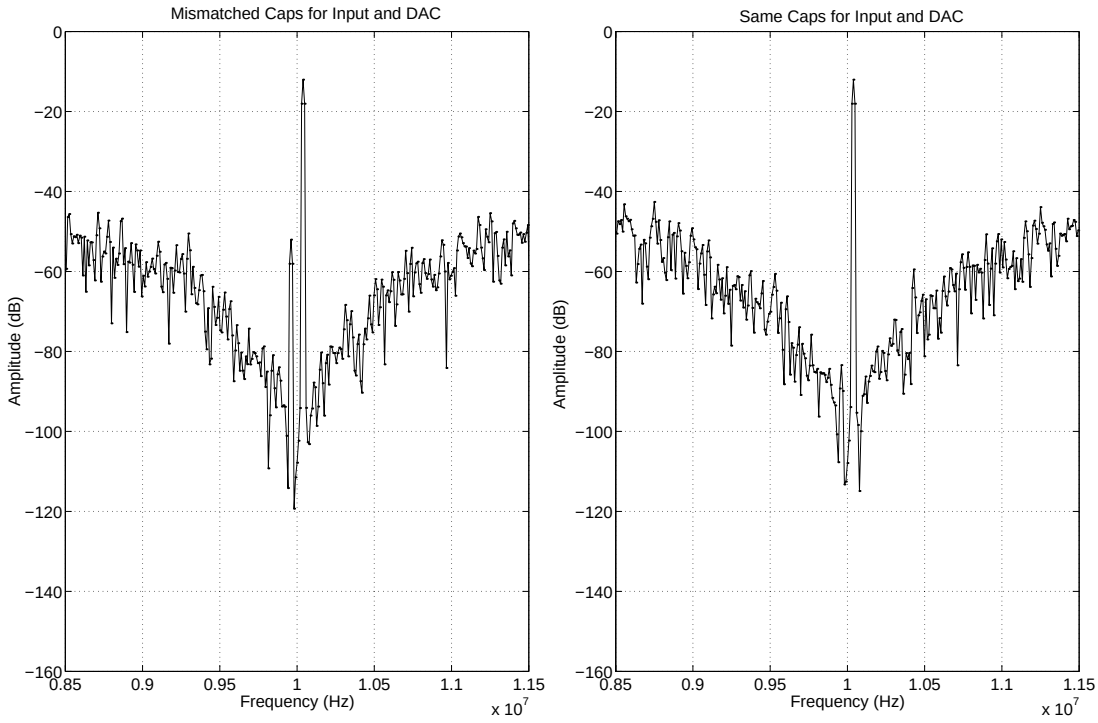

Figure 4.10. Simulation results with 1% capacitor mismatch when (a) C_{dac} is separate and when (b) C_{dac} is the same as the input sampling capacitor.

4.8.3 Clock-Edge Mismatches

The other mismatch problem is due to clock-edge variations (timing-skew) between consecutive clock phases ($1, 3$ and $2, 4$). These non-uniform sampling intervals introduce variations on the sampled-signal amplitude from one path to the other path. Clock signals twice as fast as in earlier circuits were used to sample the input signal to both paths with the same time intervals. For this reason, additional series switches (one for + and one for - signal paths) are added which are turned on/off by this faster clock. This is shown in Fig. 4.11.

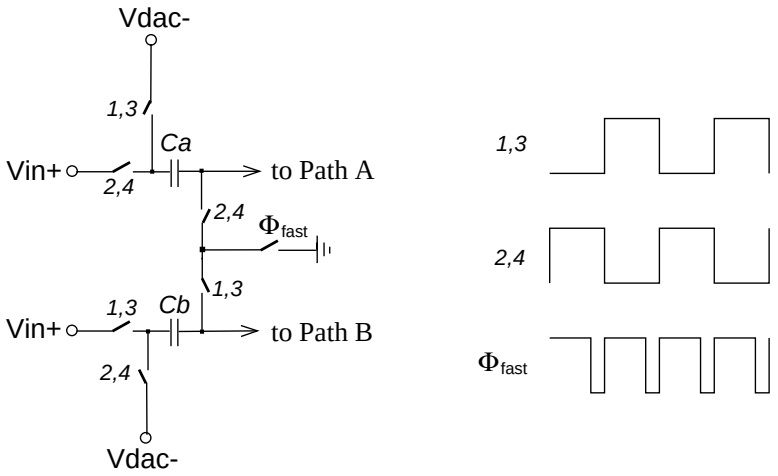

Figure 4.11. Solution to the timing skew between paths

4.8.4 Shifting of Offset Voltages

Other problems which may occur in the LV I2P bandpass $\Delta\Sigma$ modulator are the shifting of offset voltages and the 1/f noise of the opamps in the passband. Since the LV I2P architecture has four opamps and commutation operations, four different offset voltages appear at each outputs in a circulating fashion. This will create a tone at $f_s/4$.

Simulations show that the bandpass $\Delta\Sigma$ modulator is highly susceptible to first-stage offset voltages. The simulations were done with 1% capacitor mismatch and random offset voltages up to 15 mV at the inputs of the opamps. The result is shown in Fig. 4.12. The tone level at $f_{clock}/2$ is about 40 dB below the signal level. To improve this performance, we have implemented the correlated-double-sampling technique (CDS) [21, 40, 35, 9] for the bandpass $\Delta\Sigma$ modulator with 8 additional capacitors in front of opamps in order to cancel the offset voltage effects as shown in Fig. 4.5. The result with the CDS technique is shown in Fig. 4.13 showing improved SFDR performance.

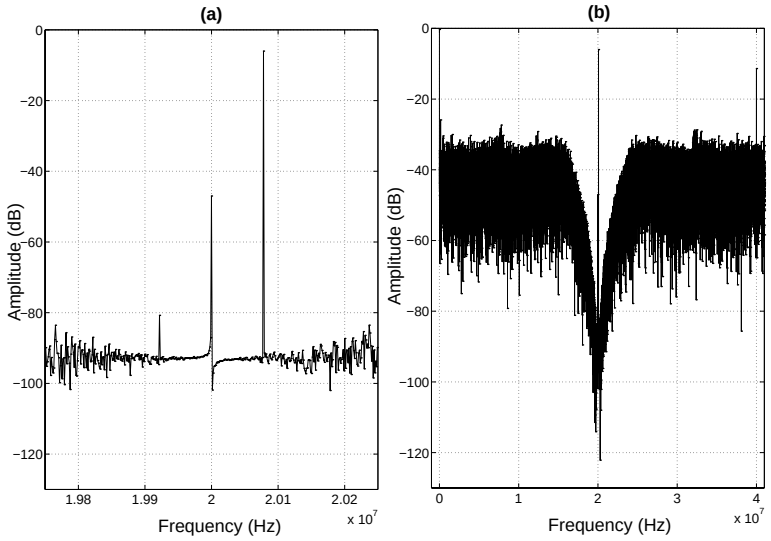

Figure 4.12. Simulation results with 1% capacitor mismatch and offset voltages up to 15 mV for 2^{17} FFT points (a) within a 500 kHz frequency interval (b) from DC to $f_{sampling}/2$.

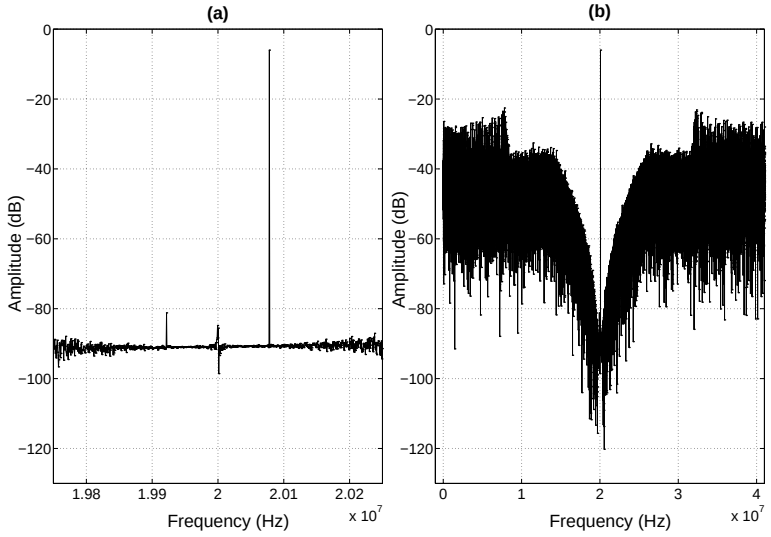

Figure 4.13. Simulation results with 1% capacitor mismatch and large offset voltages using CDS (a) within a 500 kHz frequency interval (b) from DC to $f_{sampling}/2$.

4.9 Clock Generation

There are two-phase and four-phase clocks needed for the particular $\Delta\Sigma$ modulator shown in Fig. 4.5. This clock generation is performed in three steps as shown in Fig. 4.14. First, $MCLK$, whose frequency is equal to 40 MHz, is applied to a frequency divider. Then, the resulting clock signal PHI, whose frequency is equal to 20 MHz, is used to obtain the two-phase clock. Finally, the four-phase clock is generated by using the two-phase clock. The delayed version of $MCLK$ is used to eliminate timing-skew problem discussed in Sec. 4.8.

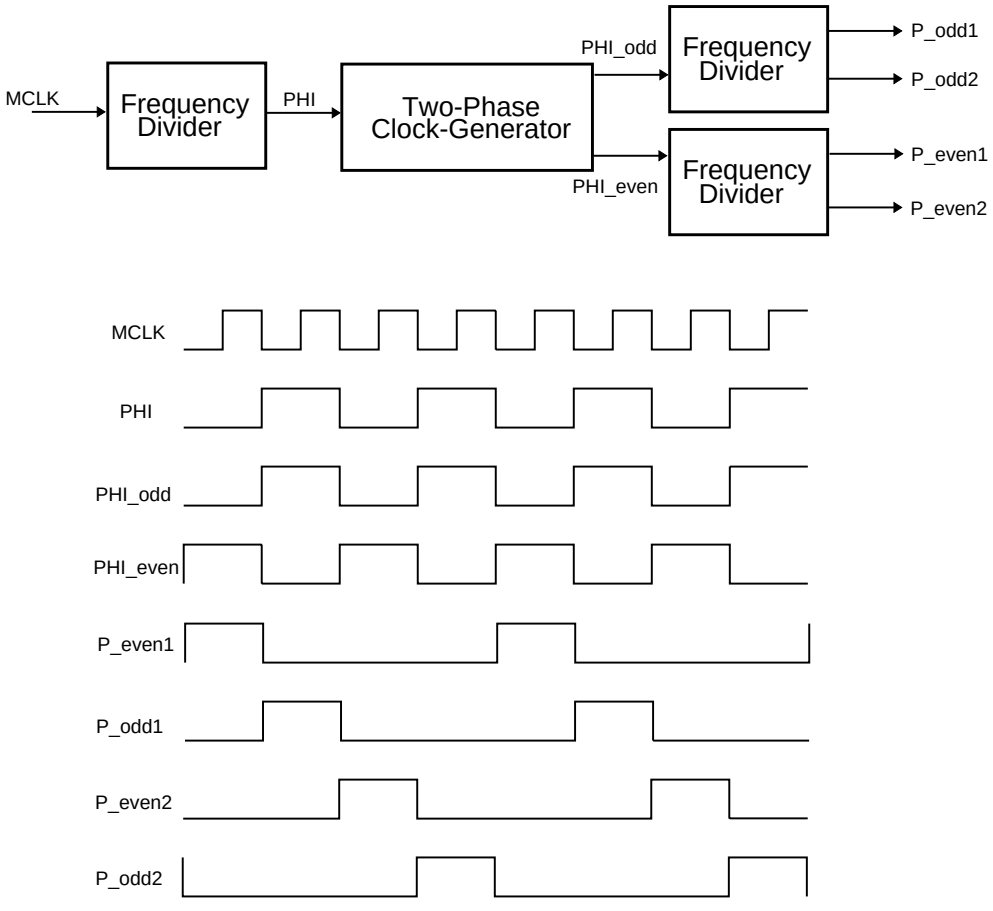

Figure 4.14. The clock generator system and the resulting clock timing diagram.

4.10 Layout and Floor Plan

Fig. 4.15 shows the layout of the prototype IC, realized in a 0.35 μm double-poly triple-metal CMOS technology by AMI. The layout was planned to realize a chip as symmetrical as possible. Having the two paths as close to each other as possible was also an important concern. For this reason, analog cells were flipped around the horizontal axis and laid out as close as possible. The other less-critical parts of the system, such as switches and digital cells of one path, are further away from those of the second path. Additionally, the layout was expanded horizontally in order to place the cells closer to each other.

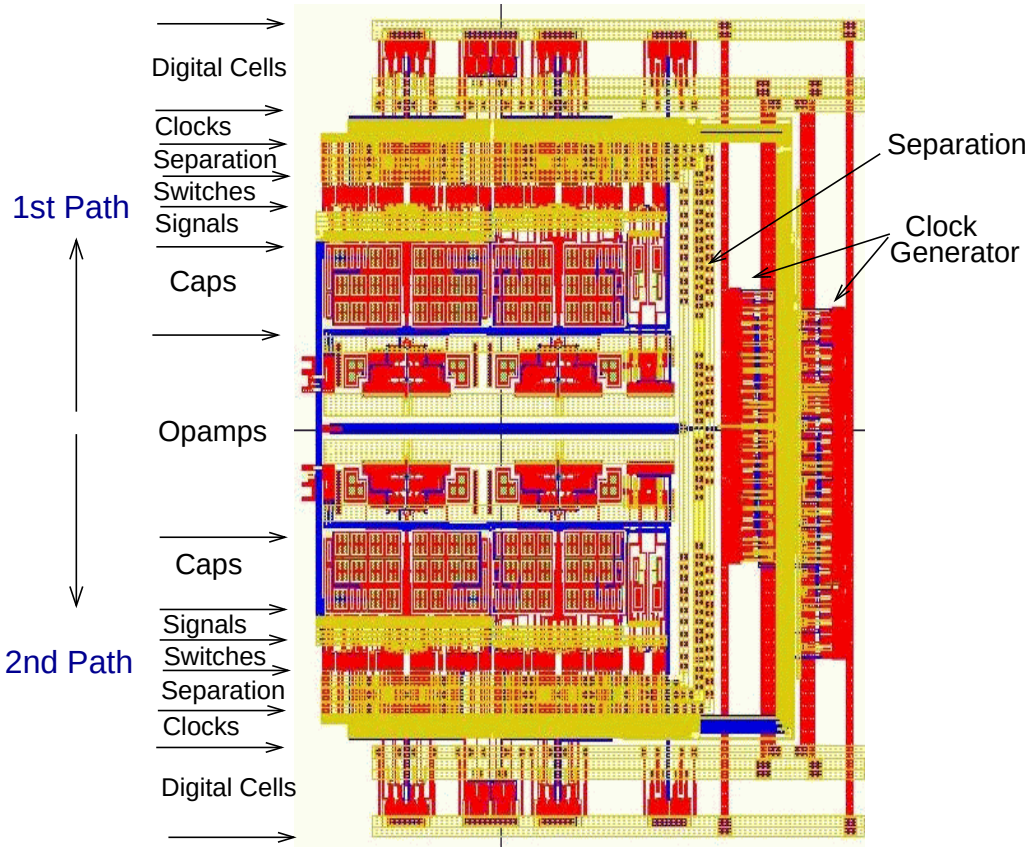

Figure 4.15. The layout of the LV fourth-order bandpass $\Delta\Sigma$ modulator.

Another important issue is the layout of the clock generation and distribution circuitry. The clock signals should have the same delay in both paths in order to avoid timing mismatch issues. For this reason, the clock generator is placed at center of the system, on the right side of the modulator. There are comparators on the right side of the modulator, hence, the clock generator will be far away from the critical input nodes. Well separation and ground connections to substrate are placed between the clock generator and the other parts of the system.

4.11 Test Board Design

Several test board design issues were considered for the bandpass modulator. These include power supply voltage without any tones, clean reference voltages and current biases, input signal from single-ended to differential, and design flexibility.

4.11.1 Power Supplies

The supply voltages will be provided either from a power supply or a battery. This power supply will be regulated by a low voltage linear regulator (MAX8869, Maxim). This regulator can be adjusted from 0.8 V to 5 V, although for this application only a range of 0.9 V to 1.2 V will be used. Three regulators are used in order to separate and minimize the crosstalk among the three different voltage supplies such as digital VDD and analog VDD, and VDD for peripheral devices.

4.11.2 Reference Voltages and Current Biases

Special attention has been paid to applying clean references to the board. There are four reference voltages needed. These are for +/- signal reference and +/- DAC feedback reference, whose nominal values are 1 V, 0 V, 1 V, 0 V, respectively. First the main reference voltage is obtained by a zener diode (REF1004-1.2,

Burr Brown). Then this voltage is applied to non-inverting amplifier stages with potentiometer-control to obtain required voltage level.

Four reference current sources needed for biasing the first and second stages and the two comparators. The nominal current values are 120 μA, 120 μA, 60 μA, and 60 μA, respectively. The comparator biases are separated in order to minimize talk and disturbance between them. The main current reference is obtained and by a dual current source (REF200, Burr Brown). This global current is adjusted by either potentiometers or non-inverting opamps.

4.11.3 Single-Ended to Differential Input Signal Conversion

A single-ended input signal will be applied to the board from a high-frequency signal synthesizer. The signal amplitude will be varied from 0 V to 1 V. The nominal frequency of the signal is approximately 10 MHz. Single-ended to differential conversion is done by using non-inverting and inverting amplifiers. Symmetry between +/- paths is preserved in order to avoid oscillations or voltage differences. Wideband low-distortion opamp (OPA642, Burr Brown) was used.

4.11.4 Design Flexibility

Lower supply voltage and power consumption are the two main concerns of this project. For this reason, the current biases and power supply voltages are designed to allow adjustments. Specificially, power supply and reference voltages can be adjusted from 1.2 V to 0.9 V and current biases can be reduced to almost half of their nominal values.

4.12 Conclusions

The crucial requirements of a SC bandpass ADC are its center frequency stability and power dissipation. Cellular phone users don't want to hear any noise, similarly, no radio listener wants to listen to music from the adjacent channel. These considerations are important for any modern communication devices. Therefore, the center frequency of the circuit blocks, especially of the analog-to-digital converter, has to be at exactly the desired frequency. Thus, this application truly affects the quality of most products in the wireless communication industry. Using our architecture, a low-sensitivity SC resonator, usable in a bandpass ADC, can be designed.

The second requirement is power consumption. It is highly desirable to use devices with longer battery life. Hence, the current trend is to make more efficient and reliable devices that consume less power. By using these architectures, power dissipation can be easily reduced since the quality of the resonator transfer function does not need opamps with very high bandwidth, thus high power. This means that low-sensitivity circuits such as our SC resonators will significantly reduce the current consumption and effectively extend battery life.

This architecture may also stimulate future work to increase the center frequency of the digitization; hence, the digital signal processing blocks could be increased in the portable devices, shifting the analog-digital boundary towards the antenna. This means reduced complexity, relaxed requirements, and higher quality and convenience.

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