A Tunable Duty-Cycle-Controlled Switched-R-MOSFET-C CMOS Filter for Low-Voltage and High-Linearity Applications

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1 Introduction

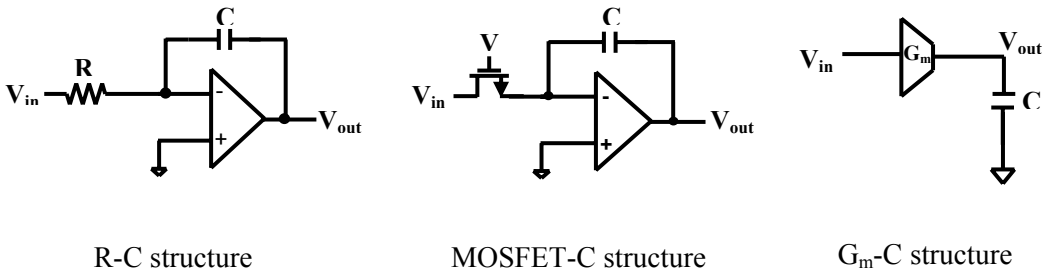
1.1 Brief Review on Filter Design

A filter is a two-port circuit designed to process the magnitude and/or phase of an input signal in some prescribed way in order to generate a desired output signal [1]. The history of electric filters can be dated back to about 1915 [2], [3]. Nowadays, application of filters is ubiquitous in communication systems, measuring equipment, and other signal processing-related devices.

All filter implementations can be classified into two categories: passive or active. Passive filters consist of only passive elements, *i.e.*, resistors and capacitors. Active filters consist of passive elements along with active devices, such as transistors or opamps. Passive filters require no power and generate no DC offset, but are large and heavy. They also suffer from problems such as insertion loss, high distortion, low precision, and low tunability, etc. The design of active filters originated in 1950s when Sallen and Key used low-gain amplifiers in their filter design [4]. These active filters enabled reduced size and did not suffer from insertion loss. Subsequent development in designing of active RC filters using high-gain operational amplifiers (opamps) [5]–[7] and hybrid integrated circuit (HIC) enabled the complete elimination of the large inductors that were essential in general LC filters [8]–[10]. As a result, active filters had significant reduction in their sizes and costs, and became the dominant form in

electrical filter design. Today, most filters are implemented in monolithic integrated circuits (ICs) in the form of an active filter.

Active filters can be categorized into continuous-time (CT) filters and discrete-time (DT) filters based on the nature of the signals processed. CT filters take continuous-time signals and output continuous time signals. Typical active CT filter building blocks include the R-C structure, the MOSFET-C structure, and the G_m-C structure (Fig 1.1). The MOSFET-C structure directly follows the R-C structure, replacing the resistors with MOSFET transistors in their triode regions. A simple G_m-C structure uses a transconductor that relates the output current with input voltage linearly to build an integrator.



R-C structure MOSFET-C structure G_m-C structure

Fig 1.1 Typical active CT filter building blocks.

For a DT filter, the input signal or output signal or both are in discrete forms. A special kind of DT filter, switched-capacitor (SC) filter, uses a switched capacitor to simulate a resistor. The basic theory can be demonstrated using an integrator shown in Fig 1.2. The circuit momentarily connects to A, charging capacitor C_s to the input voltage. Then C_s is switched to B, dumping the charge

onto the negative input of the opamp, which transfers the charge to the integrating capacitor C_i. The charge will remain on C_i until the next cycle. The switch frequency can be controlled by a clock. The higher the clock frequency, the more often C_i receives charge. This switched capacitor C_s is equivalent to a resistor with an effective resistance of $R_{eff} = 1/ (C_s f_{clk})$,where f_{clk} represents the clock frequency [11], [12]. SC filters are in the class of analog filters since voltage levels in these filters remain continuous. They operate at discrete-time steps, and the output signals of SC filters are interpreted as being discrete in nature. Since a SC filter is a sampling device, an anti-aliasing filter is required, which increases the circuit complexity. However, SC filters have accurate transfer functions (on the order of 0.1 percent), high linearity and good noise performance. They are very popular in modern filter design especially where cost, space, and accuracy are top considerations.

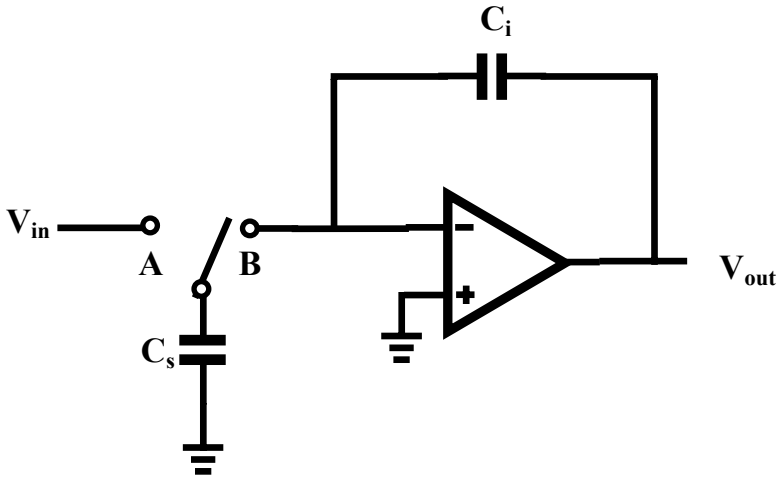


Figure 1.2 An SC integrator.

1.2 Motivation for the current research

1.2.1 Low voltage application

One important trend of modern IC design is the fast downscaling of transistor dimensions. As a result, the supply voltage for circuit operation is also decreasing fast. The forecast of operating voltages for CMOS technology is shown in Figure 1.3 [13].

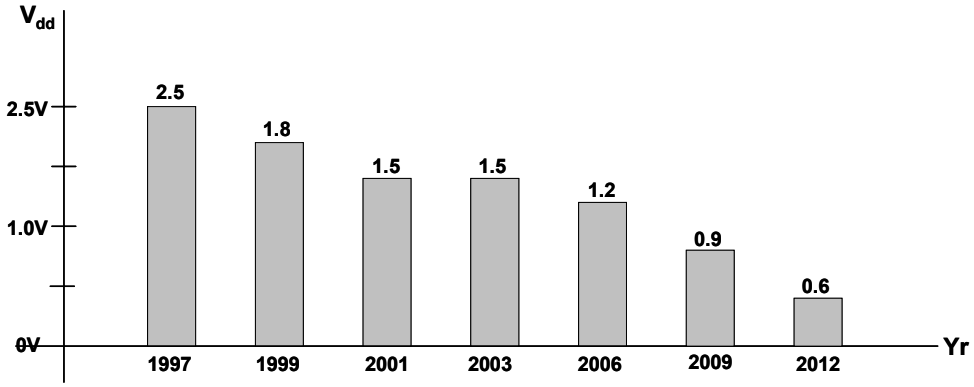


Figure 1.3 Semiconductor Industry Association 1997 forecast of CMOS supply voltage.

As a result, it becomes necessary to develop new circuit architectures and to improve many existing ones to keep the performance comparable to that achieved with higher supply voltages [14]. One particular example is the floating switch problem in the signal path of a SC filter. Switches in IC circuits are most commonly realized using MOS transistors (Fig 1.4). M1 in Fig 1.4 is a floating switch that sees the full-signal swing and may not operate properly for low gate voltages. For example, assume the input voltage (V_{in}) is a sinusoidal wave with

0.3V signal swing around a common-mode input voltage of 0.5V. Then V_{in} can swing up to 0.8V. To turn M1 on, the gate voltage (V_G) has to be larger than V_{in} + V_{th} (threshold voltage). A typical V_{th} value is 0.5V for modern short-channel MOS transistors, so a minimum V_G of 1.3V is required just to turn M1 on. If the transistor gate is connected to the supply voltage (V_{DD}), then the circuit cannot be operated for supply voltages lower than 1.3V.

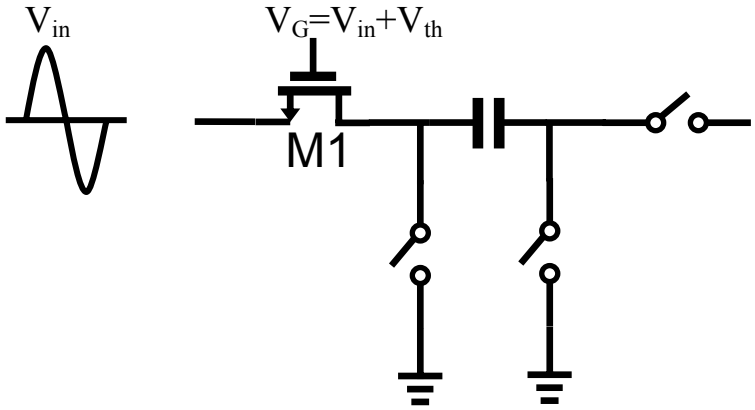


Fig 1.4 A floating switch in a switched-capacitor input branch.

Special techniques may be required to solve this problem [15]. The most direct approach is to increase V_G using voltage bootstrapping, but this may affect the long term reliability of the circuit. Along with the reduction in sizes of transistors, the gate oxide thicknesses are also reduced in modern CMOS technologies. As a result, excessive V_{GS} values may result in gate oxide stress and cause breakdown. On the other hand, excessive V_{DS} values might cause punch-through and hot electron effects. Therefore, for a design to be very reliable, all the

terminal-to-terminal voltages of the MOSFETs used in the design should always be limited to V_{DD} at any point of time during operation.

1.2.2 Accuracy and linearity issues with CT filters

One critical issue with CT filters is the RC time-constant variation problem due to process variation, temperature drift and aging. The integrated RC time constants can easily vary by as much as 30 percent [12], [16]. At extreme conditions, the integrated filter can vary up to a maximum of ± 50% in the 3-dB corner frequency [17]. This problem is magnified by the downscaling in modern IC circuits because it is more difficult to achieve good matching of physical elements.

The problem of RC variation is typically compensated by some tunable elements. Many design techniques proposed for tuning have one common drawback: the tunable elements have inherent nonlinearity. Therefore, the linearity performance in these designs is commonly limited. A more detailed review on existing CT filters is given by Moon [3].

Among various types of CT tunable filters, MOSFET-C filters have become popular, mainly because of their simplicity. They are easily implemented with opamp blocks while maintaining close architectural similarities to an active RC filter [18]. One of the main limitations of MOSFET-C filter application is its poor linearity performance. Using total harmonic distortion (THD) as a measurement of linearity, the typical THD value for a MOSFET-C filter is

between -40 to -60 dB. It is very difficult for a conventional MOSFET-C filter to exceed the -60 dB ceiling [19].

A linearity improvement technique proposed by Moon and Song [19] yielded a 50 dB improvement in THD over the conventional MOSFET-C filter when applied in a fifth-order Bessel filter. Two factors have contributed to the linearity improvement in their technique. First, the nonlinear transconductance element is moved inside a feedback loop, resulting in a significant improvement of distortion. Second, a simple R-MOSFET input branch is applied to scale down the actual voltage across the nonlinear element M1($V_x << V_{in}$ in Fig 1.5) so that the operation is more closely within the linear range.

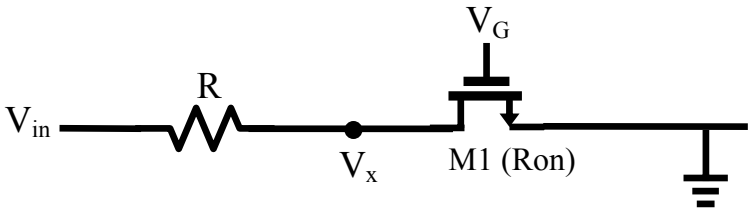


Fig 1.5 R-MOSFET input branch.

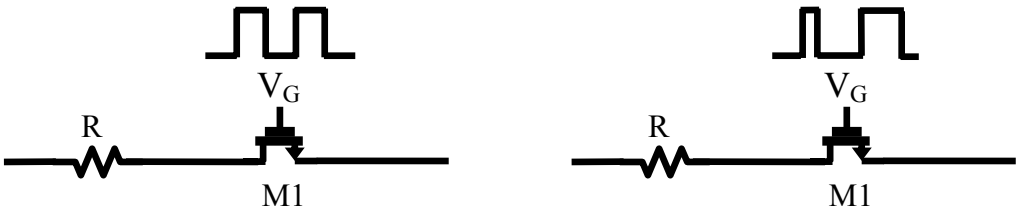
1.2.3. Limited tuning range for existing tuning techniques

Various tuning techniques exist for automatic tuning of the filter transfer functions. Most of these tuning circuits use a direct or an indirect approach to generate a variable gate voltage from an accurate reference circuit. For M1 in Figure 1.5 to be operational, V_{GS} has to be larger than V_{TH}. On the other hand, to prevent gate oxide breakdown and maintain the circuit reliability, V_{GS} should

always be smaller than V_{DD}. Hence, V_G can only be varied between $V_{TH} + V_x$ and V_{DD}, which implies a very small tuning range, especially for low-voltage application. Using thick oxide devices can allow higher voltage across the gate, so the tuning ranging can be improved. However, this approach increases the production cost, and is less commonly used.

A more commonly used approach is bootstrapping of the gate voltage, V_G. The control voltage can be generated to be a sum of a common-mode voltage and the control voltage. The common-mode voltage will turn on the MOSFET resistor and the control voltage is used to tune the MOSFET resistor. For low supply voltage, the bootstrapped V_G has to be larger than V_{DD} for sufficient tuning range, then the filter is not a true low-voltage application any more. Again, the reliability issue has to be considered.

Tsividis *et al.* reported a signal processing technique that relies on variable timing rather than variable voltages to adjust the time constants [20]–[22]. The transistors were turned on and off using programmable pulses, the duty cycles of which determined the transfer function coefficients. It is therefore possible to tune the circuit by changing the duty cycle for V_G (Fig 1.6). The variable duty cycle in Fig 1.6.b can be generated automatically in the circuit for realizing different transfer functions or to take care of the variations in RC constants. There is no change in the magnitude of V_G, so true low-voltage application is possible. Wide tuning range is easily achievable.



a) clock with constant duty cycle *b) clock with variable duty cycle*

Fig 1.6 Changing of duty cycle for V_G.

1.3 Proposed Work

In the present study, a high-Q biquad filter with tunable corner frequency is proposed to combine the advantages of MOSFET-C CT filters and SC filters. The proposed filter is simple in configuration. It has accurate corner frequency tuned to an SC reference circuit, high linearity and is highly suitable for low-voltage applications.

An automatic duty-cycle-tuning circuit is proposed with a wide tuning range (±80%). The corner frequency of the biquad filter can be tuned by changing the duty cycle of the clock of the filter automatically, using a switched-capacitor branch as a reference. The linearity improvement technique proposed by Moon and Song [19] is modified in this study to improve the linearity (Fig 1.6.). The transistor M1 in R-MOSFET input branch is functioning as a switch only instead of as a tunable resistance. Therefore the voltage across M1 can be very small, minimizing the non-linear effects of the tuning element. The branch in Fig 1.6. is named switched-R-MOSFET input branch. It can be applied in any kind of

design for a CT filter with a self-tuning feature. There is a great potential for this technique in low-voltage applications, since the tuning does not require changing the magnitude of the gate voltages, and does not affect the linearity significantly.

The rest of this thesis is organized as follows. Chapter 2 describes the principle of operation of the proposed technique. Chapter 3 describes the duty-cycle tuning scheme. Chapter 4 shows the design of a high-Q biquad filter with the proposed tuning technique. Some low-voltage considerations for transistor-level realization are also discussed. Chapter 5 describes simulation results, followed by concluding remarks in Chapter 6.

2 Operation Fundamentals

2.1 Proposed Structure

The basic principle of operation of the switched-R-MOSFET-C circuit can be illustrated using a first-order filter, shown in Fig 2.1.

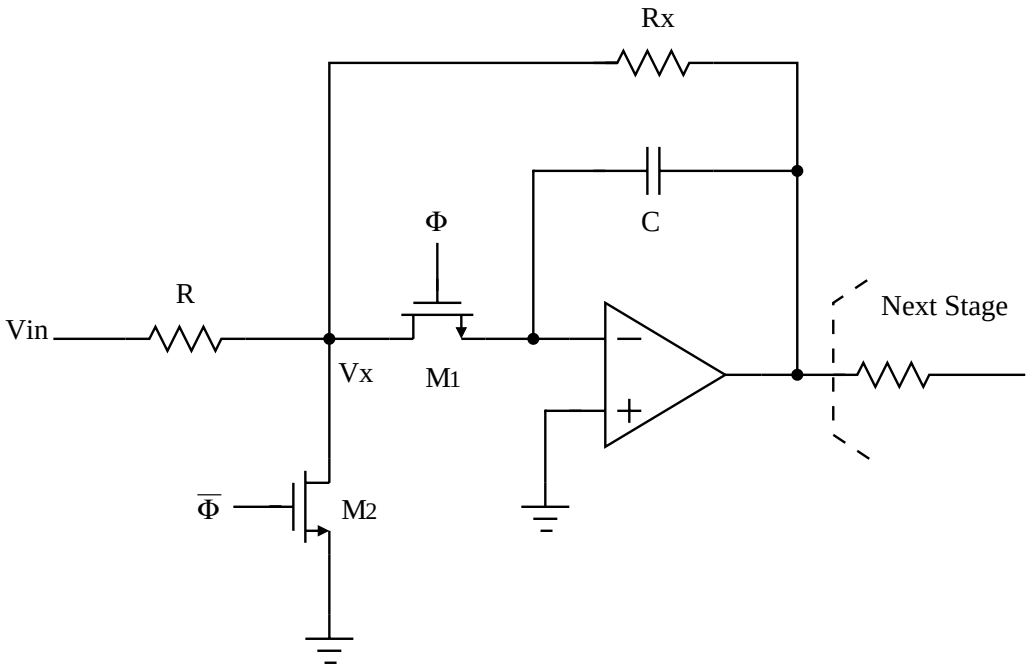


Figure 2.1 A first-order filter with switched-R-MOSFET input branch.

The transfer function can be affected by changing the duty cycle of the clock Φ that controls the gate of transistor M1. When the duty cycle of Φ is changed, the time available for the input signal V_{in} to charge C is also changed. Consequently, a multiplication factor relying on the duty cycle of Φ can be realized, which will in turn affect the transfer function [20]. The transistor M2 is

controlled by a complementary clock $\overline{\Phi}$ to keep the node voltage V_x close to the virtual ground of the opamp.

A few merits are associated with this proposed structure. First, the transfer function can be tuned by changing the time for input signal to charge C, *i.e.* by tuning the duty cycle of Φ. A wide tuning range is easily achievable because the duty cycle can be varied from 0 to 100% theoretically. If a filter is designed for 50% of clock duty cycle, 100% tuning can be achieved by changing the duty cycle to 100% and -100% tuning can be achieved by changing the duty cycle to 0. However, the tuning range will be smaller than ±100% in real implementation because of the requirements in circuit settling.

Second, the resistor R in series with the input MOSFET transistor M1 will help to improve the linearity significantly, since most of the input voltage is dropped across the linear resistor. M1 only needs to function as a switch in this structure. R_{on} of M1 can be small to minimize the non-linearity of M1. Including M1 in the feedback loop will further increase the linearity [19].

Finally, there are no floating switches in the circuit. M1 is connected to the input node of the opamp which can be biased to a low voltage close to the ground, e.g. 0.1V. There is no problem to turn M1 on for a 1-V supply voltage and a transistor with a V_{th} of 0.5V. The terminal-to-terminal voltages for all transistors are always smaller than V_{DD}, making the proposed configuration highly suitable for true low-voltage applications.

2.2 Theory of Operation

To understand the operation theory more thoroughly, basic mathematic calculations were carried out for two different configurations. Some real element values were put into the equations and calculated using Matlab6.0. The Matlab results were compared with simulation results obtained using a circuit simulator, Cadence.

2.2.1 Filter configuration with the switch M1 outside the feedback loop

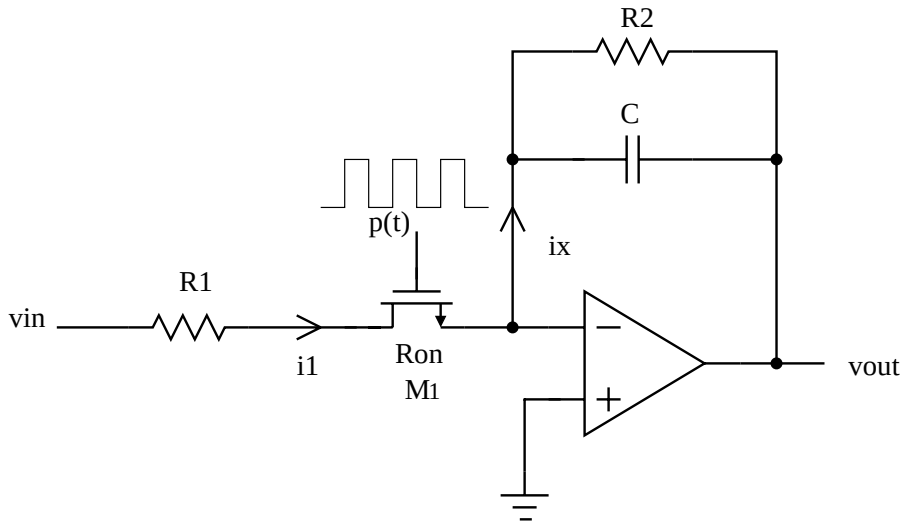


Fig 2.2 Filter configuration with M1 outside the feedback loop.

By careful examination of the circuit in Fig 2.2, it can be noted that $i_x(t)$ is the product of M1 gate controlling signal $p(t)$ and the input current $i_1(t)$. Therefore

$$i_x(t) = i_1(t)\,p(t) \qquad \text{(Eq. 2.1)}$$

$$i_x(t) = \frac{v_{in}(t)}{R_1 + R_{on}} p(t) \qquad \text{(Eq. 2.2)}$$

If Eq. 2.2 is translated into frequency domain by using the Laplace transform, the multiplication will become a convolution:

$$I_x(s) = \frac{V_{in}(s)}{R_1 + R_{on}} \otimes P(s) \qquad \text{(Eq. 2.3)}$$

$$\frac{V_{out}(s)}{I_x(s)} = -\frac{R_2}{1 + R_2 sC} \qquad \text{(Eq.2.4)}$$

The filter output using Eq. 2.3 and Eq. 2.4 is given by,

$$V_{out}(s) = -\frac{R_2}{R_1 + R_{on}} \frac{1}{1 + R_2 sC} (V_{in}(s) \otimes P(s)) \qquad \text{(Eq. 2.5)}$$

Converting equation Eq. 2.5 back into the time domain, we get:

$$v_{out}(t) = -\frac{R_2}{R_1 + R_{on}} \frac{1}{R_2 C} \left[(e^{\frac{-t}{R_2 C}} u(t) \right] \otimes [v_{in}(t) p(t)] \qquad \text{(Eq. 2.6)}$$

The Fourier series of the clock signal *p(t)* when the duty cycle is 50% is the following:

$$p(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{2\sin(\frac{n\pi}{2})}{n\pi} \times \cos(n\omega_0 t) \qquad \text{(Eq. 2.7)}$$

The output signal $v_{out}(t)$ and current $i_x(t)$, were calculated in Matlab using Eq. 2.1 and Eq. 2.2 by assuming the following values: $v_{in}(t)$: a sine wave with a frequency at 312.5 kHz and an amplitude of 1.8V. The clock is a 20 MHz, 50% duty cycle square wave. $R_1 = R_2 = 1$ kΩ, R_{on}=35 Ω, C=50 pF, opamp DC gain=1×10^6. The resulting circuit is then simulated in Cadence and the results are shown in Fig 2.3 and Fig 2.4, together with the Matlab calculation results. These

simulations indicate good match between calculated and simulated results of the circuit.

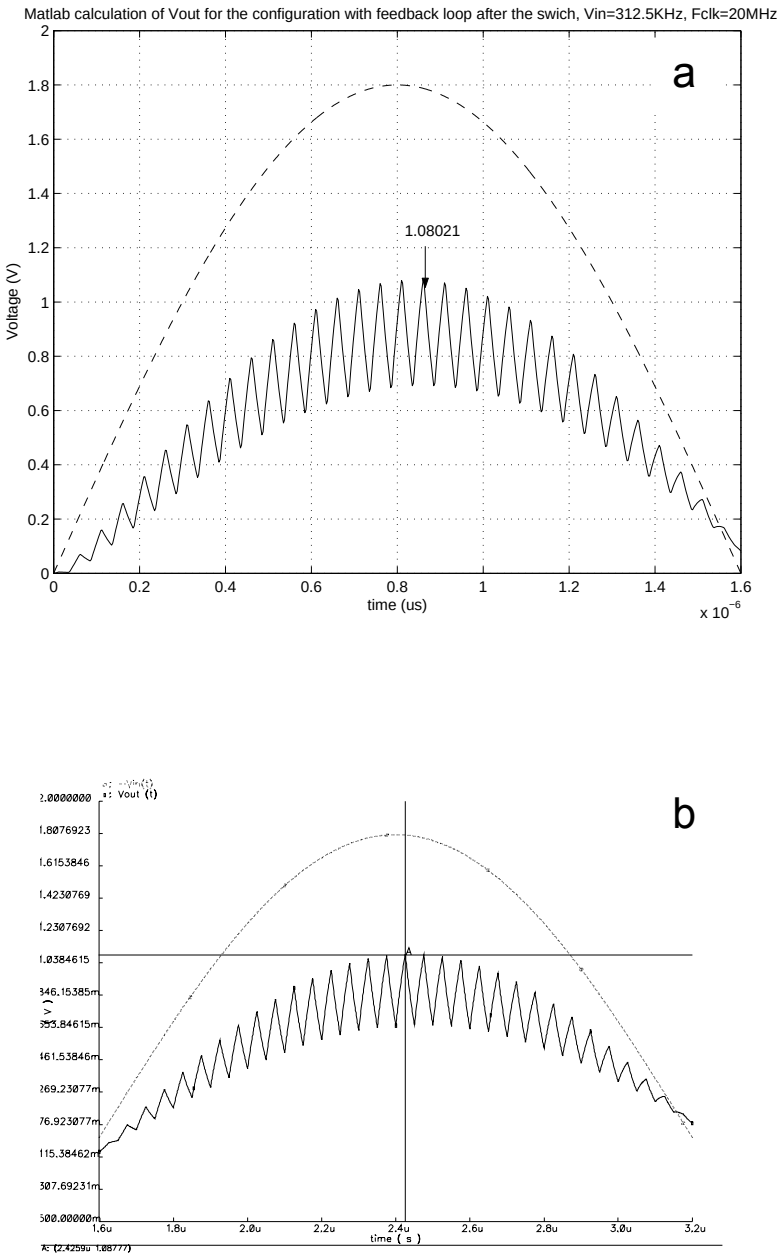


Fig 2.3 Comparison of Matlab calculation and Cadence simulation of $v_{out}(t)$ for the filter in Fig 2.2. a) calculated $v_{out}(t)$ b) simulated $v_{out}(t)$.

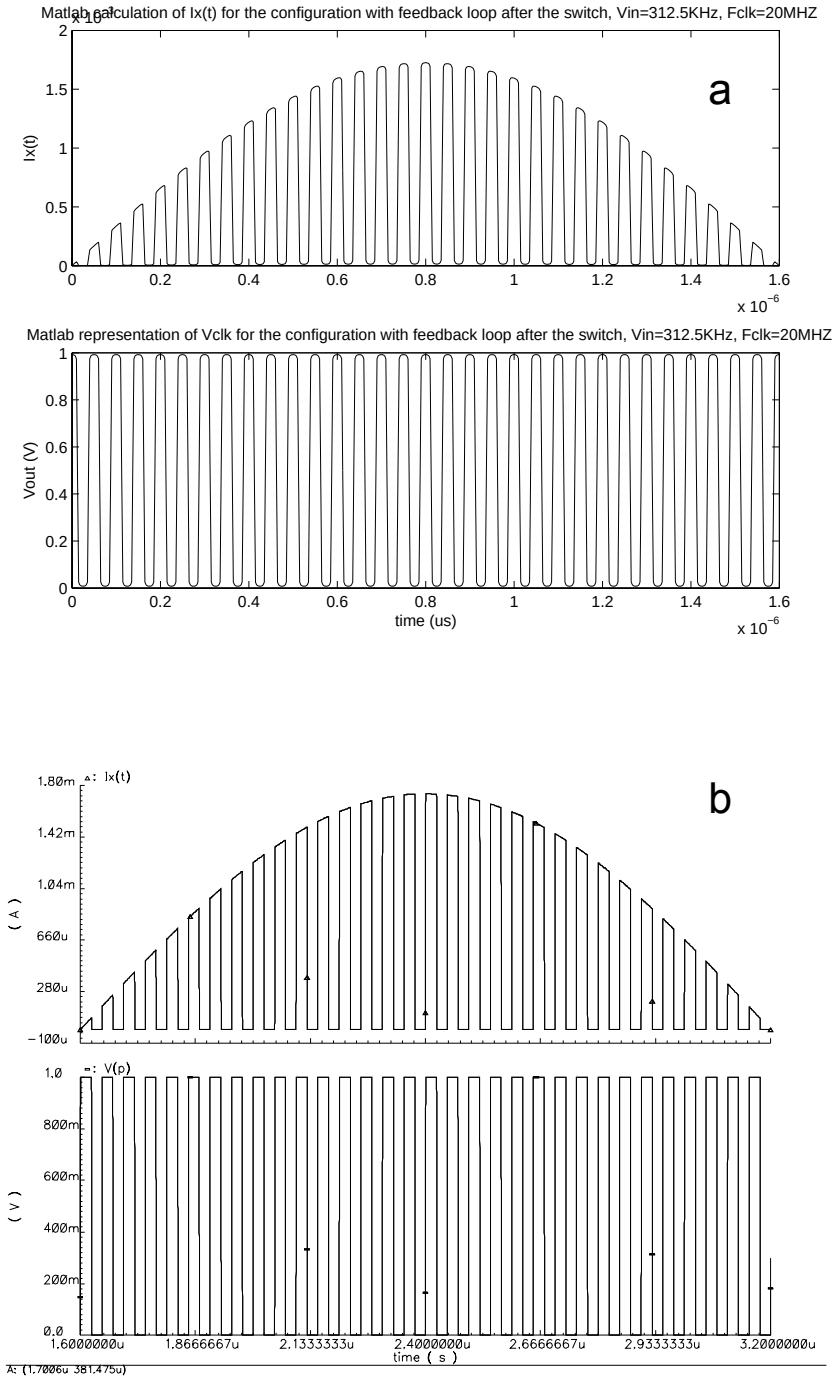


Fig 2.4: Comparison of Matlab calculation and Cadence simulation of $i_x(t)$ for the configuration in Fig 2.2. a) calculated $i_x(t)$ b) simulated $i_x(t)$.

2.2.2 Filter configuration with the switch M1 inside the feedback loop

The approach used for the filter in Fig 2.2 is not suitable for this configuration, because v_1 is not only related to v_{in} but also related to v_{out}. Therefore the calculations need to be carried out using node equations.

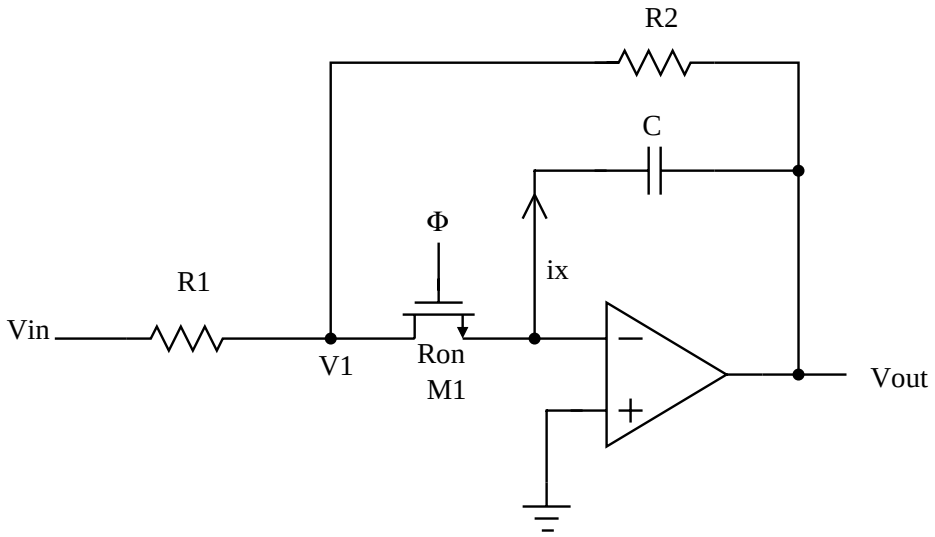


Fig 2.5. A filter configuration with M1 inside the feedback loop.

When the switch is closed:

$$\hat{i}_x(t) = \frac{v_1}{Ron} \qquad \text{(Eq. 2.8)}$$

$$\hat{i}_x(t) = \frac{v_{out}(t)v_1(t)}{R_2} + \frac{v_{in}(t) - v_1(t)}{R_1} \qquad \text{(Eq. 2.9)}$$

$$v_1(t) = \frac{v_{in}(t)R_2R_{on}}{R_2R_{on} + R_1R_2 + R_1R_{on}} + \frac{v_{out}(t)R_1R_{on}}{R_2R_{on} + R_1R_2 + R_1R_{on}} \qquad \text{(Eq. 2.10)}$$

$$\hat{i}_x(t) = \frac{v_{in}(t)R_2}{R_2R_{on} + R_1R_2 + R_1R_{on}} + \frac{v_{out}(t)R_1}{R_2R_{on} + R_1R_2 + R_1R_{on}} \qquad \text{(Eq. 2.11)}$$

$$I_x(s) = \frac{V_{in}(s)R_2}{R_2R_{on} + R_1R_2 + R_1R_{on}} + \frac{V_{out}(s)R_1}{R_2R_{on} + R_1R_2 + R_1R_{on}} \qquad \text{(Eq. 2.12)}$$

$$I_x(s) = -V_{out}(s)sC \qquad \text{(Eq. 2.13)}$$

Let $R_2R_{on} + R_1R_2 + R_1R_{on} = a$

$$-V_{out}(s)\,(sC + R_1/a) = (R_2/a)\,V_{in}(s) \qquad \text{(Eq. 2.14)}$$

$$V_{out}(s) = -\frac{R_2/R_1}{1 + (a/R_1)sC}V_{in}(s) \qquad \text{(Eq. 2.15)}$$

Transforming equation Eq. 2.15 back to the time domain, we get,

$$v_{out}(t) = -\frac{R_2}{aC}\left[e^{-\frac{t}{\frac{aC}{R_1}}}u(t)\right] \otimes v_{in}(t) \qquad \text{(Eq. 2.16)}$$

The effect of the output voltage v_{out} on the node voltage v_1 can be included in the calculations considering an initial state that is associated with the value of v_{out} from the previous clock period. Assume that t_1 is the time when the first clock pulse is turning off, then:

$$v_{out}(t_1) = -\frac{R_2}{aC}\left[e^{-\frac{t_1}{\frac{aC}{R_1}}}u(t)\right] \otimes v_{in}(t_1) \qquad \text{(Eq. 2.17)}$$

The $v_{out}(t)$ for the second clock period can be calculated using Eq. 2 with $v_{out}(t_1)$ as its initial condition

$$v_{out}(t) = -\frac{R_2}{R_1}\frac{R_2}{aC}\left[e^{-\frac{t}{(a/R1)\times C}}u(t)\right] \otimes (v_{in}(t) + \frac{R_1}{R_2}v_{out}(t_1)) + v_{out}(t_1) \qquad \text{(Eq. 2.19)}$$

$v_{out}(t)$ for the third clock period can be calculated using the same approach. The complete waveform for $v_{out}(t)$ can then be found by repeating this procedure. For every off phase, $i_{out}(t)$ will hold the value of the last point of the previous on phase.

The current $i_x(t)$ can then be calculated using Eq. 2.12. The same element values depicted for the filter in Fig 2.2 were used for calculation and simulation of this filter. Again, the simulations indicate good match between calculated and simulated results of the circuit (Fig 2.6 & Fig 2.7).

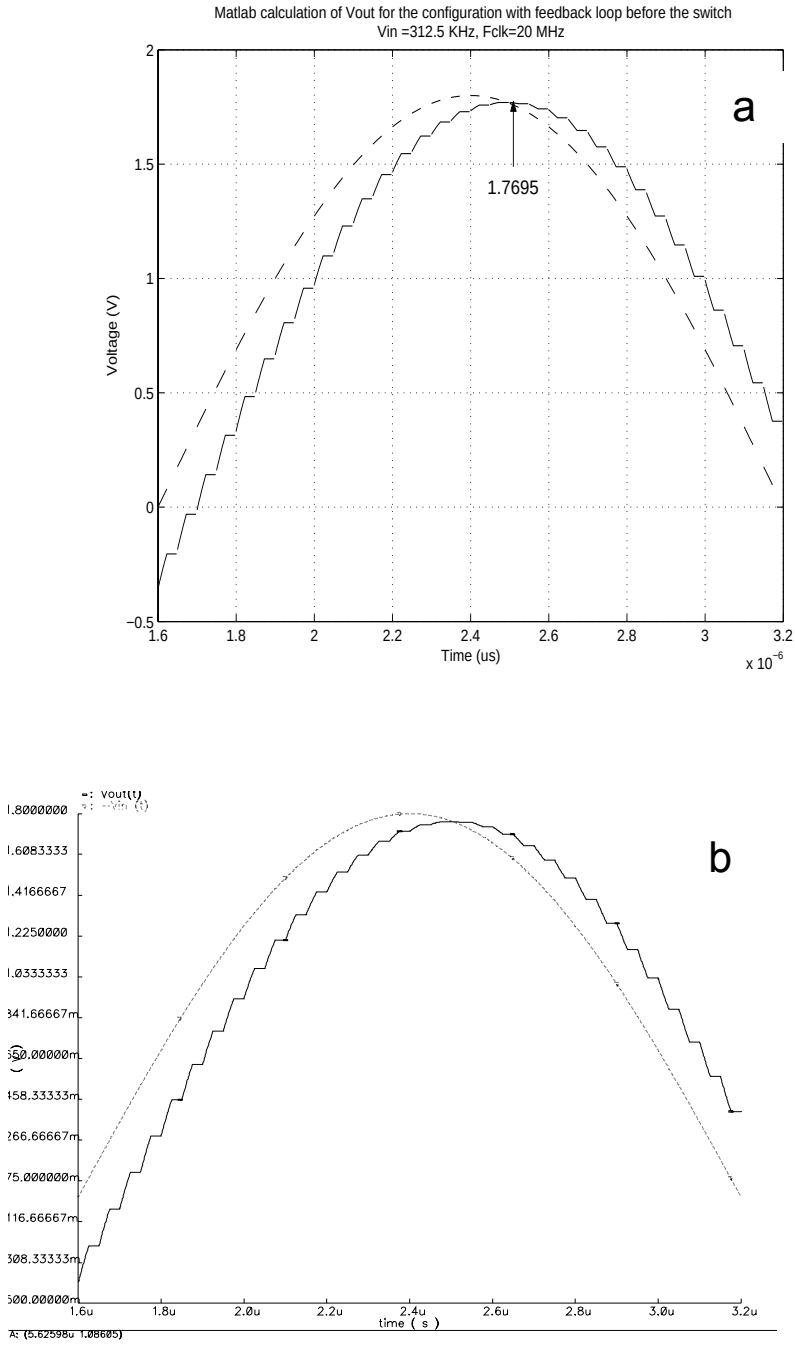


Fig 2.6 Comparison of Matlab calculation and Cadence simulation of $v_{out}(t)$ for the configuration in Fig. 2.5. a) calculated $v_{out}(t)$b) simulated $v_{out}(t)$.

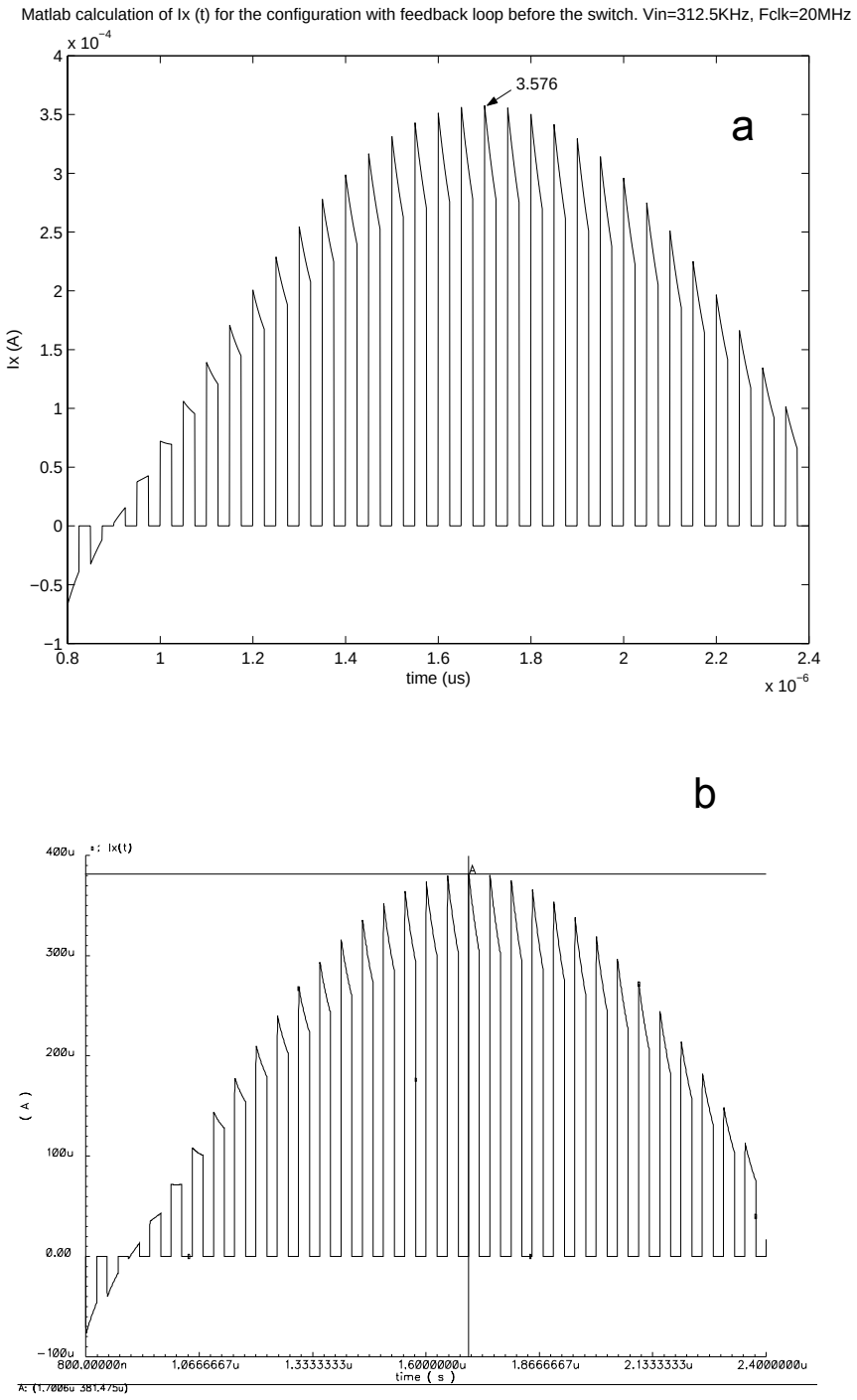


Fig 2.7. Comparison of Matlab calculation and Cadence simulation of $i_x(t)$ for the configuration in Fig. 2.5. a) calculated $i_x(t)$ b) simulated $i_x(t)$.

3 Automatic Duty-cycle Tuning Scheme

3.1 Existing Tuning Techniques

As mentioned in Chapter 1, the main drawback of MOSFET-C filters is the inaccurate RC-constant realization due to process variations, temperature drift and aging, and because the cut-off frequency depends on the matching of different types of elements (*R* and *C*). This problem is magnified in modern short-channel processes because it is more difficult to get precise physical edges for elements with smaller sizes. For most MOSFET-C filter designs, it is necessary to design an on-chip automatic tuning circuit to overcome this problem. However, in MOSFET-C filters it is not possible to trim the cut-off frequency by varying the bias current like in G_m-C filters. The values of the capacitors or resistors have to be adjusted. Some typical tuning techniques include using trimmed resistors [23], capacitor arrays [24], and varactors [25]–[27]. Each technique has its own advantages for specific applications. Nevertheless, the most commonly used approach is to tune the resistance of a MOSFET by adjusting its gate voltage.

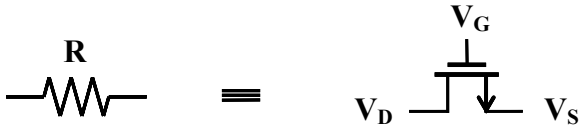


Fig 3.1 A MOSFET resistor.

A MOSFET transistor can be operated in triode region or saturation region depending on the terminal voltages. In the triode region, the transistor is equivalent to a resistor. The MOSFET resistor in Fig 3.1 has an on-resistance (R_{on}) that is inversely related to V_{gs} as given by

$$R_{on} = \frac{1}{\mu C_{ox} W/L(V_{gs} - V_{th})} \qquad \text{(Eq. 4.1)}$$

3.1.1 Direct and indirect tuning

On-chip automatic tuning strategies may be separated into categories: direct tuning and indirect tuning [28], [29]. In direct tuning, a reference signal is applied to the input of the filter. The filter is tuned by comparing its output with an expected value (Fig 3.2). The filter can be very accurately tuned using this method, because the filter itself is tuned to the accurate reference. No mismatch problem exists for this kind of tuning. However, interruption of the filter operation when the filter is being tuned is inherent because the filter has to be taken offline periodically by on-chip switches and inserted in the automatic tuning loop. Therefore this tuning approach is not good for applications where an uninterrupted filtering operation is necessary. Extra circuitry can be added to cause the circuit to appear as if the operation were uninterrupted, which will increase the complexity of circuit implementation and cost [3]. The application of direct tuning is very limited in actual circuit implementations [28, 30].

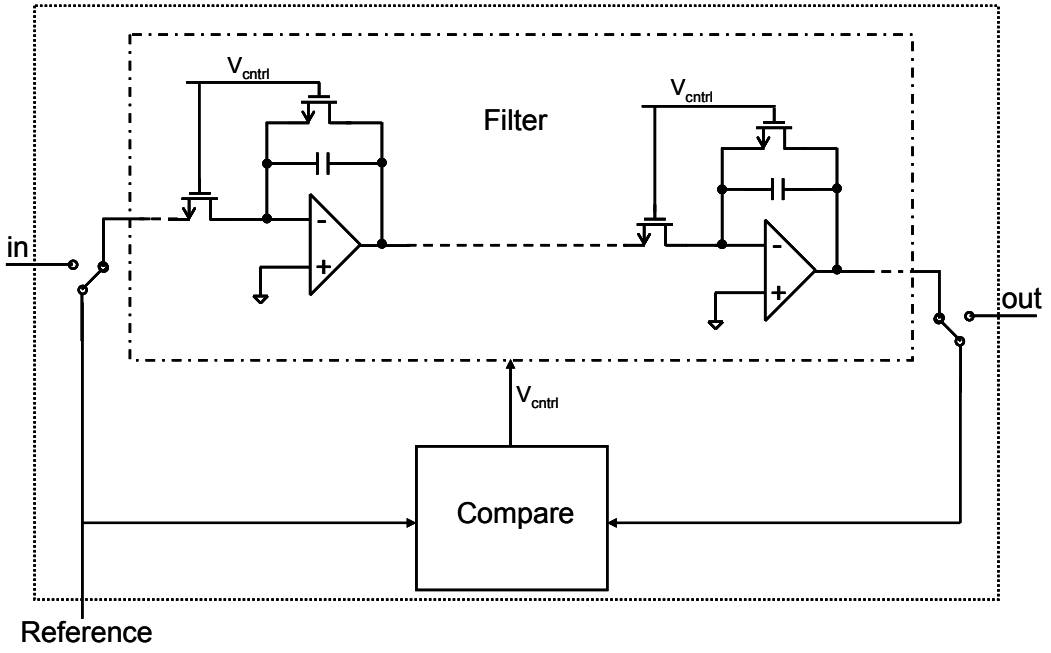


Figure 3.2 A block diagram for a direct tuning scheme (reused drawing from [31] with author's permission).

Indirect tuning is based on the master-slave approach in which a master circuit with similar time constants as the actual filter-also (called slave), is tuned to track an external reference, and the tuning signal is indirectly applied to tune the slave (Fig. 3.3). This scheme automatically corrects for the variations of both resistances and capacitances, and requires no initial adjustment. In contrast to the direct tuning, the filter is always operational even when it is being tuned [28]. Indirect tuning is advantageous over direct tuning because of its inherent setup for background adjustment [3].

In master-slave tuning, the master (reference) block can be a replica of the slave (main filter) block or a replica of one basic cell of the slave. The output of

the master block is observed and is used to correct for the errors (RC time constant variation) in the master and the slave. The master must be accurately modeled such that it will have all the performance criteria of the main filter. The main drawback of master-slave tuning resides in the required matching relationship of the master and the slave blocks, which relies heavily on tight component matching between the two circuit blocks. Any mismatch between the master and the slave will directly affect the accuracy of the desired -3dB corner frequency of the filter (the slave).

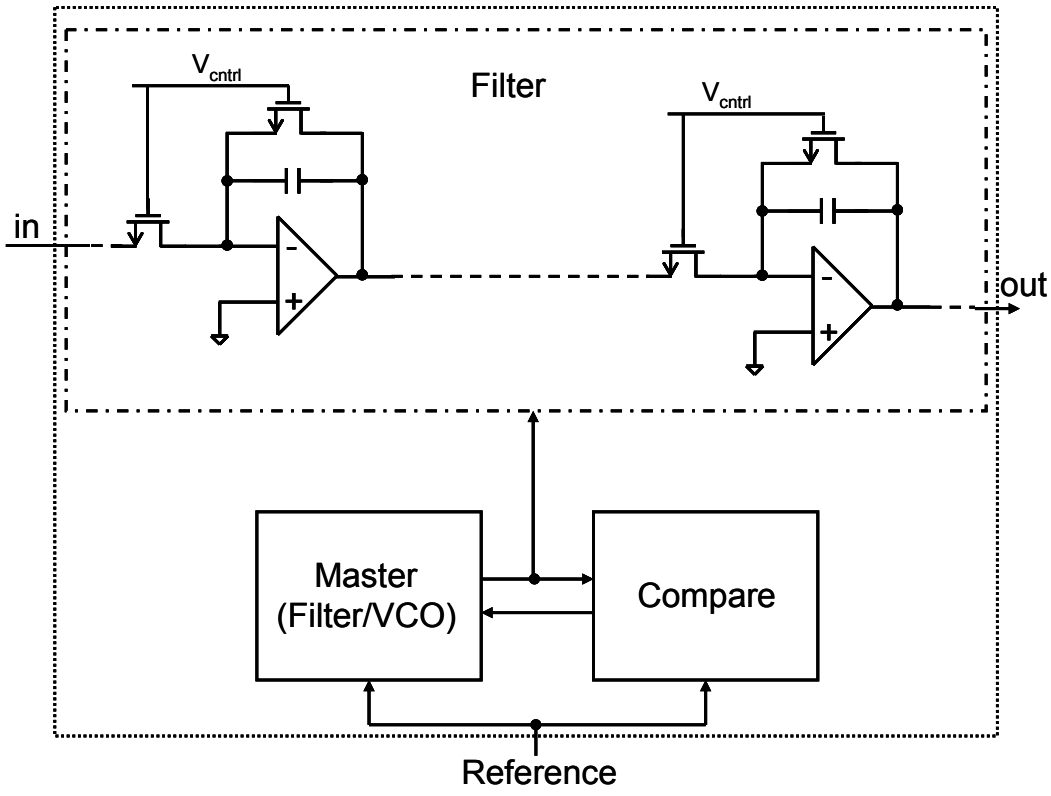


Figure 3.3 A block diagram for an indirect tuning scheme (reused drawing from [31] with author's permission).

3.1.2 Application of switched-capacitor circuit in automatic tuning

The implementation of master-slave tuning can take different forms based on the operational circuit in the master block. There are several common implementations, including RC time-constant-based tuning, transconductor-based tuning, PLL-based tuning, and Q-tuning [31].

In RC time-constant-based tuning, a reference is required to provide an accurate RC time constant. One approach is to take the advantage of the accuracy of a switched-capacitor circuit [32], [3]. The corner frequency of a switched-capacitor filter can have an accuracy in the order of 0.1%, which is much superior than their MOSFET counterparts.

Figure 3.4 shows a tuning circuit using a switched-capacitor circuit as the reference branch. The switched-capacitor branch is equivalent to a resistor, $R_{eq} = 1/(f_{clk}C_1)$, where f_{clk} is the clock frequency. The time constant realized by the switched-capacitor circuit is therefore equal to $C_2 / f_{clk}C_1$. At the output of the opamp, the difference between the R-MOSFET branch and the switched-capacitor branch is detected, and used to generate a variable gate voltage, V_G, through a control block. V_G is tuned until the RC constants of two input branches match each other.

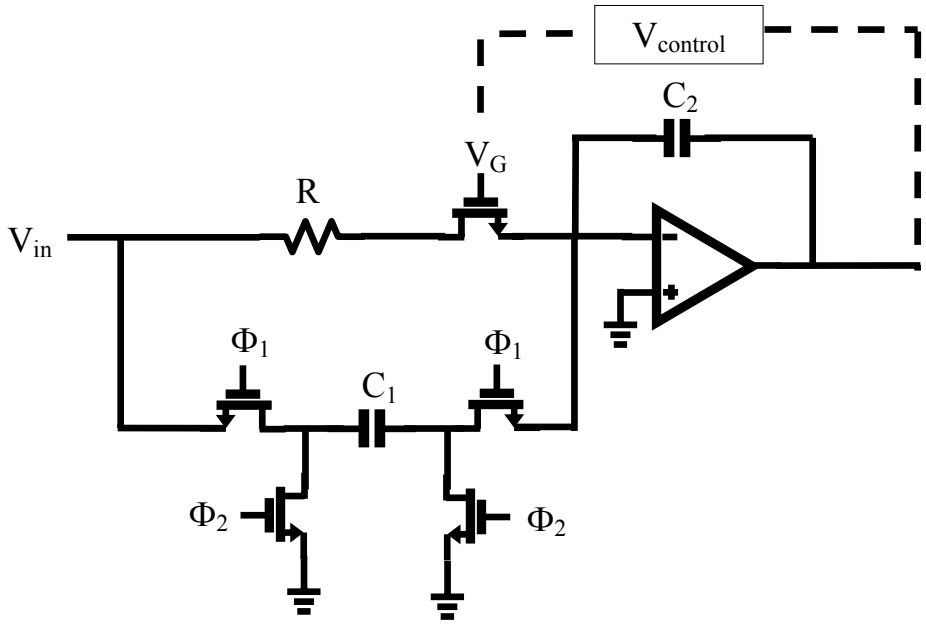


Figure 3.4 Tuning a R-MOSFET filter to a switched-capacitor branch.

3.2 Automatic Duty-Cycle Tuning Scheme

The purpose of this study was to build a filter that will have the simplicity of an R-MOSFET-C filter and the accuracy of a SC filter. To obtain the accuracy, a novel automatic tuning scheme is proposed. The fundamental difference between this tuning technique and existing techniques is that the MOSFET transistor is not used as a resistor, and there is no change in the gate voltage involved in the tuning. Instead, the MOSFET transistor functions as a switch, the operation time of which (duty cycle) is tuned to change the corner frequency of the filter.

The master-slave tuning configuration is used for the whole filter design, and includes three main blocks (Fig 3.5). This chapter discusses the master circuit

and the clock generator. The main filter block (slave) will be described in the next chapter.

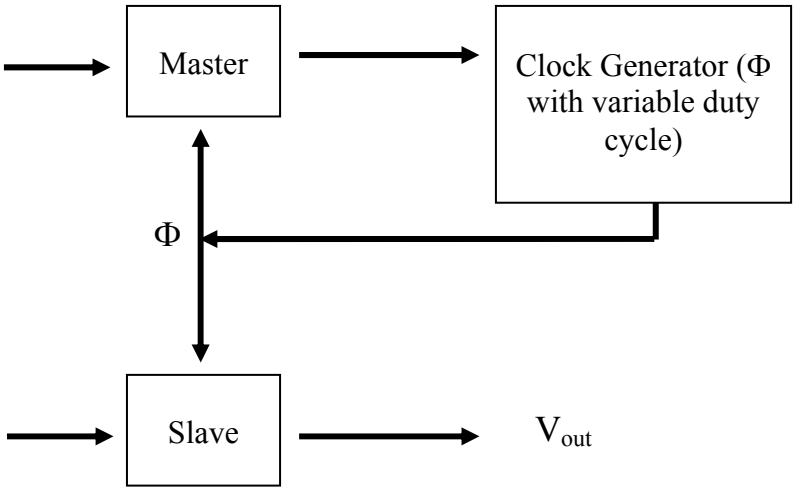


Fig 3.5 Block diagram for the filter design.

3.2.1 Master circuit

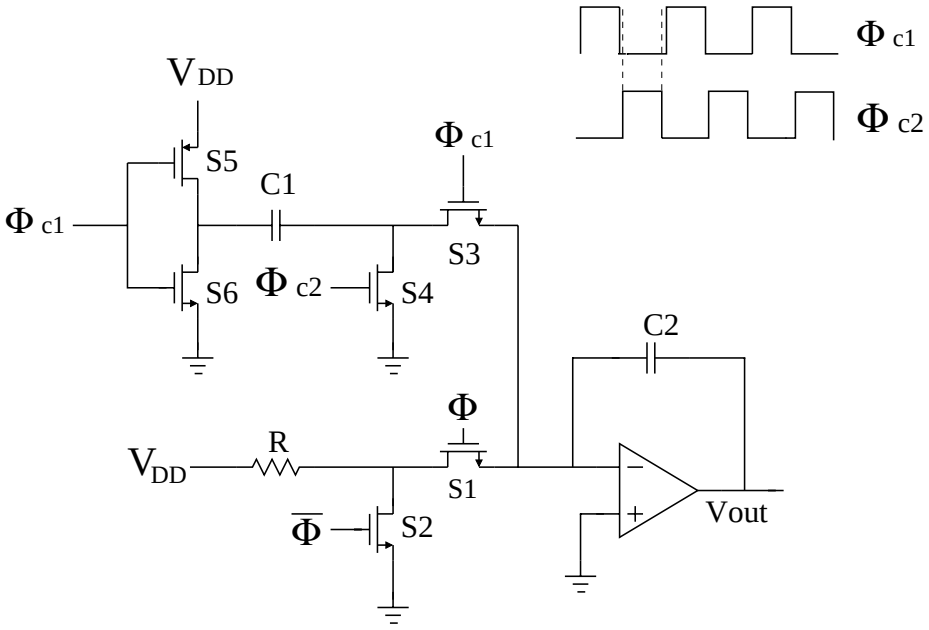


Fig 3.6 Circuitry in the master block.

As mentioned before, the automatic duty-cycle-tuning scheme uses a switched-capacitor circuit with an accurate time constant C_2/f_cC_1, as a reference for the rest of the circuit (Figure 3.6). The resistive branch uses similar components to that of the main filter circuit. The switched-capacitor branch is non-inverting, and it is controlled by fixed clocks (Φ_{c1} and Φ_{c2}), while the resistive branch is inverting, and controlled by an adjustable clock (Φ). Both paths are providing currents to the integrator with opposite polarities. Therefore V_{out} will be driven positive if the switched-capacitor branch provides more current, and negative if the resistive branch provides more current. The balance will be achieved by tuning the duty cycles of Φ and $\overline{\Phi}$ based on the output V_{out} of the opamp. Note that the function of the S5 and S6 switches is similar to the two input switches in Fig 3.4, but they do not suffer from low-voltage problems because the input of this branch takes the value of either 0 or V_{DD}. Some design issues will be discussed later.

3.2.2 Clock generating block

The variable-duty-cycle (VDC) clock generator consists of a comparator, a NAND gate, and an SR latch (Fig 3.7). As mentioned above, the output V_{out} of the opamp in the master block will be 0 if the R-MOSFET branch is providing the same current as the switched-capacitor branch. Therefore, a comparator can be

used to compare V_{out} with zero and determine whether the time constants of the two branches match.

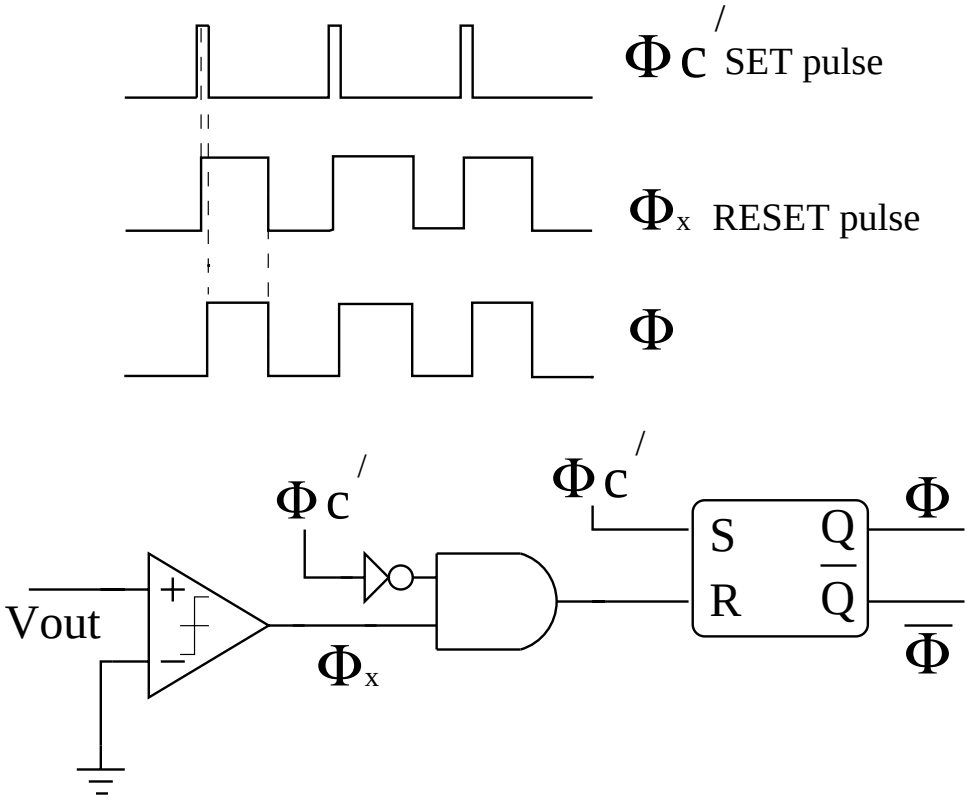
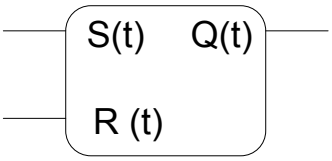


Fig 3.7 Variable-Duty-Cycle (VDC) clock generator.

The input of the comparator will take positive or negative values based on which branch is providing more current. When the switched-capacitor branch is providing more current, the duty cycle for the switch S1 needs to be increased, and vice versa. The output of the comparator is a digital signal that sets the roll-off edges for the clock Φ.

An SR latch is used to create the VDC clock Φ and Φ bar. A SET pulse (Φ_c' in Figure 3.7) is necessary to turn Φ on. The SET pulse is obtained from the master clock. The clock phase of Φ turns off to the SR latch with a RESET pulse which is provided by the comparator. The SET pulse is made very narrow because its width determines the minimum duty cycle.



Q(t): past output
Q(t′): present output
×: not applicable

S (t)	R (t)	Q (t)	Q (t′)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×

Fig 3.8 Operation logic for the SR latch.

The logic function of the SR latch requires that the two inputs must never be high at the same time (Fig 3.8). A NAND gate is used to ensure that the output of the comparator and the SET pulse are not high at any time.

4 High-Q Biquad Filter Design: Transistor-Level Realization

4.1 Design of a Differential High-Q Biquad Filter

4.1.1 Biquads

A biquad stage is a very commonly used building block in higher-order filter designs. It realizes two poles and two zeros. There are many different realizations of biquad filters, based on the requirements of the filter response. The filter design in this study is based on a high-Q biquad filter originally proposed by Brackett and Sedra [33] (Fig 4.1).

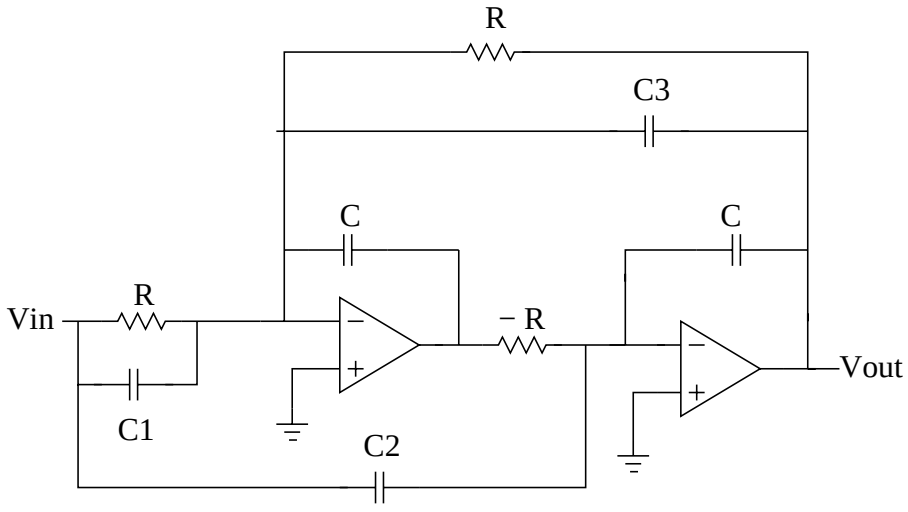


Figure 4.1 High-Q biquad filter design: RC realization.

Note that a negative resistance is required for this single-ended configuration to function. As pointed out before, this configuration also suffers from inaccurate corner frequency and low tunability.

A switched-capacitor counterpart of this structure was also proposed [34], [35] (Fig 4.2). It realizes the transfer function much more accurately, at the price of increased complexity.

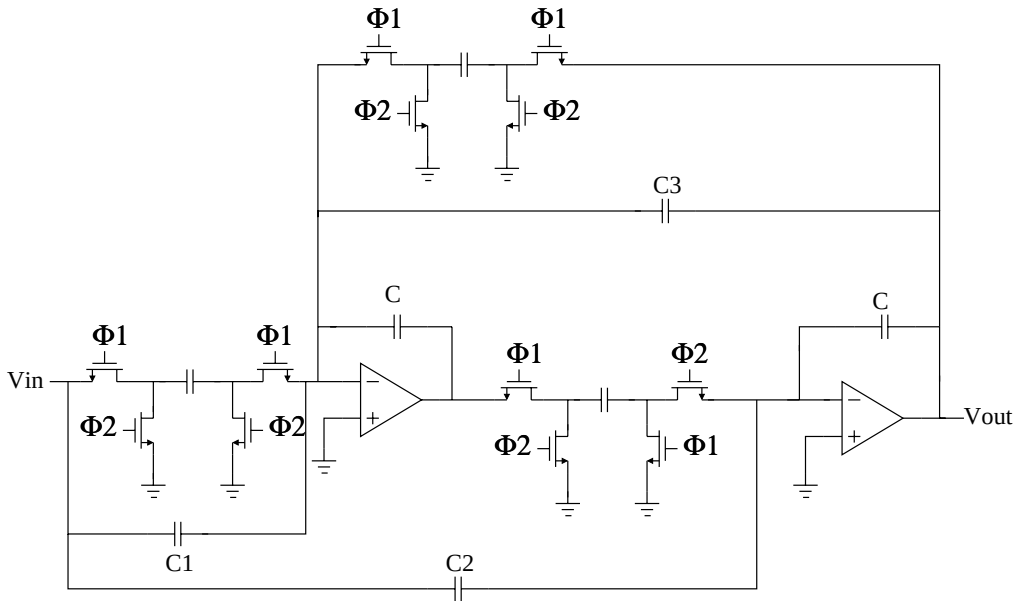


Fig 4.2 High-Q biquad filter design: SC realization.

This circuit is nearly optimum for the great majority of filtering applications, with the exception of phase equalizers [12].

4.1.2 Design of a high-Q biquad filter in a switched-R-MOSFET-C (SRMC) realization

A high-Q biquad filter was designed and simulated to illustrate the advantages of SRMC technique. The circuit is similar to an active-RC filter, so it takes advantage of its simplicity. The resistors are replaced with switched-R-MOSFET branches (Fig 4.3). The accuracy of the filter can be comparable to its SC counterpart owing to the on-chip automatic tuning circuit described in Chapter 3.

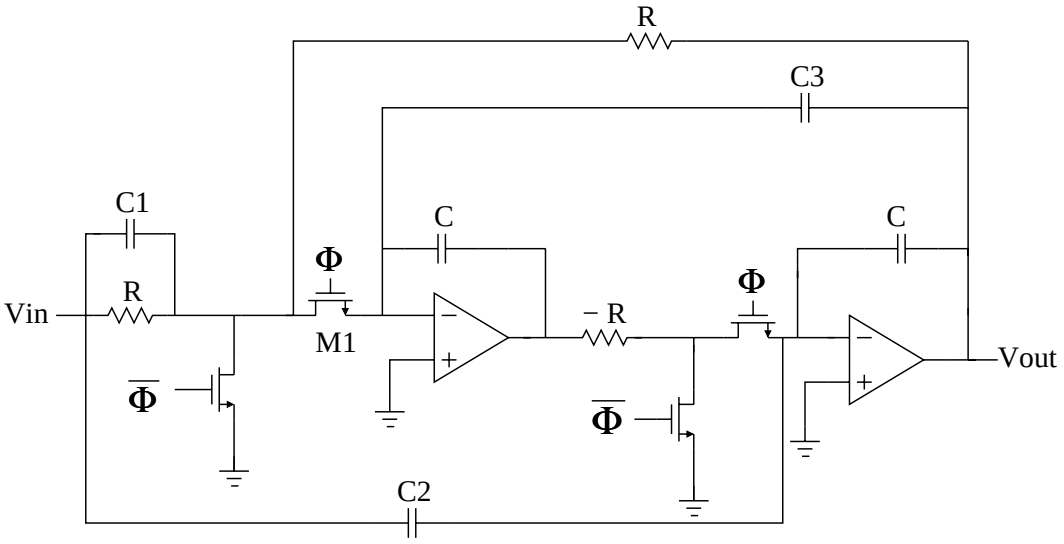


Fig 4.3 High-Q biquad filter design: SRMC realization.

For initial calculation of the transfer function, the switched-R-MOSFET branch can be considered as a resistor with its value depending on the duty cycle of clock Φ, denoted as D ($0 < D < 100\%$). The contribution of the on-resistance of the switch M1 can be ignored since R_{on} is much smaller than R. Therefore an

equivalent resistance can be defined as $R_{eq} \cong R/D$, and used in calculations of component values.

The designed filter has a low-pass transfer function with a corner frequency f_c of 100 kHz and a Q-factor of 4. The element values can be determined by comparing the transfer function obtained using Matlab with the one calculated from the circuit. However, some final adjustments will be needed through simulation because, as mentioned above, the calculation of resistance R_{eq} is just an approximation.

4.1.3 Differential configuration

The whole filter including the master and the slave part was implemented in differential configuration mainly for two reasons (Fig 4.4). The negative resistance required for the biquad filter can be easily realized by swapping positive and negative connections in the differential configuration. Noises from various sources are converted into common-mode voltage and get cancelled in a differential circuit.

For maximum tuning range, the filter is designed in a way such that the duty cycle of Φ for nominal operation is around 50%. The element values for the designed filter are given in Table 4.1. Note that C_1 and C_2 shown in Fig 4.3 are not needed in the filter because these two capacitors have zero value for the specified LP transfer function.

Table 4.1 Specifications and element values for the designed filter

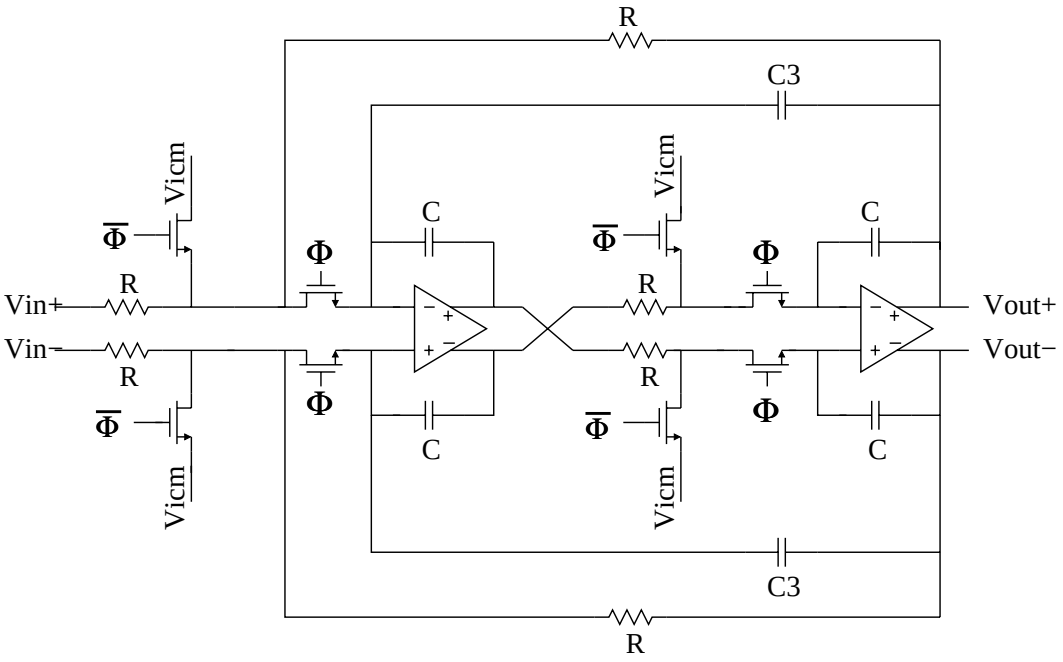
f_{clk}	f_c	Q	R	C	C_3	C_{t1}
10 MHz	100 kHz	4	90 kΩ	8 pF	2 pF	240 fF

4.2 Transistor-Level Circuit Design: Low-Voltage Considerations

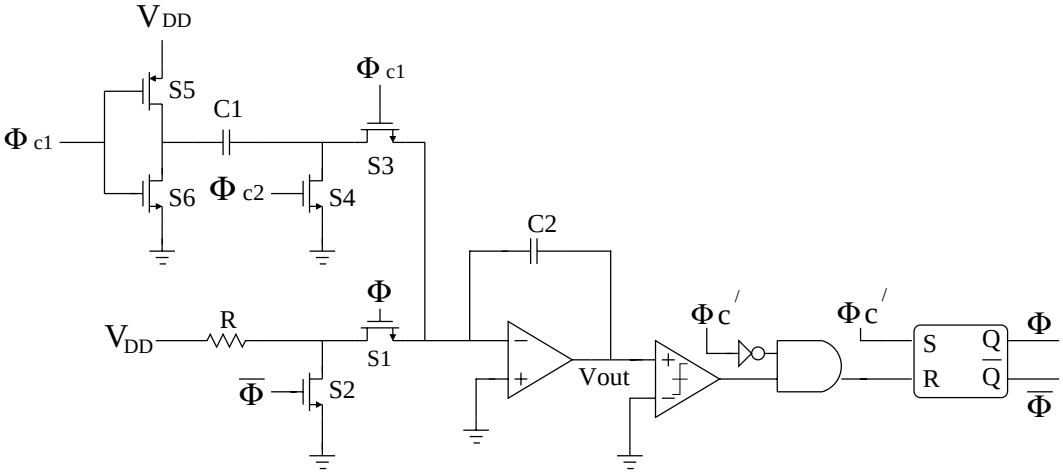
The TSMC 0.18 μm process was assumed for transistor-level circuit design. The threshold voltage V_{th} for the transistors ir this process is around 0.5V. The targeted supply voltage is 1V. Therefore the voltage overhead for circuit design is limited. As shown in Fig 4.4, there is one opamp and one comparator in the tuning block (master), and two identical opamps in the main filter block (slave). Special considerations are needed to make sure that these blocks work properly under 1-V supply voltage. Transistor-level realization of the NAND gate and the SR latch can be easily achieved using standard logic cells.

4.2.1 Biasing the input common-mode voltage of opamp for low-voltage application

For maximum voltage swing, the input and output signals need to be biased at 0.5 V, which is in the middle of the supply voltage. If the circuit is implemented as shown in Fig. 4.5, nodes V_1 and V_2 will also be biased at 0.5 V. However, in order to properly turn on the transistor M1 with a gate voltage of V_{DD}, its source and drain terminals need to be biased at a lower voltage, so that $V_{GS} > V_{TH}$.



(a) Differential high-Q biquad filter: SRMC realization



(b) Tuning circuit

Fig 4.4 Overview of the complete filter structure.

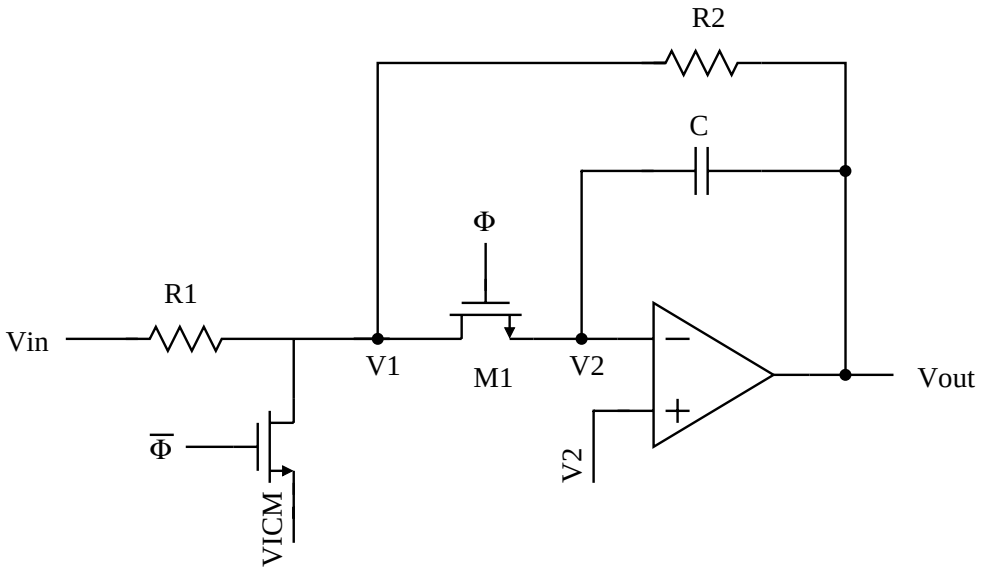


Fig 4.5 Biasing in the switched R-MOSFET-C filter structure.

One solution to this problem is to bias the node voltage V_1 at a voltage close to ground by connecting a current source I_b or a resistor R_b between this node and ground as proposed by Karthikeyan *et al.* [36] (Fig 4.6).

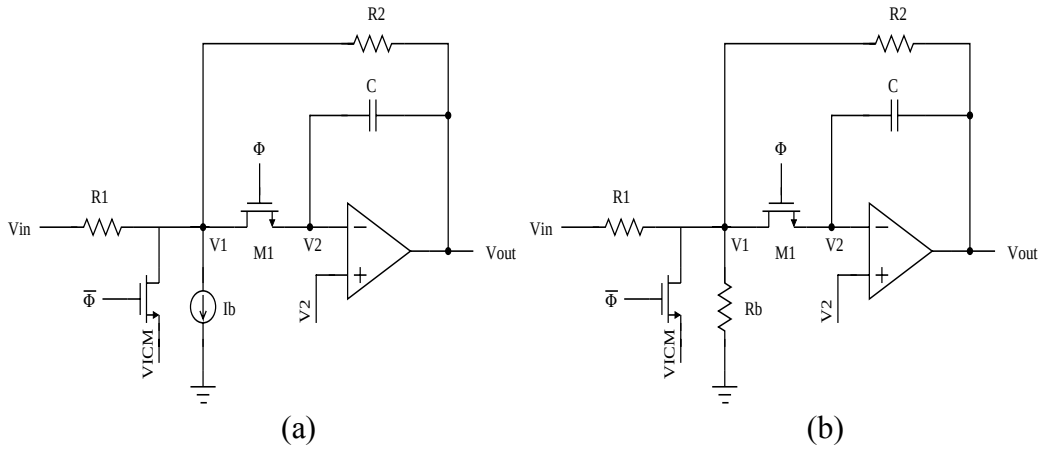


Fig 4.6 Biasing schemes that use (a) a current source (b) a resistor.

The design shown in Fig 4.6 (a) is extended into the design of the differential biquad filter. Identical current sources are connected on both sides of the differential circuit to bias the opamp input voltage near ground. Therefore the switch transistor M1 can always be turned on.

4.2.2 One volt (1-V) opamp design

The two-stage differential folded-cascode opamp is a modified version of the low-voltage two-stage Miller-compensated opamp designed by Chang [37] (Fig 4.7). A PMOS differential pair (M1 and M2) is used as the input stage. The maximum input common-mode voltage for proper operation is around 0.3 V ($V_{CMmax} < V_{DD} - V_{thp} - V_{dsat9}$). We can see that biasing the input common-mode voltage of the opamp near ground also helps with the operation of the opamp at low supply voltage. The differential output stage consists of inverters M10, M11, M12, and M13 for high output signal swing. Miller compensation is realized using capacitors *C* to stabilize the opamp.

A common-mode feedback (CMFB) circuitry has to be used because the opamp has differential outputs. A simple resistive CMFB circuit is used with the output voltage connected directly to the control gate after an inverting stage (M14 and M15 in Fig 4.7). The inverting stage is necessary for this two-stage (even number of stages) opamp to ensure the negative common-mode feedback. There is no additional circuit for extra gain in the common-mode loop, which makes this CMFB structure notably simple. The output common-mode voltage can be easily

adjusted by changing the size ratio of M14 and M15. The only factor that restricts the magnitude of the output common-mode voltage is the threshold voltage V_{th} for M14, which is around 0.5V. However, this CMFB does not have a reference voltage, which limits its flexibility. To avoid turning off M14, the output common-mode voltage is biased at 0.45 V for the opamps used in the main filter structure.

The designed opamp has a DC gain of 62 dB, a unity-gain bandwidth of 60 MHz, and a phase margin of 77° (Fig 4.8). The relative high DC gain of the opamp results in a high feedback loop gain at low frequencies, which helps suppressing nonlinearities in the filter [3], [31].

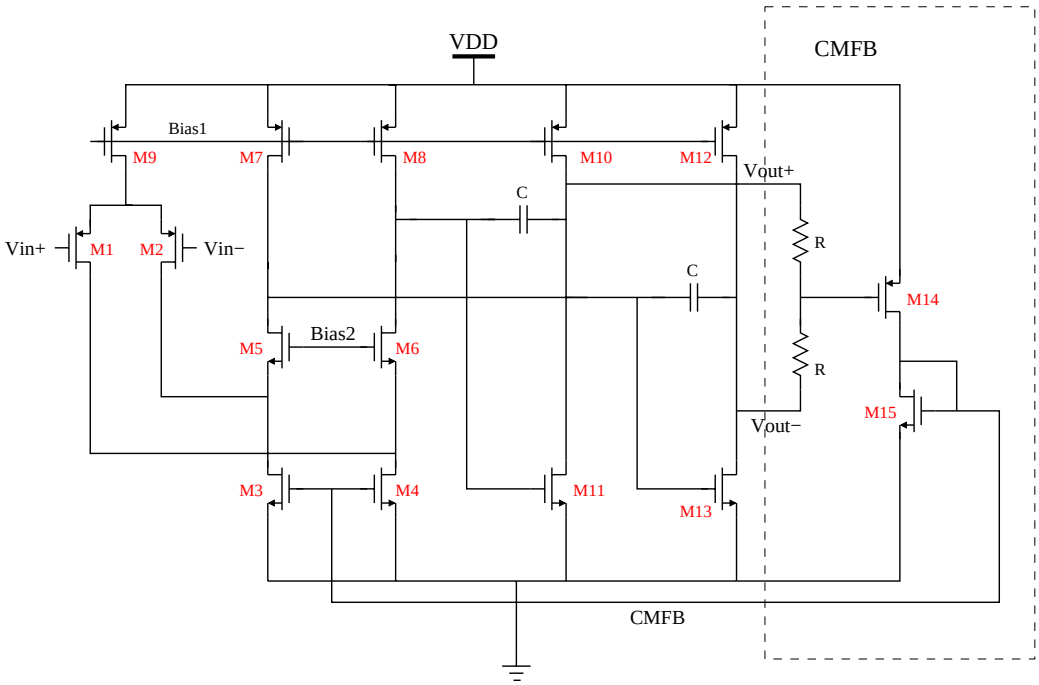


Figure 4.7 Two-stage differential opamp design with 1-V supply voltage.

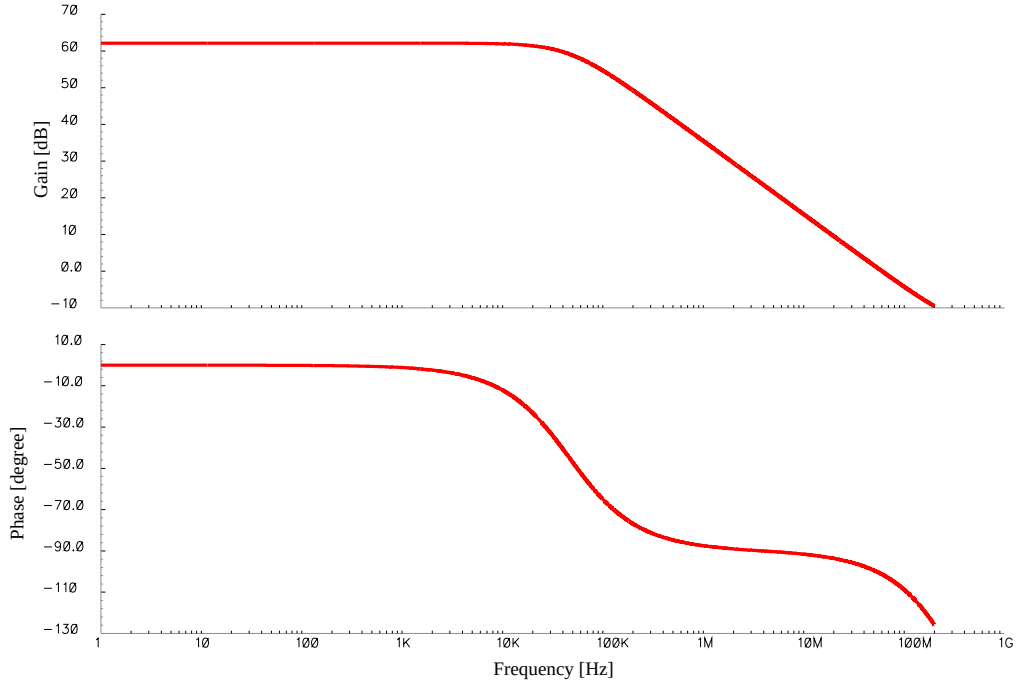


Fig 4.8 AC response of the designed opamp.

4.2.3 Comparator design

As described in chapter 3, a comparator is required for the tuning circuit. Most existing comparator designs have dynamic operation, meaning that they are enabled by a clock signal. Usually, some form of a regenerative latch is employed. The purpose is to detect the sign of the input signal at a given instant. For this work, in contrast, it is necessary to determine the instant when the comparator input signal crosses zero, so that a clock with variable duty cycle can be generated. Therefore, it is not feasible to use a clocked comparator. A simplistic approach for realizing a non-clocked comparator is to use an open-loop

opamp (Fig 4.9). The main drawback of this approach is its slow response time since the opamp output has to slew for a large output step and it will settle too slowly [12].

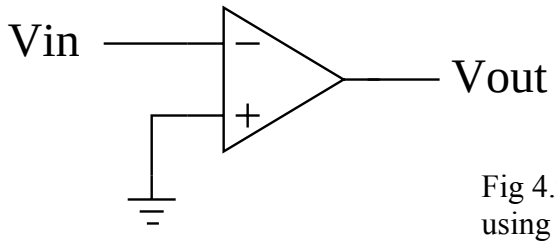


Fig 4.9 A simplistic approach of using an open-loop opamp for a comparator.

The gain requirement for the comparator in this study is not high, therefore a simple one-stage opamp is used its realization (Fig 4.10). The differential outputs from the opamp are directly connected to the differential input stage of the comparator and compared with each other (Fig 4.11). The comparator itself consists a PMOS input pair (M1 and M2), a current mirror (M3 and M4) for converting the opamp output to single-ended, and two inverters to convert the opamp output into pulse form that takes value of either 0 or V_{DD}. There is no compensation capacitor required in this circuit, so the speed limiting is minimized. The designed comparator has a gain of 22 dB and a phase shift of 6.5° (a delay of 1 ns) at 10 MHz (Fig 4.12).

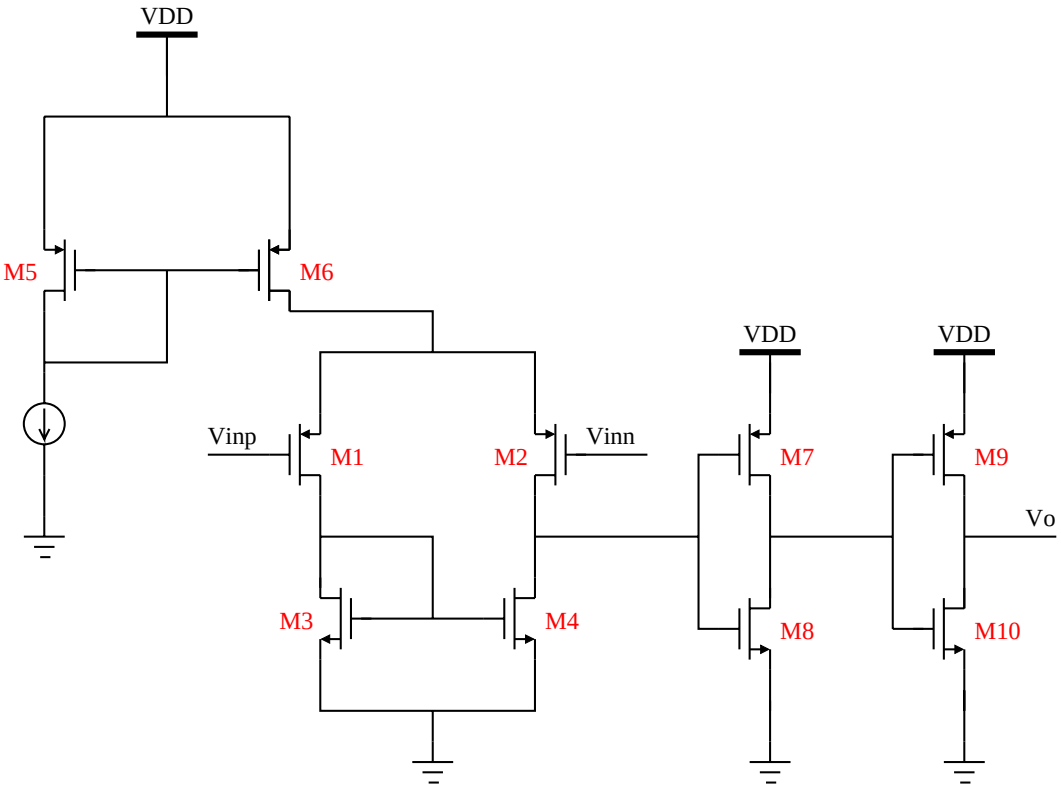


Fig 4.10 Comparator design with 1-V supply voltage.

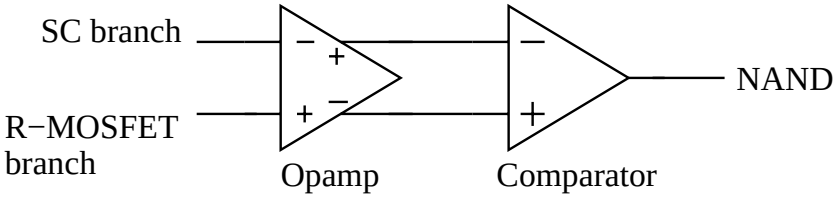


Fig 4.11 Block diagram of a part in the tuning circuit that includes the opamp and the comparator.

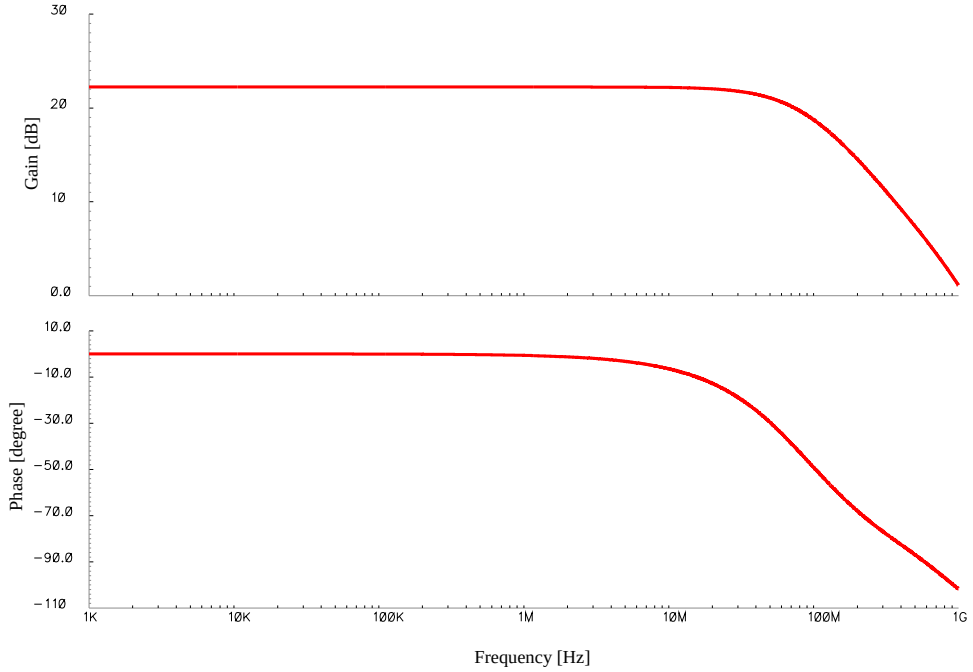


Fig 4.12 AC response for the designed comparator.

Similar to the design of the opamp shown in Fig 4.7, there is a limitation for the maximum input common-mode voltage in the comparator. In this case it is around 0.3 V. Since the input stage for the comparator is connected to the output of an opamp in the tuning circuit, it will not work properly if the output common-mode voltage for the opamp is too high. Therefore, the opamp used in the tuning circuit is changed slightly from that used in the main filter with its common mode output voltage set at 0.3V.

5 Simulation Results and Discussion

5.1 Frequency Response

5.1.1 Periodic AC Analysis (PAC)

Due to the discrete-time nature of this filter, determining its frequency response by traditional methods would require many lengthy transient analyses with one simulation for each frequency point. A more efficient way to find the frequency response is the "Periodic AC Analysis" (PAC) simulation method [38]. Transient analysis results were found to agree with the PAC analysis results. The frequency response for the designed filter was simulated using PAC analysis and is shown in Fig 5.1.

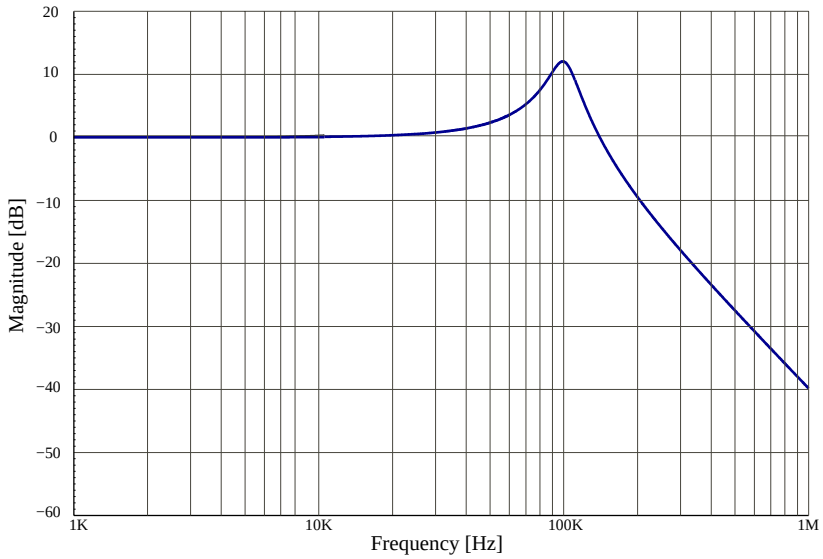


Fig 5.1 Frequency response of the designed filter with a corner frequency f_c = 100 kHz and a Q-factor of 4 (12 dB).

5.1.2 Accurately tunable corner frequency

The corner frequency of the biquad filter can be accurately tuned by changing the equivalent RC time constant of the switched capacitor path. When the capacitor C_{t1} in the reference branch (Fig 4.4) has a value of 240 fF, the designed filter has a corner frequency of 100 kHz (Fig 5.1) corresponding to the clock duty cycle of 50%. The actual corner frequency of the filter was found to be 50 kHz, 100 kHz and 150 kHz, respectively when C_{t1} is set to 120 fF, 240 fF or 360 fF (Fig 5.2). The corresponding duty cycle was 25%, 50%, and 75% respectively.

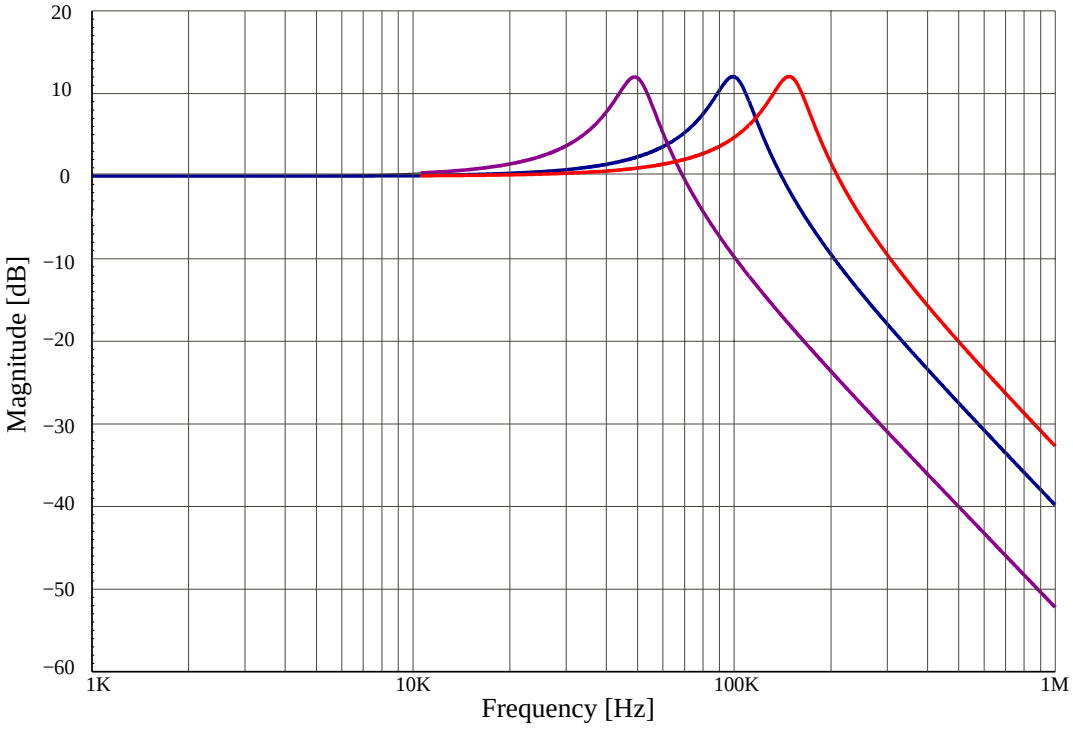


Fig 5.2 Three frequency responses of the biquad filter tuned to different duty cycles.

5.1.3 Fast automatic tuning

Another important consideration is the speed of the automatic tuning circuit. This can be examined by simulating the transient response of the circuit. Fig 5.3 illustrates the time-domain operation of the tuning circuit with the clock duty cycle abruptly changed from 25% to 75%. The change is realized by switching the reference branch that contains a capacitance of 120 fF to another reference branch that contains a capacitance of 360 fF at 500ns. For such a big change (50%) in duty cycle, it only takes one clock period for the circuit to lock to the new time constant, suggesting a capability for the circuit to rapidly switch between different corner frequencies.

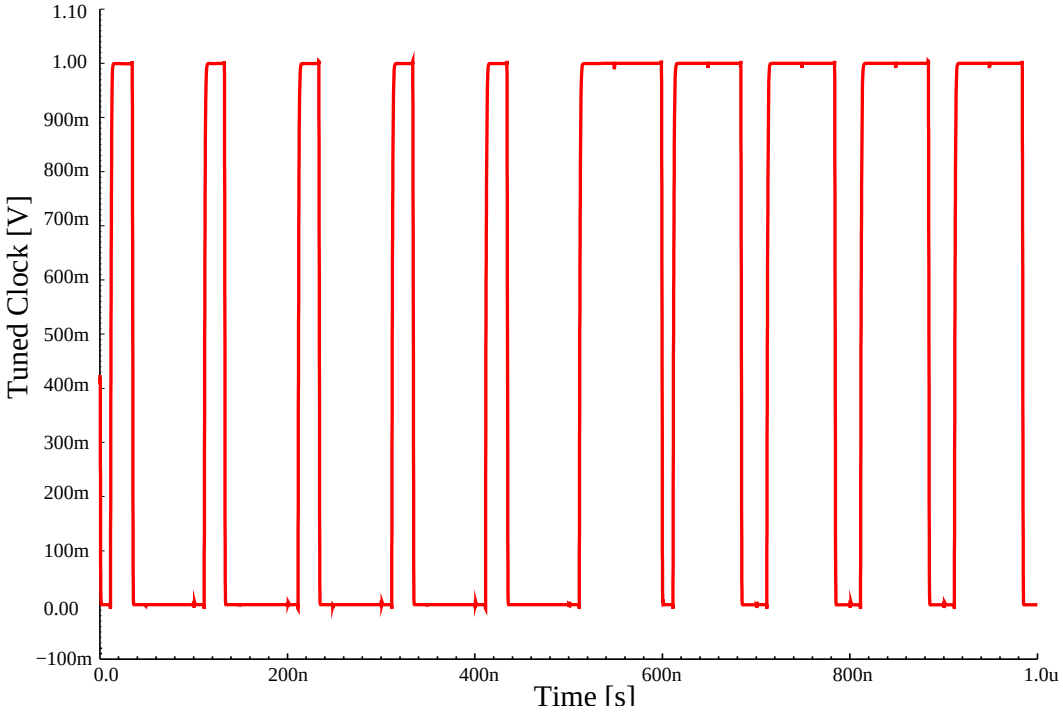


Fig 5.3 Automatic clock duty-cycle tuning.

5.2 Harmonic Distortion

5.2.1 Simulation methods

A common technique for characterizing the performance of a mildly nonlinear system is to analyze its harmonic distortion. Generally one (single-tone test) or two sine (cosine) waves (two-tone test) are applied to the system, and then the output signal spectrum is analyzed for distortion products.

In the case of single-tone excitation, the harmonic-distortion components are located at integer multiples of the source frequency. The waveforms are represented by a Fourier series whose coefficients are calculated by applying the discrete Fourier transform (DFT), usually through the use of the fast Fourier transform (FFT) algorithm [39]. Total harmonic distortion (THD) is a specification often used as a single number representation of the harmonic distortion($THD = \sqrt{\frac{\sum_{i=2}^{N} h_i^2}{h_1^2}}$, where h_1 is the amplitude of the fundamental and the $h_{2...N}$ are the amplitudes of the harmonics). It is the root mean square (RMS) sum of the individual harmonic distortions. The even-order harmonic components are caused by asymmetrical errors and will be cancelled in fully-differential circuits owing to their symmetrical nature. The odd-order harmonics are caused by symmetrical errors, and cannot be cancelled in differential circuits.

For two-tone analysis, the input consists of two sinusoids closely spaced in frequency. The resulting output waveform will contain a large number of closely spaced mixing products, grouped at integer multiples of the center frequency, representing the intermodulation distortion (IMD) of the system. IMD is another way of measuring the nonlinear distortion.

In this study, the single-tone method was used for THD analysis. The two-tone test was also applied and the spurious free dynamic range (SFDR) was measured to represent the IMD distortion of the designed filter.

5.2.2 Simulation results

For single-tone test a sine wave signal $V_{in}(t) = A\sin(2\pi f_t t)$ of an appropriate amplitude A is applied to the filter input. It has been shown that the optimum frequency f_t of the test signal is of the form Lf_s / N, where f_s is the sampling rate (f_{clk} in this study), N is the number of FFT samples (power of 2), and L an integer such that L, N are relative prime numbers [40]. Based on this requirement, the test signal was selected to have a frequency of 9.765625 kHz for the 10 MHz clock. A typical DFT plot is presented in Fig 5.4 fore A = of 200 mV ($V_{p\text{-}p}$ = 400 mV). The high-Q factor is also reflected in the noisespectrum.

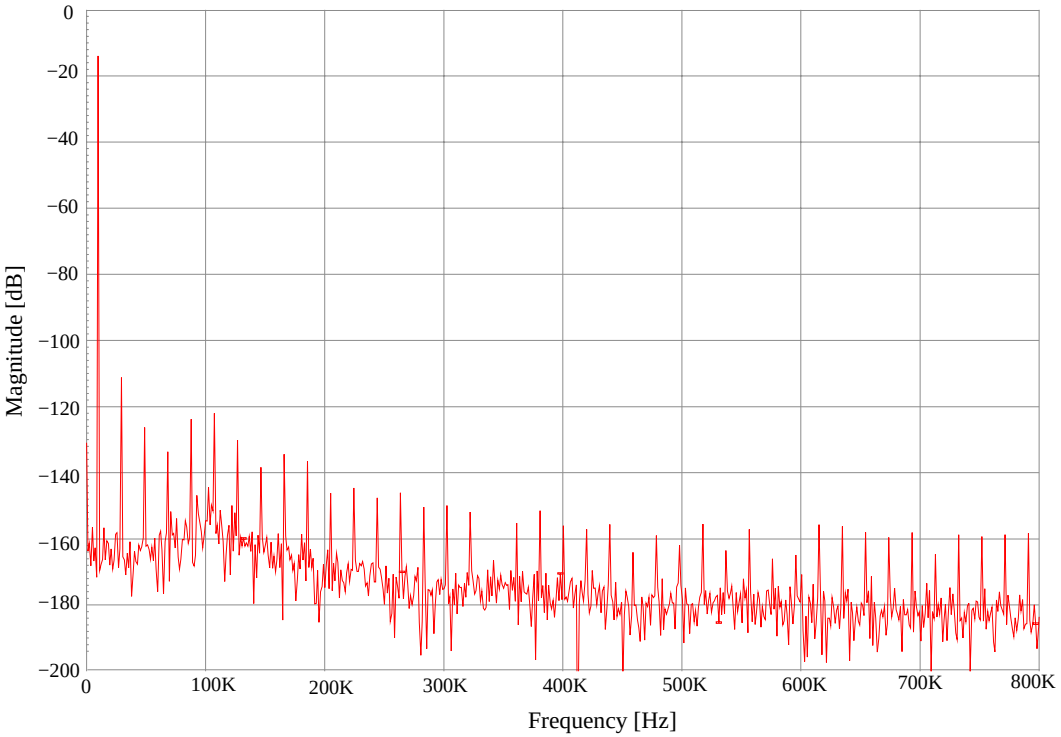


Fig 5.4 DFT plot of the filter output with a 9.765625 kHz signal frequency.

The THD for the simulation shown in Fig 5.4 is -96.5 dB with the largest harmonics below -110 dB. For a conventional MOSFET-C filter, a THD of -40 to -60 dB is achievable, and it is very difficult to exceed the -60 dB ceiling. The low THD obtained for the designed filter illustrates the potential of this design in high-linearity applications.

The THD is found to relate to the amplitude of the input (Fig 5.5). For the convenience of discussion, from this point on we will use the peak-peak value ($V_{p\text{-}p}$) to represent the input voltage V_{in} and the output voltage V_{out}. For an input signal up to 1 V, a THD of -80 dB or better can be achieved. The input signal range (0 – 1 V) for high-linearity application is significant for a 1-V supply voltage

especially if we consider that the threshold voltage V_{th} for this simulation process is around 0.5 V. If the supply voltage is increased to 1.4 V, the input signal range will be increased by 0.8 V (0 – 1.8 V) with comparable high-linearity performance (Fig 5.6).

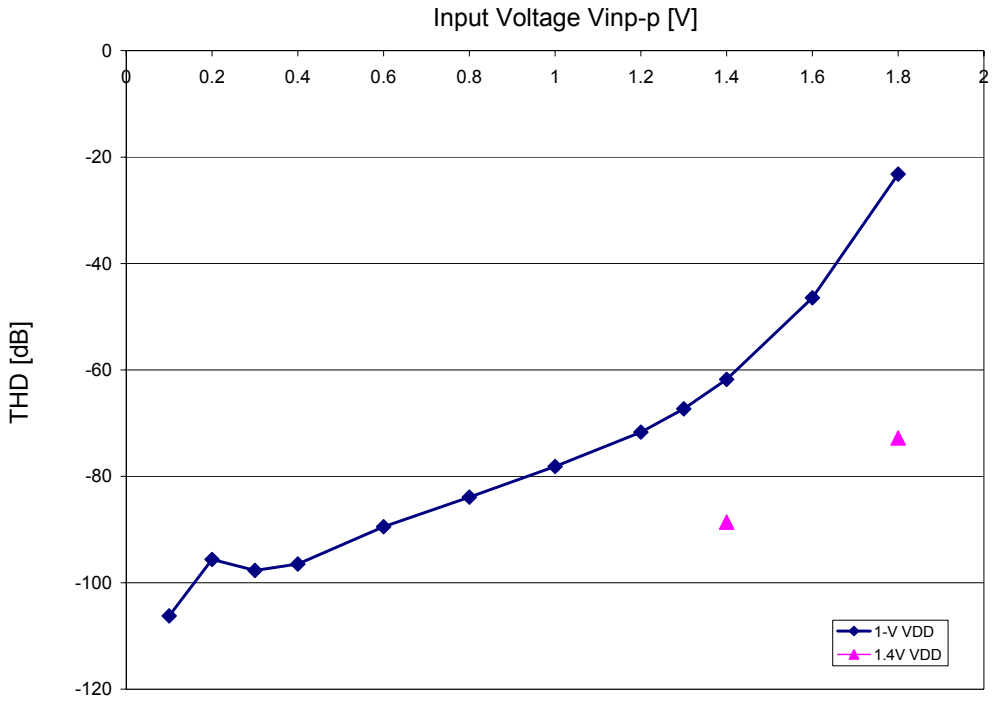


Fig 5.5 THD *vs.* input magnitude.

Note that the THD curve is almost linear when the input voltage V_{in} changes from 0.4 – 1.2 V. When the input voltage V_{in} is larger than 1.2 V, the curve becomes nonlinear due to output saturation. When the input voltage V_{in} is lower than 0.4 V, the THD results become variable since other noise sources in the circuit become dominant.

One of the main factors contributing to the high linearity of this filter is that the non-linearity of the switch is suppressed by the opamp feedback loop gain [3]. This effect is expected to be weakened when the input frequency increases. Therefore the THD performance will get worse when the frequency of the input signal increases, while maintaining the same amplitude. To verify this, the THD analysis wass carried out for a series of input signals with a constant $V_{p\text{-}p}$ of 200mV and a frequency of Lf_{clk}/N where L is 1, 3, 5, 7, or 9, and N is 1024 (Fig 5.6). Generally speaking, the effects of the loop gain on THD performance decrease when the input frequency increases. However, there is a drop in the curve that requires explanation. Careful examination of the input frequency where the drop occurs, we can see the third harmonic for that input frequency falls out of the pass band of the filter. This also adds to the suppression of harmonics.

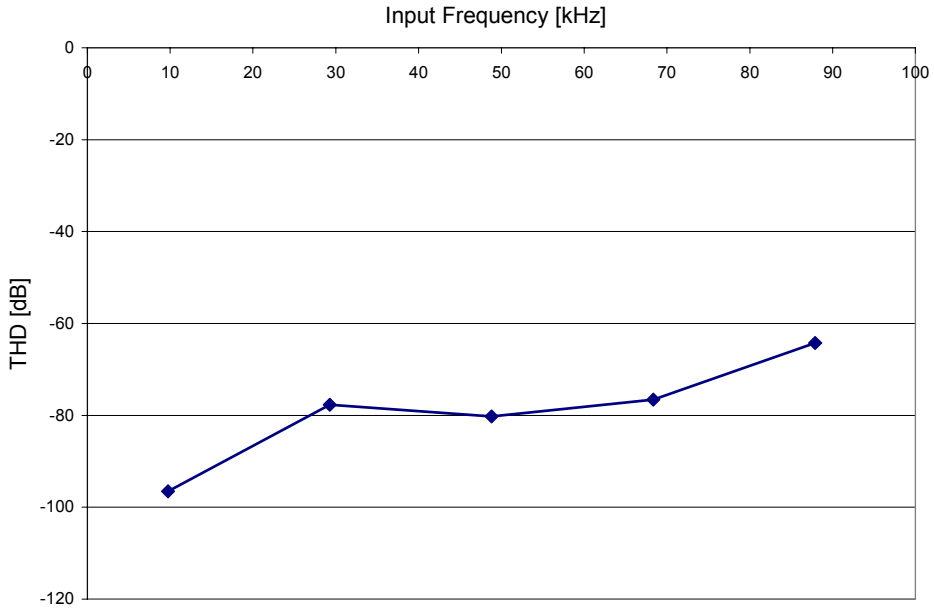


Fig 5.6 THD *vs.* input frequency.

The effect of the opamp loop gain on the filter linearity performance can also be examined by applying a two-tone test and measuring the SFDR. An ideal DFT plot for two-tone test is shown in Fig 5.7. The two input signals have frequencies at f_1-Δ and f_1+Δ, where Δ is a small value but enough to resolve the two input signals for DFT analysis. The SFDR measured at both sides of the two input signals will be the same for an ideal case.

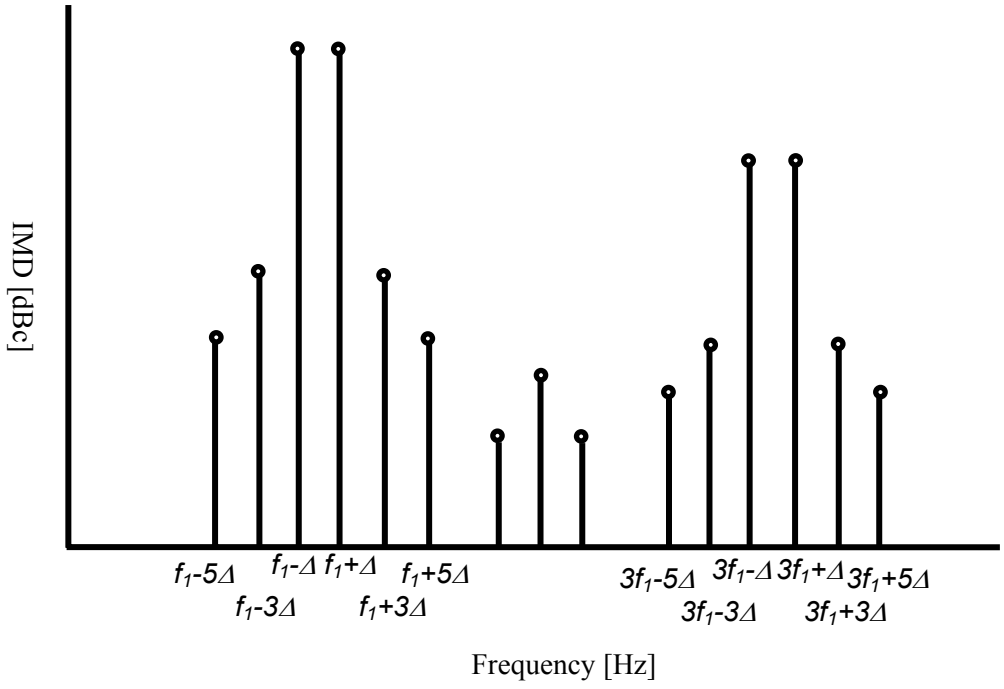


Fig 5.7 An ideal output spectra for two-tone test.

However, the output spectra will look different for the real circuit (Fig 5.8). The high-Q filter design has a peak in the response. The gain of the output starts to increase when the input frequency is higher than 20 kHz, until it arrives

at the peak (Fig 5.1). Therefore there is an inherent asymmetry in the output spectra of the two-tone test. To measure the SFDR, the worse case is considered, meaning the smallest difference between the two peaks, found at f_1 and $f_1+3\Delta$, is measured.

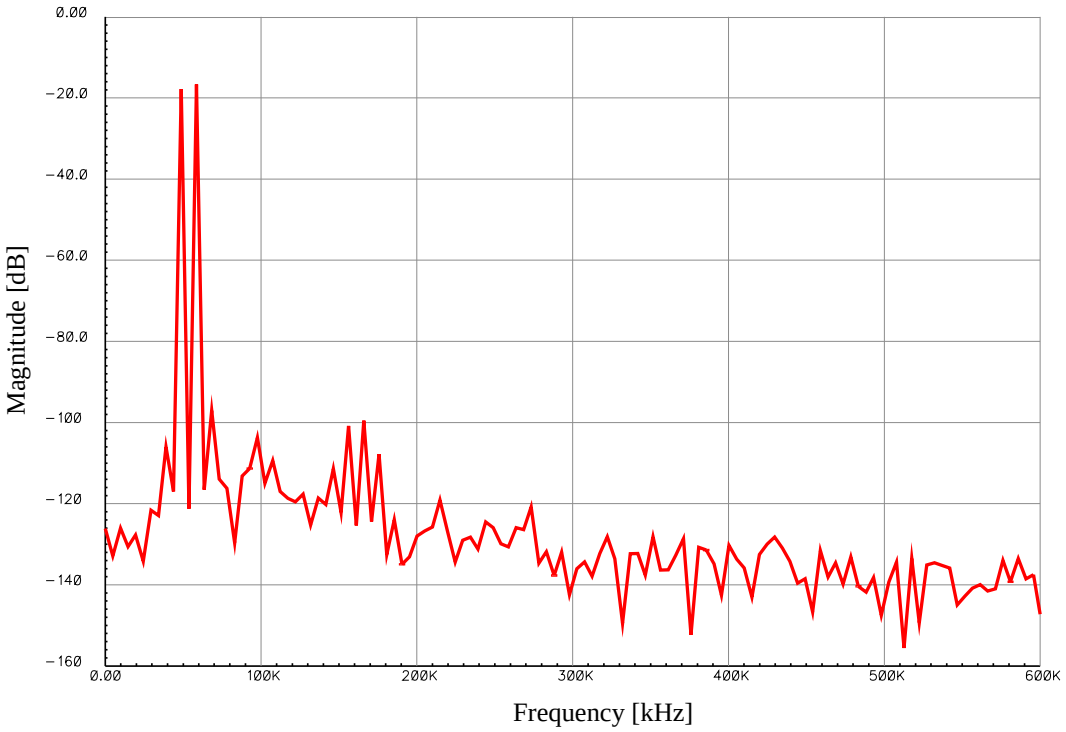


Fig 5.8 An example of the simulated output spectra for two-tone test.

For comparison with the single-tone test, a number of input frequencies similar to that used for obtaining Fig 5.6 are used with the two-tone test. The simulation shows that IMD increases almost linearly with frequency (Fig 5.9). In contrast to that obtained from the one-tone test, there is no drop in the curve observed. This is because all measurements, except the last one, are taken in the

passband. Recall that in single-tone test, the harmonics shift out of the passband once the input frequency is over a certain point. Then the distortion is suppressed by both the feedback loop gain and the filter itself. The curve shown in Fig 5.9 may reflect the suppression effect of the opamp feedback loop gain better, because the analysis was carried out in the passband for all frequencies.

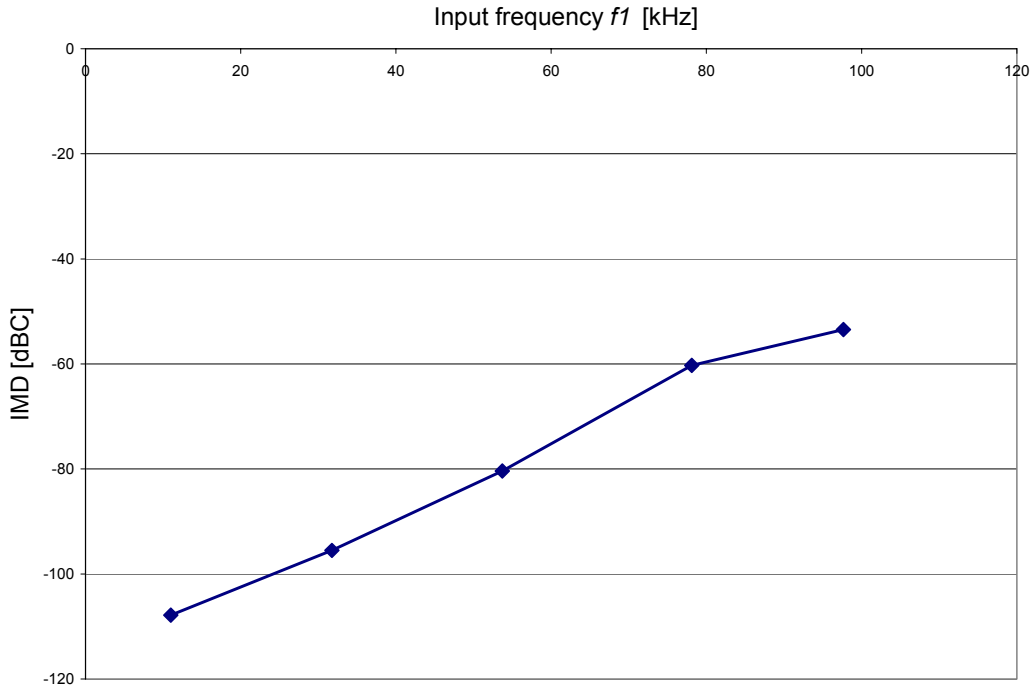


Fig 5.9 IMD vs. input frequency.

6 Conclusions

One of the key motivations for this study is the increasing demand for circuit design techniques for low-voltage applications. Conventional MOSFET-C filter designs suffer from low accuracy, and require on-chip automatic tuning in most applications. The dominant approach in existing tuning techniques is to tune the gate voltages of the MOSFET transistors, which is not suitable for true low-voltage application and causes poor linear performance. SC filters are accurate but may include floating switches that will cause problems in low-voltage applications. This thesis describes a filter design technique that has the simplicity of a MOSFET-C filter and the accuracy of a SC filter. The filter has high linearity and is highly suitable for low-voltage applications. All these advantages were illustrated by the transistor-level realization of a high-Q biquad filter.

The filter input branch proposed is a modification of an existing R-MOSFET input branch. Unlike what is done in R-MOSFET-C circuits, the MOSFET transistor functions only as a switch in this design. Therefore the input branch was named switched-R-MOSFET branch. It can be applied in any kind of design for a CT filter with a self-tuning feature.

The accuracy of the filter is achieved by a novel automatic tuning technique that changes the duty cycle for the MOSFET switch in the input branch (Chapter 3). Simulation shows that the corner frequency of the filter can be accurately tuned, and the tuning can be rapidly achieved (Chapter 5). There is no

change in the magnitude of the gate voltages, so all terminal-to-terminal voltages are always lower than V_{DD}. Therefore the proposed technique is highly suitable for low-voltage applications.

The designed filter has high linearity. The THD can as low as -100 dB, much superior to that achievable in conventional MOSFET-C filters (-40 to -60 dB). When the magnitude of the input signal increases, the harmonic distortion also increases. However, THD of -80dB can still be achieved for an input signal ($V_{p\text{-}p}$) as large as 0.5 V. This is significant considering that the supply voltage is only 1-V and the transistor threshold voltages V_{th} is around 0.5 V in the process used for simulation (Chapter 5). Two factors contribute to the high linear performance: firstm the MOSFET transistor in the input functions only as a switch. Its on-resistance R_{on} is very small compared to the linear input resistance R. As a result, the voltage across the nonlinear transistor is small. The non-linear effect from the transistor can thus be minimized; second, the MOSFET transistor is included in the feedback loop. Its non-linear effect is further suppressed (Chapter 2).

In summary, a high-Q biquad filter was successfully designed and simulated at transistor-level. The filter has an accurately tunable corner frequency and has high linearity. The tuning is realized by varying the duty cycle for the input MOSFET switch, involving no changes in the gate voltage. There is no floating switch in the circuit. Therefore the design is highly suitable for low-voltage application.

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