A 10 Bit Algorithmic A/D Converter for a Biosensor

by
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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

CHAPTER 1
INTRODUCTION

This thesis discusses a novel design technique for an algorithmic A/D converter that is capable of giving 1.5 bits/phase. The ADC is a part of Catalyst Foundation project, which involves the design of a cell-based sensor. The ADC performance is discussed including non-idealities and it is compared with a conventional architecture. Circuit design is done in 0.18μm CMOS technology.

1.1 Thesis Organization

Chapter 2 gives an overview of biosensors and discusses the proposed cell-based sensor system.

Chapter 3 gives an introduction to analog-to-digital converters and discusses various low power ADC architectures. Serial A/D converters such as incremental and successive approximation A/D converters are discussed.

Chapter 4 introduces algorithmic A/D converters, its advantages and disadvantages and applications. It gives an overview of existing algorithmic A/D converters.

Chapter 5 introduces the new algorithmic converter and also an earlier approach by Nagaraj et al., which is capable of the same performance.

Chapter 6 discusses the non-ideal effects in the algorithmic converter and ways to correct for them. Some of the non-ideal effects discussed are amplifier and comparator offset, capacitor mismatch, charge injection, amplifier finite gain, parasitic capacitances and thermal noise. The proposed

approach is compared with an existing approach with respect to the non-idealities in the system.

Chapter 7 discusses circuit design for the converter in 0.18μm CMOS technology. The amplifier and the comparator specifications are derived from the system level simulation of the converter. The schematics and the simulation results are given.

Chapter 8 provides the conclusions for the thesis.

CHAPTER 2

AN OVERVIEW OF BIOSENSORS AND THE PROPOSED CELL BASED SENSOR ARCHITECTURE

2.1 Biosensors

The term biosensor generally includes analytical devices that use immobilized biological materials (tissues, microorganisms or sub cellular components) and produce electronic signals in proportion to an analyte or a combination of analytes. Biological early warning systems (BEWS) detect toxicity by continuously monitoring the responses of organisms. The state of the art biosensors use live organisms such as bacteria, fish and nerve cells to detect the presence of chemicals in an environment. These biosensors are effective for specific toxins and are good in identifying the toxins. Most of the current sensors are bulky and require extensive use of computers and other sophisticated equipment and hence are expensive. Also these sensors are based on subjective detection requiring human observers. Detection speed is slow and typical observation cycles span several hours.

If the interest lies only in characterizing an environment in terms of its ability to support life, the present sensors are not very useful. Hence there is a need for a biosensor, which is cheap, handheld, consumes low power and is fast in determining the hospitability or the hostility of an environment.

2.2 Optical Detection

The present research involves developing a cell based sensor. The chromatophores of the Siamese fighting fish, *Beta Splendens*, is used as the cyto-sensor element. The above mentioned cells are very sensitive to toxicity and hence can give a fast response. These cells change in appearance when exposed to unfavorable environment. When exposed to hostile environment the cells move closer towards each other and hence it appears as though they have shrunk in size. This is known as aggregation. Aggregation can be observed visually and hence can be detected optically. Aggregation behavior is depicted in Figures 2.1 and 2.2.

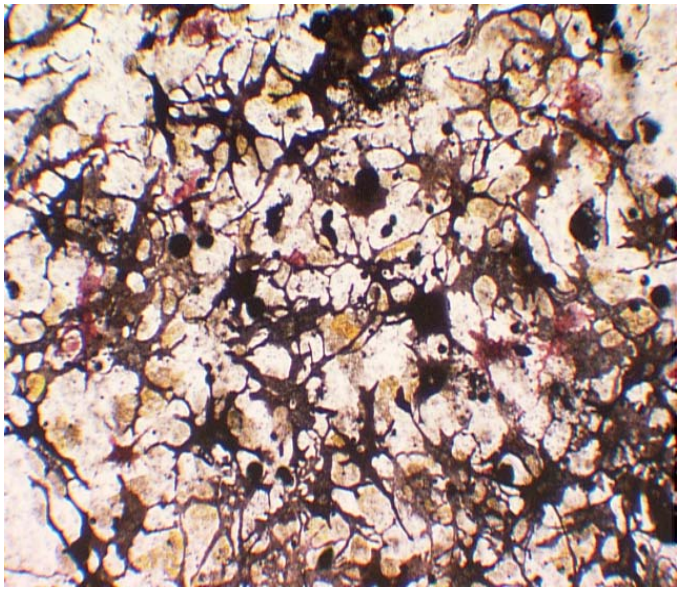


Figure 2.1 Chromatophores in hospitable environment

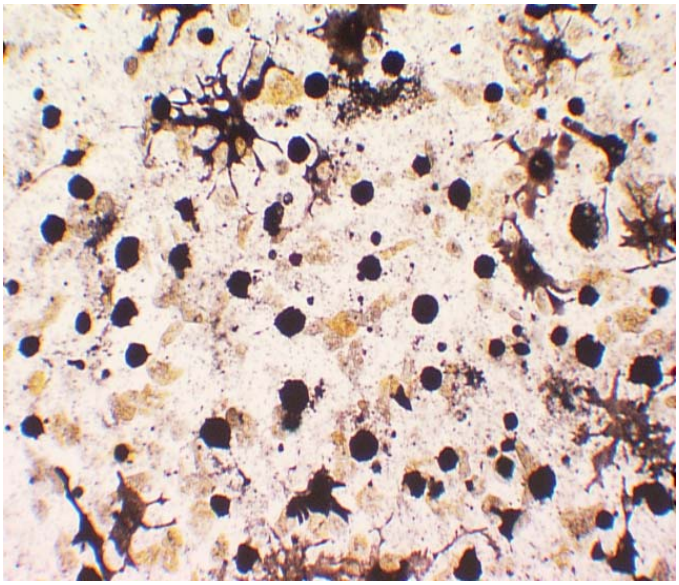


Figure 2.2 Chromatophores in hostile environment

Optical detection involves photodiodes on which the cell culture is placed. Light is passed through the culture and is converted to current by the photodiode. The experimental setup is shown in Fig 2.3. When a toxin is added to the culture, the cells aggregate and hence the light falling on the photodiode increases. Experiments were done using a commercially available photodiode and the current plots are shown in Figures 2.4 and 2.5. The experiments were done for 2 different kind of toxins and for different concentration.

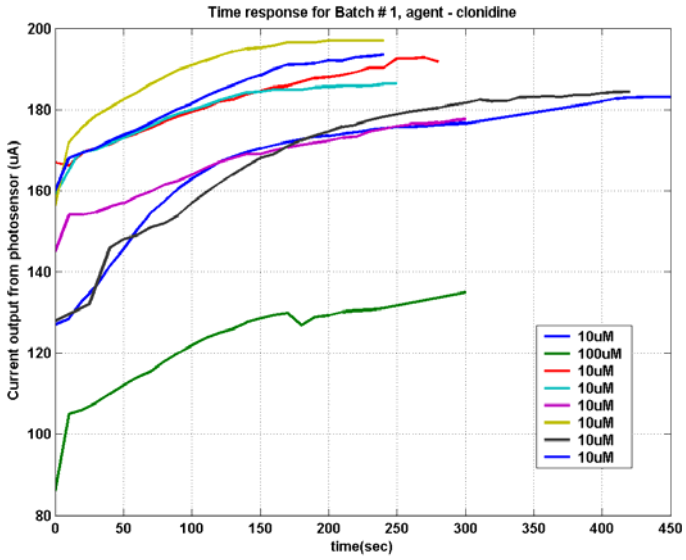


Figure 2.3 Current output for toxin Clonidine

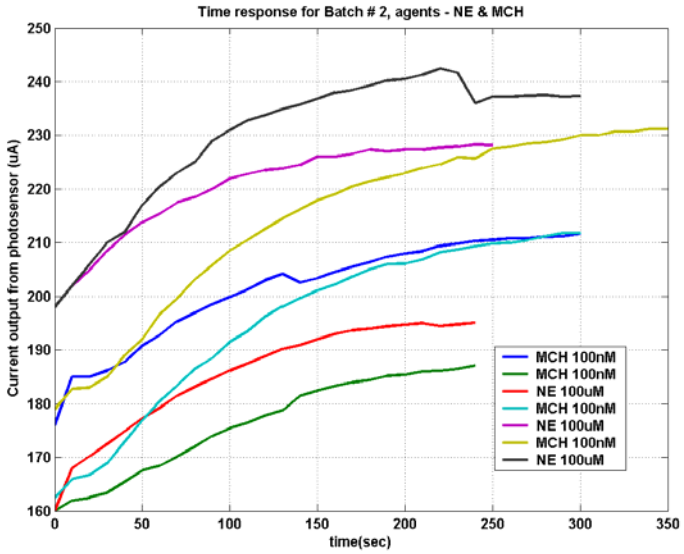


Figure 2.4 Current response for toxin NE and MCH

Observing the percentage change in the photocurrent performs detection, a threshold must be set by experimentation. The response of the cells depends on the culture technique, temperature, media, and concentration of the toxin. Two cultures prepared at the same time and

tested with the same toxin of the same concentration might not give the same result. Hence extensive experimentation with different cultures, toxins and concentration is required to find a threshold. But since different toxins affect cells in a different way, a biosensor assay containing many sensors can be built. This assay should be capable of covering many types of toxins.

2.3 Overview of sensor architecture

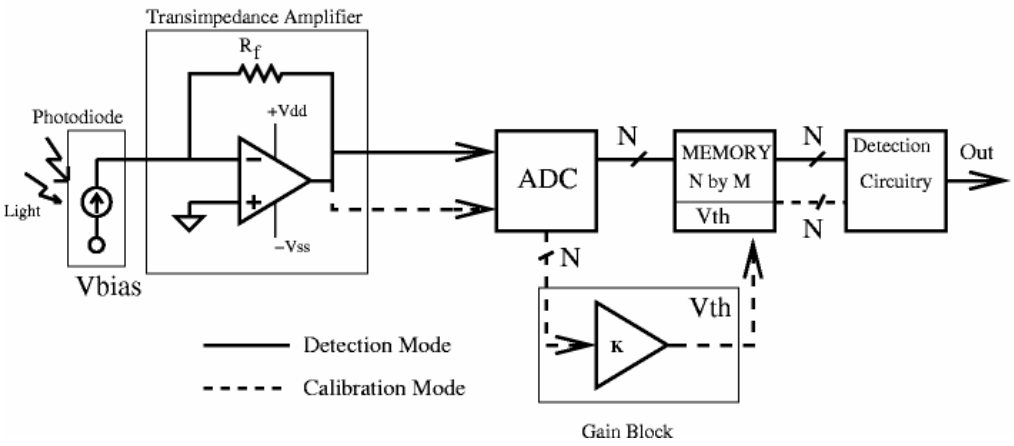


Figure 2.5 Sensor block diagram

The sensor architecture is shown in fig 2.6. The photocurrent from the photodiode is converted to a voltage by a trans-impedance amplifier. An A/D converter digitizes the voltage output from the trans-impedance amplifier, which is then stored in a SRAM. The increase in current can be continuously tracked by storing the outputs at intervals of time. This helps in identifying the effect of a toxin on the cell culture.

2.3.1 Calibration Mode

The threshold voltage is decided during the calibration mode. The cell culture is placed on the photodiode without a toxin and the digitized

output is scaled by the required percentage to set the threshold. The resulting threshold is stored in the memory for future comparisons.

2.3.2 Detection Mode

Cell culture with the toxin is the cytosensor element in this mode. Readings are taken from time to time and compared with the stored threshold. A single bit output can be given when the voltage exceeds the threshold. The sequence of readings is also stored in the memory for determining the action of the toxin which help in characterizing a toxin.

2.3.3 Photodiode Characteristics

Silicon photodiodes are devices responsive to high-energy particles and photons. Photodiodes operate by absorption of photons or charged particles and generate a flow of current proportional to the incident power in an external circuit. The photodiode used in experimentation is a planar diffused silicon photo diode. These are simply P-N junction diodes formed by diffusing a P-type impurity into a N-type silicon wafer or vice versa. A silicon photodiode can be represented as a current source in parallel with an ideal diode. The current source represents the current generated due to the incident radiation and the diode represents the P-N junction. In addition, a junction capacitance (depletion region capacitance), (C_j) and a shunt resistance ($R_{Sh,}$ usually 10s to 1000s of megohms) are in parallel with the other components. Resistance $R_{Se,}$ usually 10 to 1000 ohm, is connected in series with all components in the model. Dark current reduces the effective photocurrent. The model is shown in fig 2.7.

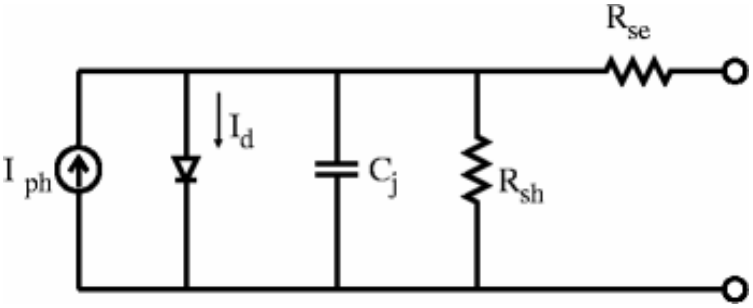


Figure 2.7 Equivalent circuit for the silicon photodiode

The transimpedance amplifier converts the photocurrent from the photodiode to a voltage which is digitized by the ADC. The ADC is discussed in detail in the subsequent chapters.

2.3.4 Converter specifications

From the above system details, the following converter specifications can be derived:

1. Approximately 5 minutes are needed for the changes to settle. Hence the speed required from the converter is low.
2. Measurements can be taken once every 5 or 10 seconds.
3. Since the main goal is a portable sensor, the converter must be low power. Usual sensor converters are in the 10s of micro watt range and the same is specified.
4. The change in current is in 100s of μA and can be converted to a voltage in 100s of mV. Hence the accuracy requirement of the converter is low (8 ~ 10 bits of resolution).
5. LEDs can be used as the light source in the portable sensor. These are the main power consuming devices in the system. Since measurements are to be taken once every 5 or 10 seconds, the system can be switched off in between to reduce LED consumption.
6. The ADC should be capable of conversion using least number of clock cycles to help in the above operation.

CHAPTER 3
ANALOG-TO-DIGITAL CONVERTER ARCHITECTURES

This chapter discusses existing analog to digital converters suitable for low power applications, their advantages and disadvantages.

3.1 Introduction to Analog-to-Digital Converters

An analog-to-digital converter is a device which converts real world signals into digital codes. An ADC is a key part of an interface between analog and digital components. The ADC by nature is sampled data circuit[10].

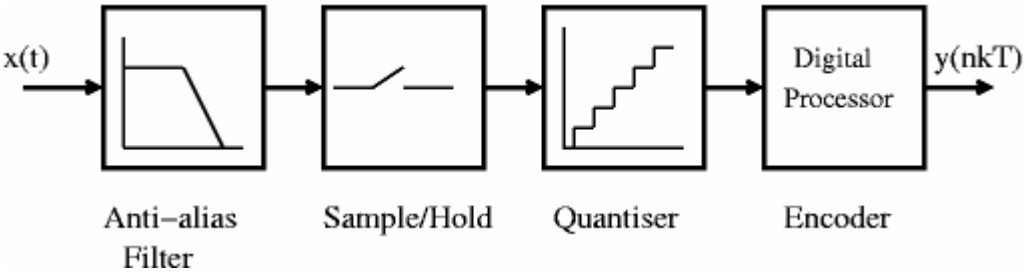


Figure 3.1 Block diagram for an ADC [10]

Figure 3.1 shows a block diagram of a general ADC. Since the ADC is a sampled-data circuit, a prefilter called an anti-aliasing filter is required to avoid aliasing. A sample-and-hold circuit that maintains the ADC input constant during the time the signal is converted to its equivalent digital code follows the anti-alias filter. The conversion is accomplished by a quantization step. A quantizer segments the reference range into subranges. Typically there are 2^N subranges where N is the required resolution in bits. The quantization step finds the subrange that corresponds to the sampled analog input. An encoder encodes the subrange into a digital output code.

3.2 ADC Characteristics

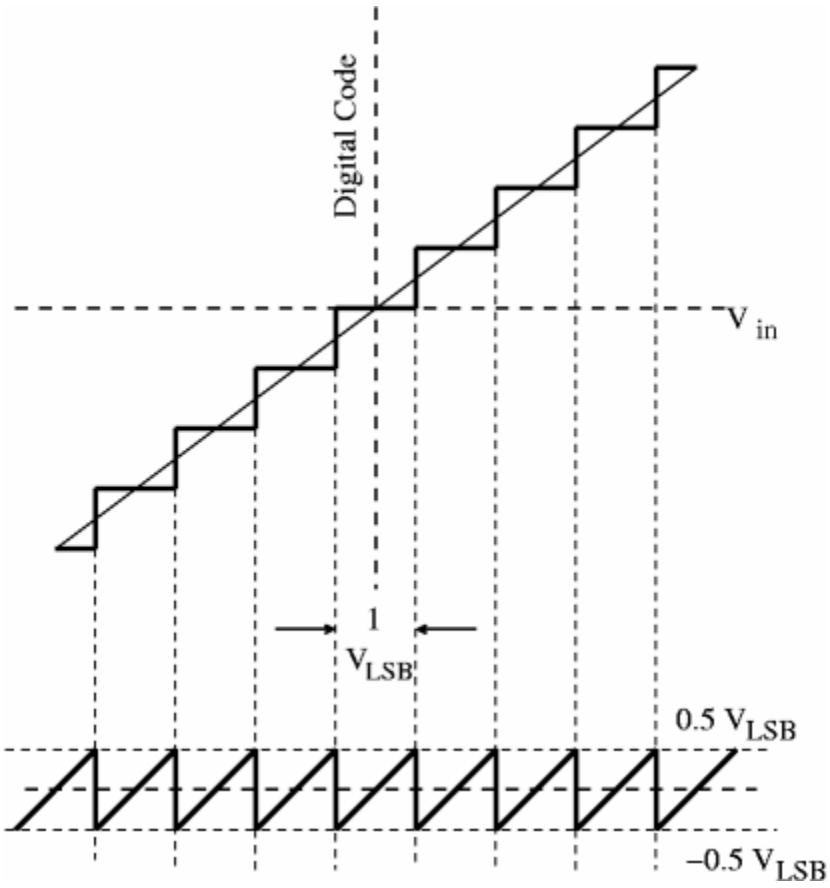


Figure 3.2 Transfer curve and quantization noise of a 9 level ADC

Figure 3.2 shows the characteristics of a 9 level A/D converter. It is evident from the above figure that a range of input values gives the same code. Thus there is a loss of information that is called quantization error or quantization noise. The quantization noise for an ideal A/D converter ranges from $-\frac{V_{LSB}}{2}$ to $\frac{V_{LSB}}{2}$ where $V_{LSB} = \frac{V_{ref}}{2^N}$. The output of an A/D converter is a sum of the input signal and the quantization noise. For a busy signal at the

input of the converter the quantization noise power is given by $\frac{V_{LSB}^2}{12}$. An A/D converter is overloaded when the quantization noise exceeds the range mentioned above. The SNR of an ideal converter, assuming a full scale sine wave input, is given by $(6.02N + 1.76)$ dB, where N is the resolution of the converter.

3.2.1 Resolution

The resolution of a converter is defined as the number of levels the reference can be divided. An N bit A/D converter divides the reference range into 2^N levels. Resolution does not necessarily represent the accuracy of a converter.

3.2.2 Nonlinearity

Nonlinearity in an A/D converter manifests in the form of non-uniform steps and missing codes or levels. These are measured as integral nonlinearity (INL) and differential nonlinearity (DNL), which are expressed in LSBs. INL refers to the maximum deviation of the actual curve from the ideal curve. For a converter not to have missing codes the maximum INL should be less than 0.5 LSB.

In an ideal A/D converter, the transition voltages are 1 LSB apart. DNL is defined as the deviation of the separation of the transition voltages from 1 LSB. Non-monotonicity in an ADC occurs when the jump is negative and this can be determined only through DNL. A converter may have a maximum DNL of 1 LSB for it to be monotonic. Figure 3.3 shows the actual and the ideal curve of a 9-level A/D converter.

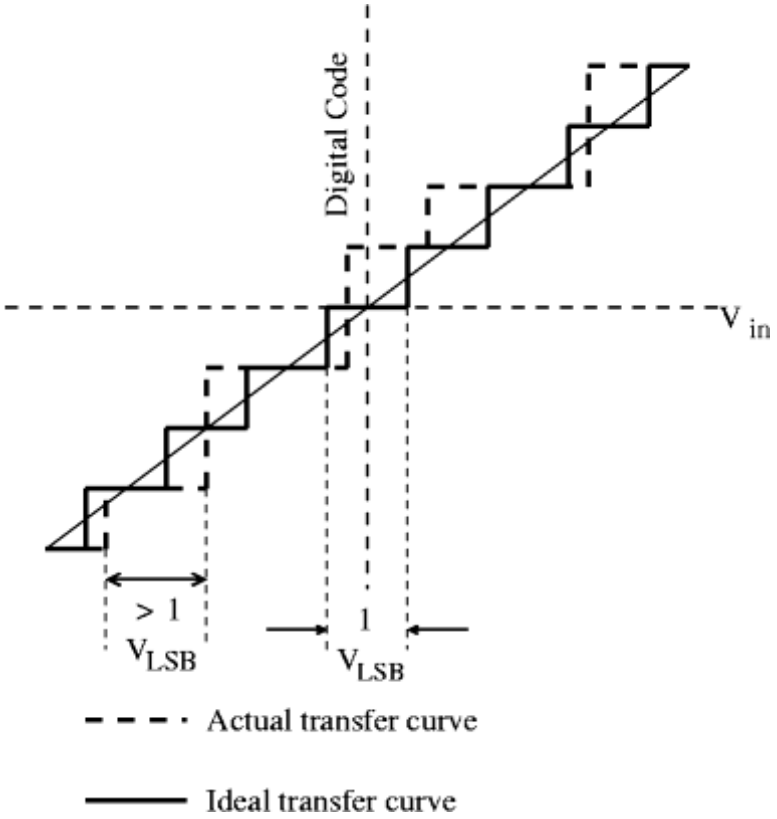


Figure 3.3 Actual and ideal transfer curves

3.2.3 Accuracy

Accuracy of a converter refers to how precisely the transfer characteristics is controlled. Ideally a converter is infinitely accurate. Thus accuracy does not mean resolution.

3.2.3 Signal to noise ratio (SNR)

SNR refers to the ratio of the signal power to the noise power at the output of the ADC.

$$SNR(dB) = signal\ power(dB) - noise\ power(dB)$$

For an A/D converter the above includes the quantization noise and other noise. The effect of distortion can also be included into the calculation and is referred to as the signal to noise + distortion ratio or SNDR.

3.2.4 Dynamic Range

Dynamic range is defined as the input range for which a system gives useful output. The maximum input level in a system is limited by distortion whereas the minimum signal level that can be applied is limited by noise. The minimum detectable signal is the input for which the SNR is 0 dB.

Spur-free dynamic range or SFDR is another way of expressing the dynamic range. It gives the range of input that can be applied before distortion becomes dominant.

3.3 ADC Architectures

The following table [9] classifies the different ADC architectures in terms of conversion rate and resolution.

Conversion rate	ADC Architecture	Resolution
Slow	Integrating, incremental	Very high resolution > 16bits
Medium	Successive approximation 1 bit pipeline and algorithmic	Moderate resolution > 10bits
Fast	Flash Multi-bit pipeline Folding and interpolating	Low resolution > 6bits

Table 3.1 Classification of ADC architectures

3.3.1 Incremental A/D converter

For converters used in measurement and instrumentation applications, the input signals are usually at a very low frequency, but the required absolute accuracy is very high. Incremental A/D converters are used in such applications.

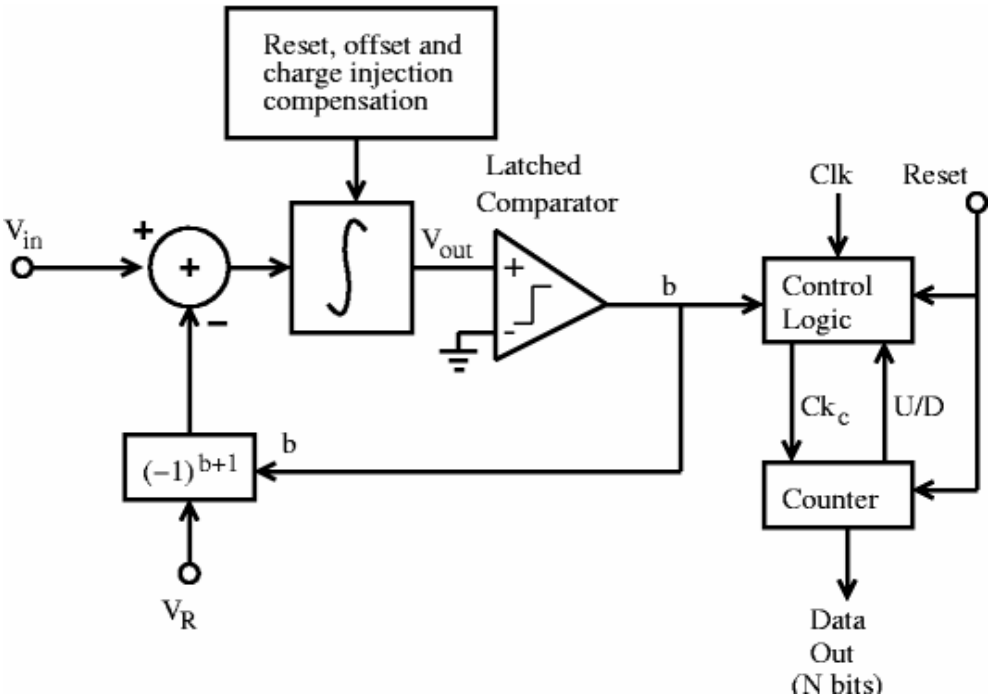


Figure 3.4 Incremental A/D converter block diagram[4]

Figure 3.4 shows the block diagram of a 1st order incremental A/D converter [4]. The converter works in the following manner: Before each conversion, the integrator and the counter are reset and a compensating voltage is established at the input of the integrator. A fixed number of integration steps are performed to find the integer $N = 2^n \frac{V_{in}}{V_R}$, where n+1 is the number of integration steps, n is the resolution needed and V_R is the reference voltage. Thus N is the digital value of V_{in}. The above procedure is repeated for the next input.

The 1st order incremental converter uses a delta-sigma loop for the conversion but is reset before each input. Hence the input needs to be a constant throughout the conversion time. A conventional delta-sigma modulator gives output once every R clock periods, where R is the oversampling ratio. But an incremental A/D converter gives once in 2^{n+1} cycles. The digital circuitry consists only of a counter rather than a decimation filter in the case of a ΔΣ modulator. The output of a ΔΣ modulator oscillates for DC inputs and hence needs dithering to avoid tones but an incremental converter is designed for DC inputs and does not need dithering. But it is much slower than a conventional ΔΣ modulator.

The incremental A/D converter is capable of resolution > 16 bits which is well suited for precision instrumentation, telemetry and measurement applications. The effect of offset can be corrected digitally by adding the digital outputs due to V_{in} and $-V_{in}$. Analog compensation can also be used to reduce the effect of offset. Capacitor nonlinearities such as sensitivity to voltage variations should be reduced since they can affect very high-resolution converters.

The incremental converter is a highly accurate but very slow converter. The converter uses a ΔΣ loop and hence does not require accurate components. It requires only a simple circuitry, no need for high performance analog components and requires a single voltage reference for bipolar operation. The area and power requirements are low. Typical conversion times range from 1 sec to 5 secs for 16 bit applications.

3.3.1.1 Higher Order Incremental Converters

The first order incremental converter needs 2n clock cycles for conversion and hence it is very slow. Higher order incremental A/D converters [5] can reduce the number of clock periods necessary but the trade-off lies in analog and digital circuit complexity. A block diagram of a

higher order incremental converter is shown in figure 3.5. The converter consists of a discrete time ΔΣ modulator, a digital filter and a controlling circuit. As in the case of a 1st order converter, all memory elements and counters must be reset before each input is converted.

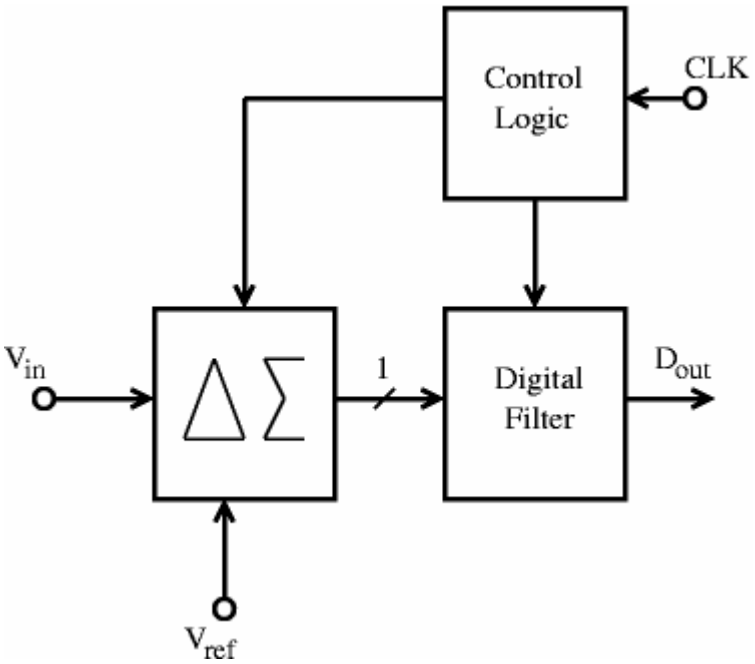
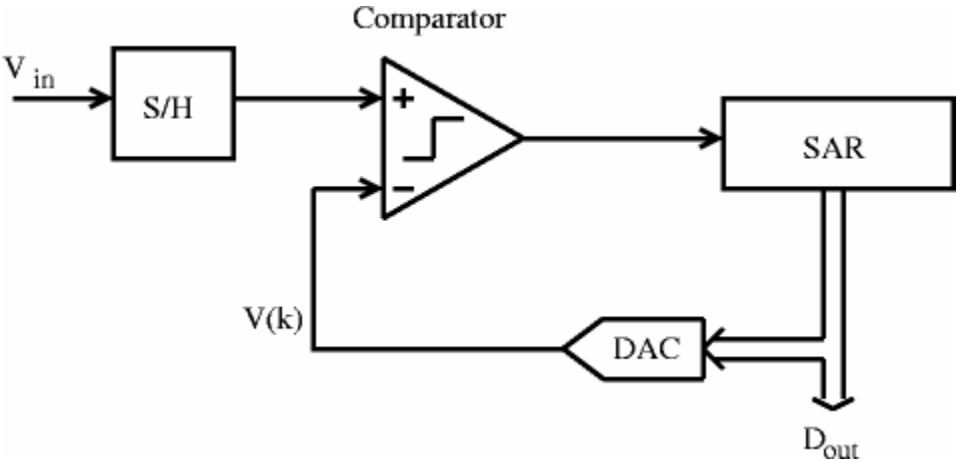


Figure 3.5 Block diagram of higher order incremental A/D converter

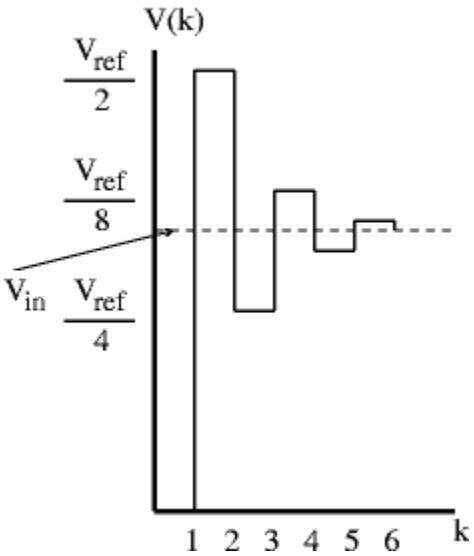
The ΔΣ modulator in the converter can be designed using conventional delta-sigma design techniques. The number of clock cycles needed for conversion goes down drastically as the order of the modulator increases. A digital filter with higher order as the modulator is needed. Decimation filters used in conventional ΔΣ modulators can be used as digital filters. Incremental converters need a dedicated sample-and-hold stage, since the input needs to be a constant till the conversion is complete.

3.3.2 Successive-Approximation A/D converters

Another serial converter, which can be used for low power applications, is the successive-approximation A/D converter. Their circuit complexity is moderate. General successive approximation converter architecture is shown in figure 3.6.



(a)

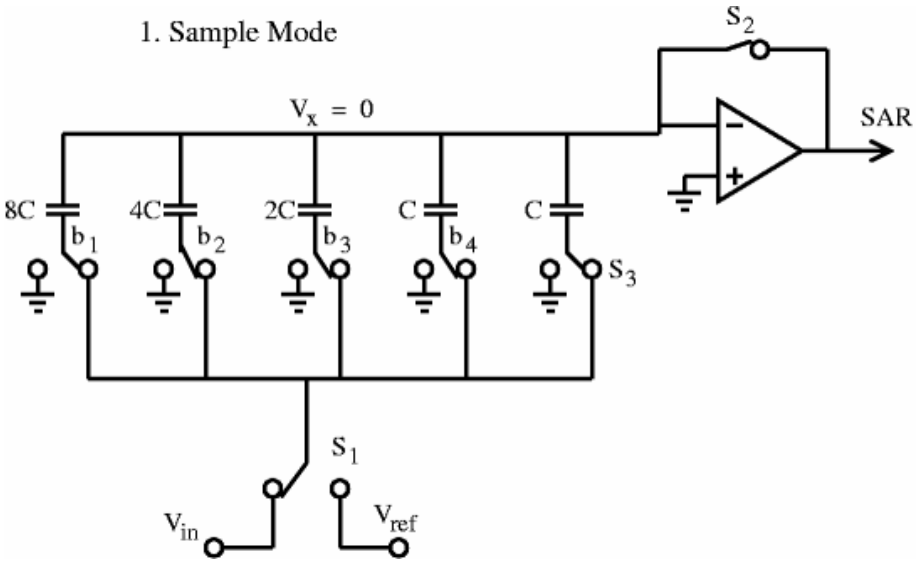


(b)

Figure 3.6 Successive approximation ADC

Successive approximation conversion is very similar to a binary search algorithm. With respect to unipolar operation, the comparison voltage V_{DAC} is set to $\frac{V_{ref}}{2}$. V_{in} is compared with V_{DAC}. If $V_{in} > V_{DAC}$, then the new V_{DAC} is voltage is $\left(\frac{V_{ref}}{2} - \frac{V_{ref}}{4}\right)$. If $V_{in} < V_{DAC}$, then the new V_{DAC} voltage is $\left(\frac{V_{ref}}{2} + \frac{V_{ref}}{4}\right)$. This operation is repeated till the difference between V_{in} and V_{DAC} is < 1 V_{LSB}. The operation is depicted in figure 3.6(b). The DAC output is continuously compared with the input and hence this converter needs a dedicated sample and hold circuit to keep the input a constant till the conversion is complete. For an N bit converter, the conversion takes place in N clock cycles. MSB is found first. The internal DAC is in the feedback path of the converter and hence the converter's accuracy is determined by the DAC accuracy. Thus DAC design is very critical in a SAR converter. Calibration must be done in order to achieve high resolution.

Successive approximation converters can also be implemented as a charge redistribution converter[11] with binary weighted capacitors. Figure 3.7 shows a 4-bit unipolar charge redistribution ADC.


1. Sample Mode
S2
Vx = 0
SAR
8C
4C
2C
C
C
b1
b2
b3
b4
S3
S1
Vin
Vref

(a)

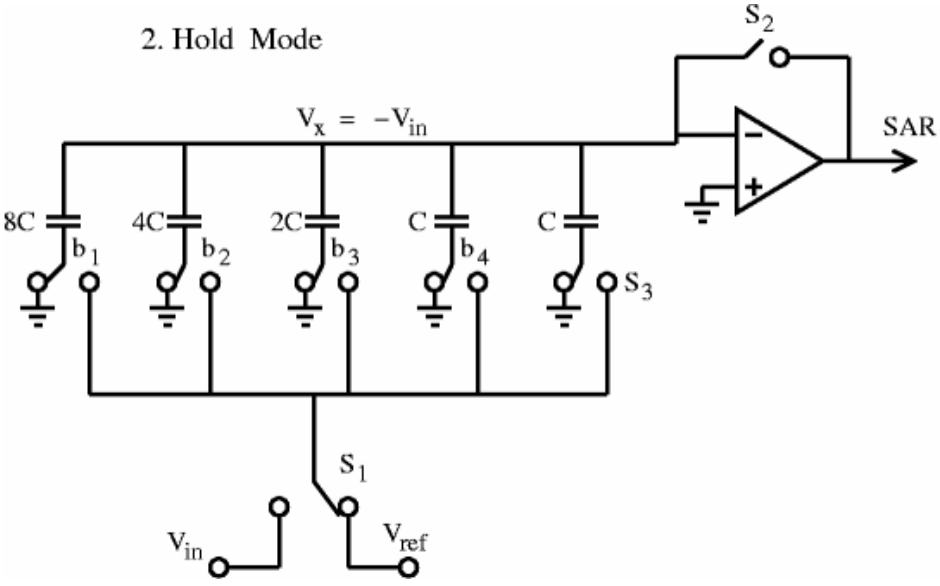

2. Hold Mode
S2
Vx = −Vin
SAR
8C
4C
2C
C
C
b1
b2
b3
b4
S3
S1
Vin
Vref

figure 3.7(b)

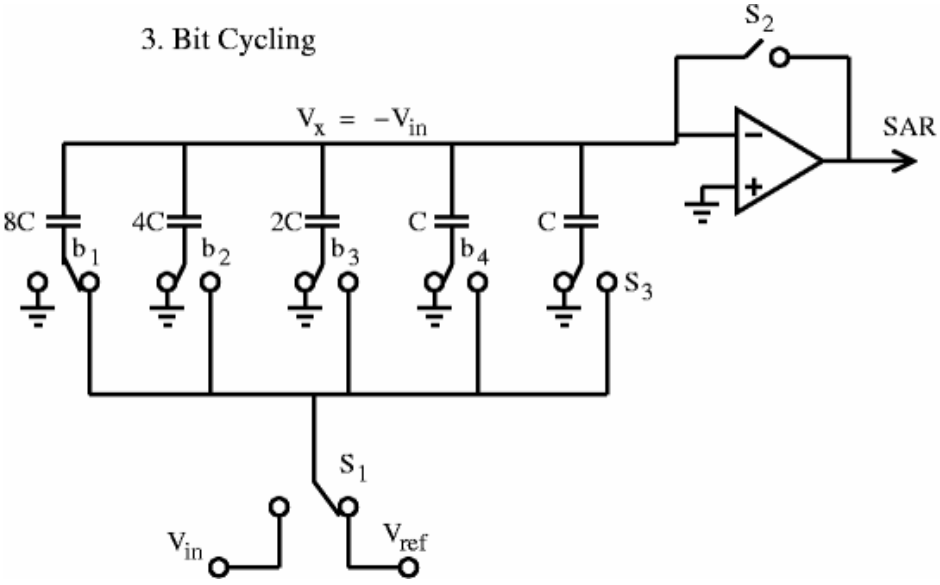


figure 3.7(c)

Figure 3.7 A 4 bit unipolar charge redistribution ADC

- Sample Mode: Comparator is reset and all capacitors are charged to V_{in}
- Hold Mode: Comparator is taken out of reset and all capacitors are switched to ground and this causes the comparator input to be $-V_{in}$ and comparison takes place.
- Bit Cycling: The largest capacitor (8C) is switched to V_{ref}. This makes the input of the comparator to become $-V_{in} + \frac{V_{ref}}{2}$. The MSB capacitor is left connected if $V_{in} > V_{ref}$. The process is repeated for the next largest capacitor in the array till all the capacitors are used.

In the original successive approximation algorithm, V_{DAC} is updated after comparing V_{in} with V_{DAC}, but in charge redistribution converter it is V_{in} that is updated after each comparison. This does not require a DAC which can limit the linearity. Thus the linearity depends on capacitor matching and 10-bit linearity is obtainable with careful layout. For higher

resolution, capacitor mismatch correction must be performed which is usually done in the digital domain. Circuit complexity is low. These converters do well for moderate speeds and moderate resolution. Since a binary array of capacitors is required, area is large. Power can increase by a large amount if higher speeds are required.

3.3.3 Algorithmic A/D converter

Also known as cyclic converters, algorithmic ADC is a serial A/D converter and needs N cycles to complete a conversion. Residue cycling is involved. These converters will be discussed in detail in chapters 4 and 5.

CHAPTER 4
ALGORITHMIC A/D CONVERTERS

This chapter discusses cyclic converters and introduces a new architecture for algorithmic A/D converters

4.1 Introduction

Cyclic converters operate in a similar way as successive-approximation converters. In successive-approximation converter, the reference is halved each cycle, whereas in algorithmic converters the error voltage is doubled. The operation of a cyclic converter is given as a flowchart[9] in figure 4.1.

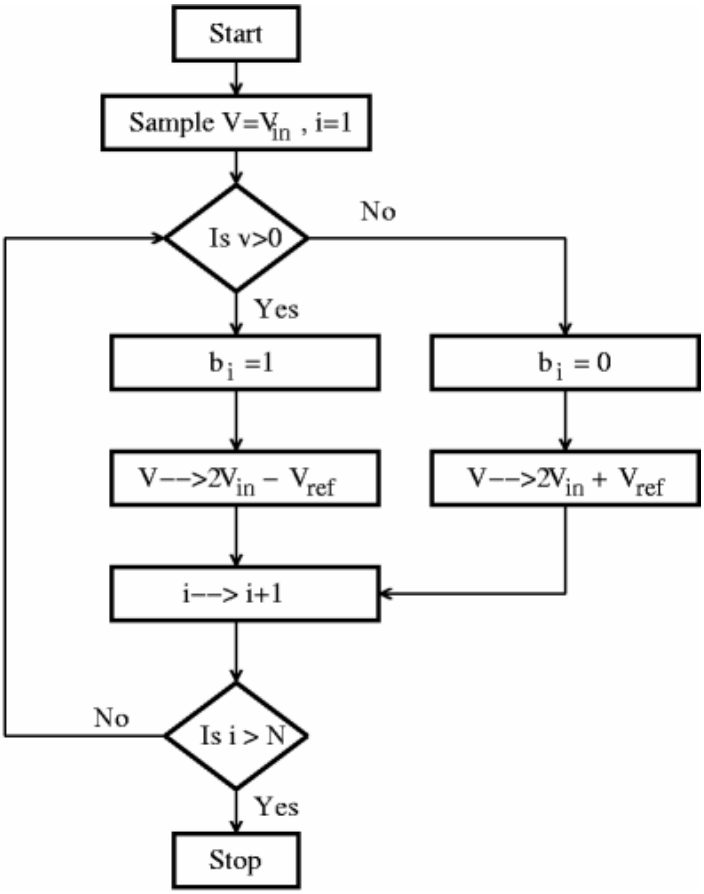


Figure 4.1 Cyclic converter flowchart

An algorithmic converter consists of a sample and hold, a multiply-by-2 amplifier, a comparator and a reference subtraction circuit. Figure 4.2 shows a block diagram of the algorithmic converter[12]. The input is sampled only once every conversion cycle. The same sampling circuit samples the first residue again and this process continues. Comparing each residue with a reference makes a bit decision. Thus a cyclic converter requires at least N cycles for N bit conversion. Till the conversion is complete the input circuit is disabled. Hence the converter has to sample the input during one clock period. This is unlike SAR or an incremental A/D where the input needs to be constant throughout the conversion cycle.

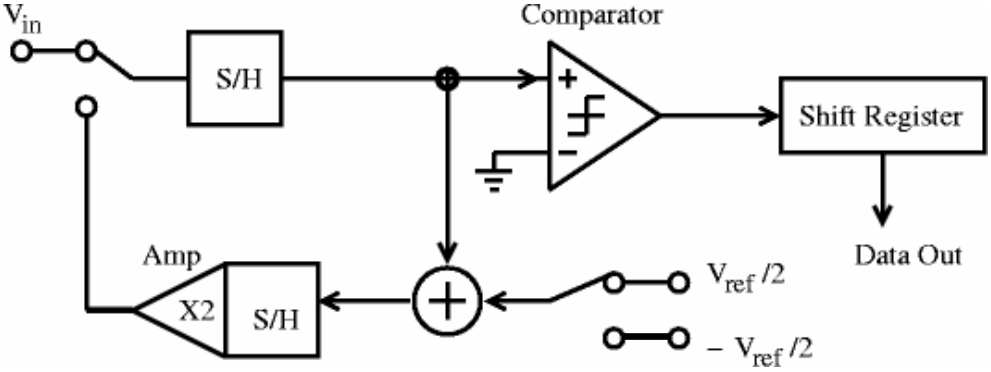


Figure 4.2 Block diagram of algorithmic converter[12]

The residue in each cycle is given by $2V_{in} \pm V_{ref}$. The switched capacitor implementation of a multiply-by-2 circuit is shown in figures 4.3. During the sampling phase, the input is sampled on to the capacitors C_f and C_s. During the doubling phase, C_s discharges into C_f and, $V_{out} = \left(1 + \frac{C_s}{C_f}\right) V_{in}$.

For Cs = Cf, $V_{out} = 2V_{in}$.

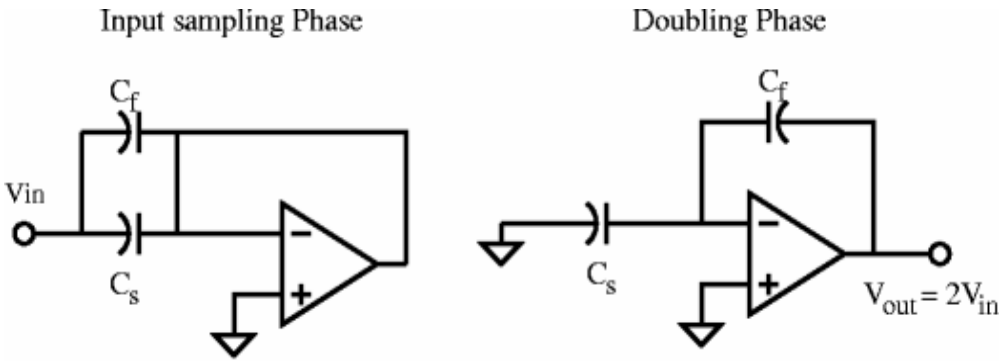


Figure 4.3 Multiply-by-2 circuit

Building an accurate multiply-by-2 circuit is a difficult task in the design of algorithmic converters. Capacitor mismatch leads to gain errors and leads to non-linearities in the converters.

Ratio-independent switching schemes[13] (as shown in figure 4.4) remove mismatch dependence. During phase 1, capacitor C_s is charged to the input and capacitor C_f is discharged. During phase 2 C_s is discharged onto C_f and $V_{out} = V_{in}$. In the 3rd phase, C_s is charged to V_{in} and in the fourth phase C_f discharges onto C_s to give $V_{out} = 2V_{in}$. C_f does not define the final voltage at the output of the op-amp. C_f is just used as a storage device to store the charge of C_s and transfer it back to C_s and hence the above switching scheme is ratio independent. The length of the basic clock cycle is determined by 4 op-amp settling times. Hence the speed is limited by the op-amp. The converter needs 2N clock cycles for N-bit conversion. Accuracy-speed trade off is presented in the above switching scheme.

All the above algorithmic converters are slow in the sense that they need at least N clock cycles to perform N bit conversion. The following chapter introduces a new algorithmic converter that is capable of giving a bit per *phase*., rather than a bit per *cycle.*

CHAPTER 5

A New Cyclic Converter Architecture

Most of the algorithmic converters designed earlier need at least N clock cycles for N-bit conversion. This chapter introduces a new algorithmic converter architecture that is capable of providing 1 bit per *phase*.

5.1 1-Bit/Step Architecture

The operation of the new architecture consists of 3 phases: reset, phase 1 and phase 2.

Reset Phase: Capacitors C_1 and C_2 are charged to the input voltage V_{in}. C_3 is the load capacitor to the amplifier, which is reset to V_{os}. Also during this phase V_{in} is compared with a reference that gives the MSB of the digital code. The reset phase is shown in figure 5.1.

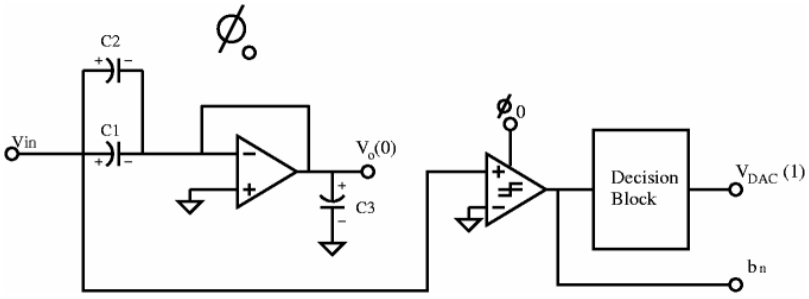


Figure 5.1 Reset Phase

Phase 1: Capacitor C_1 is connected as the feedback to the amplifier, and connecting capacitor C_2 to the DAC voltage does the reference subtraction. Hence C_2 discharges to the DAC voltage and the residual output of the amplifier is given by

$$V_o(k+1) = 2 \cdot V_o(k) - V_{DAC}(k+1)$$
$$V_{DAC}(k+1) = V_{ref} \text{ for } V_o(k) < V_{ref}$$
$$V_{DAC}(k+1) = -V_{ref} \text{ for } V_o(k) > V_{ref}$$

C_3 and C_1 are charged to the residual voltage $V_o(k)$ The residual voltage is compared with the reference to obtain the next bit in the conversion and this bit is used to decide the next DAC voltage, which should be subtracted from the residue. Phase 1 is shown in figure 5.2.

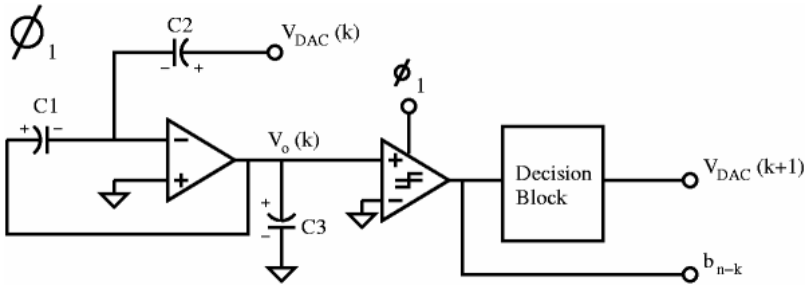


Figure 5.2 Phase 1

Phase 2: During this phase capacitors C_2 and C_3 are interchanged, C_3 is connected to the DAC voltage and the next residue is obtained. The next bit is obtained by comparing the residue to the reference. Phase 2 is shown in figure 5.3.

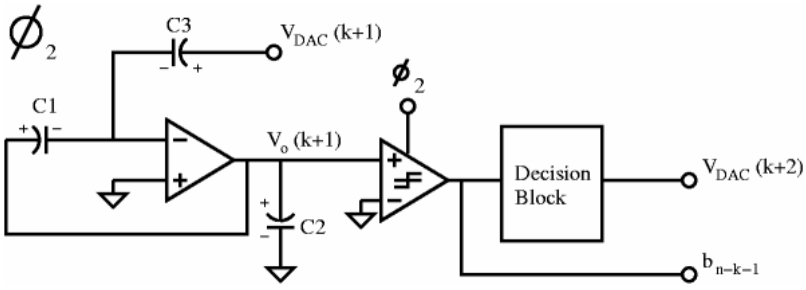


Figure 5.3 Phase 2

During the reset phase the input is sampled, and then phase1 and 2 take over to bring about the conversion. Since three capacitors are used, a bit can be obtained each phase and hence leads to 2 bits per clock period. Thus N/2 clock cycles are required for N bit conversion. The above converter is at least 2 times faster than the existing cyclic converters. Figure 5.4 gives the transfer characteristic of the 1 bit/ stage architecture.

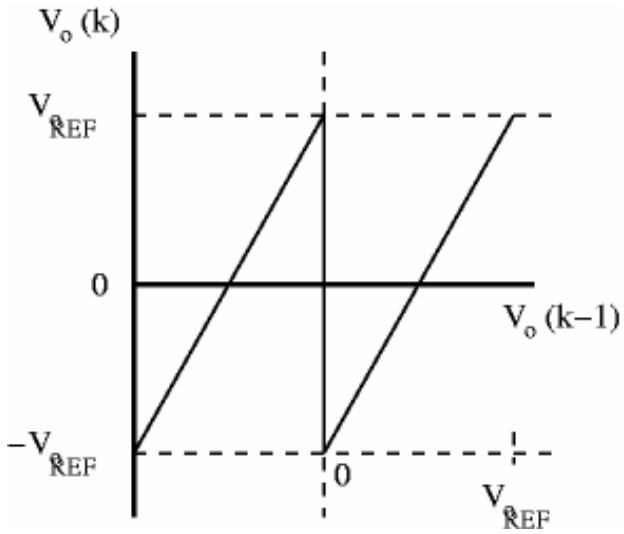


Figure 5.4 Transfer Characteristic of 1-Bit/Phase Architecture

The above description assumed that all the components in the system were ideal. Non-linearities in the system deviates the curve from the normal and limits the performance.

5.1.1 System Non-Idealities

These can be divided into 2 major categories: dc nonlinearities and dynamic nonlinearities. These lead to missing codes, harmonic distortion, and non-monotonicity, which limit the performance.

DC non-linearities include amplifier and comparator offsets, capacitor mismatch, amplifier finite gain and non-linearity and capacitor

non-linearity. Dynamic non-linearities include amplifier settling errors, comparator insensitivity and charge injection.

5.1.2 Problems of the 1-Bit/*Phase* System

The above non-linearities lead to decision errors at the segment boundaries. Amplifier and comparator offsets lead to bit error which propagates to the DAC voltage being subtracted from the previous residue. Figure 5.5 gives the transfer curve in the presence of comparator or amplifier offset

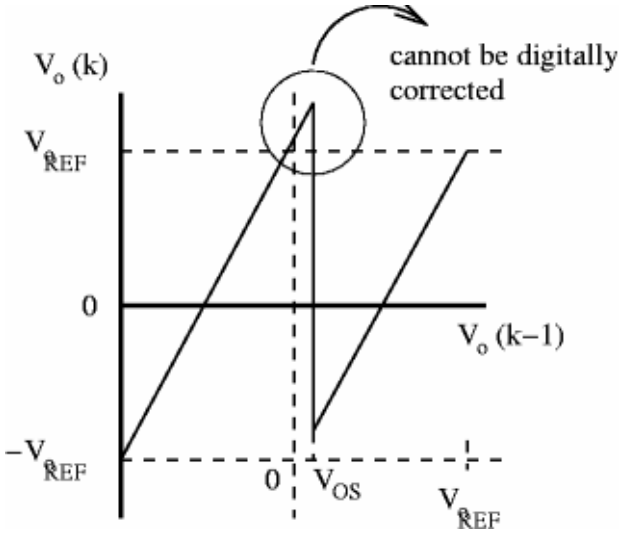


Figure 5.5 Transfer Curve with Comparator Offset

When a residue exceeds the ideal bounds, it does not have a unique digital code to define it and hence digital correction cannot be performed. Amplifier offset builds up exponentially as the conversion proceeds and hence cannot be tolerated. Missing decision levels occur due to amplifier and comparator offsets, incomplete settling and comparator insensitivity. Amplifier offset can be removed by offset cancellation techniques like CDS and chopper stabilization. Latches can remove comparator insensitivity. But

the biggest problem in a single bit per stage architecture is the comparator design due to the following:

1. Comparator offset voltage must be cancelled. This results in extra circuitry for comparators to cancel their offsets and this results in low speed comparators.
2. It needs to amplify very small signals.
3. Comparator operation can begin only after the op-amp settles completely. If not, it leads to decision errors and hence distortion.

5.2 (N>1) Bit/*Phase* Architecture

The difficulty in the comparator design in a 1 bit/step architecture leads to error correction techniques to correct for comparator and amplifier offsets.

An N-bit stage in the converter implies that ideally $-\frac{V_{ref}}{2^N} \le V_q \le \frac{V_{ref}}{2^N}$, where V_q is the quantization error. In a non-ideal converter, the quantization error exceeds this bound. In a cyclic converter it is the quantization error of the previous conversion that is converted in the next cycle. This quantization error is amplified by 2^N (amplifies the residue to the full input range of the converter), where N is the resolution of the stage. To keep the quantization error from exceeding its bounds an amplification of 2^{N-1} is used. The redundant bit in the stage is used for error correction.

5.2.1 Transfer Characteristic

The DAC voltage takes 3 values depending on the input. A 2-bit flash converter is used to resolve the residue in to 2 bits. The following table gives the DAC voltage and the residual voltage for different bit outputs.

$b_{1(k)}$	$b_{2(k)}$	$V_{DAC}(k+1)$	$V_o(k+1)$
0	0	$-V_{REF}$	$2V_o(k) + V_{REF}$
0	1	0	$2V_o(k)$
1	1	V_{REF}	$2V_o(k) - V_{REF}$

Table 5.1 Feedback and Residue with respect to output

The comparator threshold voltages are at $-\frac{V_{ref}}{4}$ and $\frac{V_{ref}}{4}$. The output of the comparators is a thermometric code that is converted to digital code before the overlap addition. Figure 5.6 shows the transfer characteristic of 1.5-bit/phase architecture.

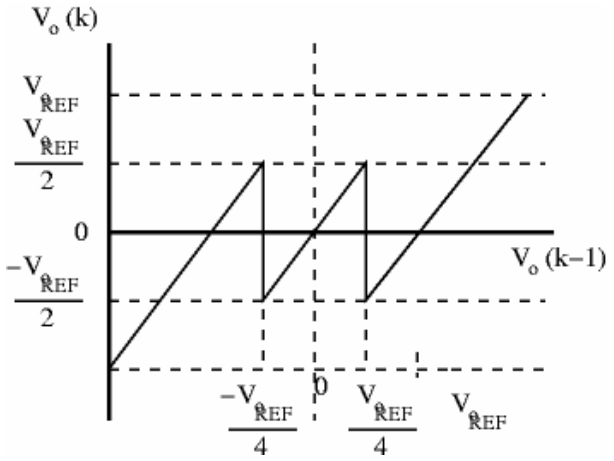


Figure 5.6 Transfer curve for a 1.5-Bit/Phase architecture

The full input range of the converter is ($-V_{ref}$, V_{ref}) but at the decision boundaries ($V_{in}=-V_{ref}/4$ and $V_{in}=V_{ref}/4$), the input range is ($-V_{ref}/2$, $V_{ref}/2$). The transfer characteristics with comparator or amplifier offsets is given in figure 5.7

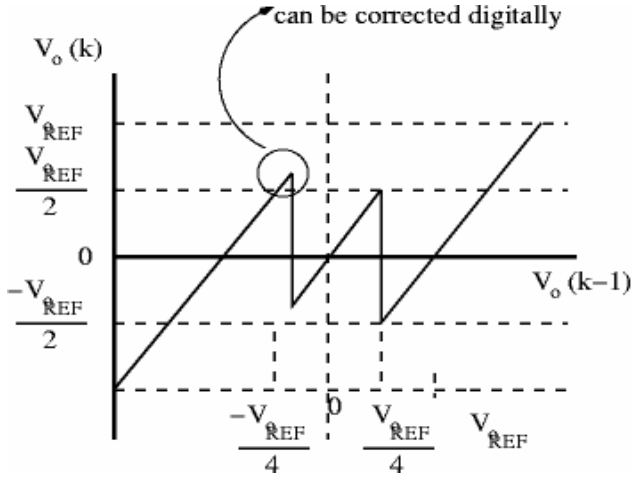


Figure 5.7 1.5-Bit transfer curve with comparator offset

Comparator and amplifier offsets shift the curve according to the sign of the offset. As shown in figure 5.7, the residue does not go below $-V_{ref}$ or above V_{ref} for small offsets and hence any error in the residue can be corrected using digital correction.

Let us assume a $V_{in} = -\frac{V_{ref}}{4}$. For this input the residue is given by $V_o = 2V_{in} + V_{ref} = \frac{V_{ref}}{2}$. For $V_{in} > -\frac{V_{ref}}{4}$, the residue is given by $2V_{in}$. If the comparator with the lower threshold has an offset $V_{os,comp}$, the residue is given by $V_o = 2V_{in} + V_{ref} + V_{os,comp}$. Only when $V_{os,comp} > \frac{V_{ref}}{4}$, the residue goes out of bounds. Hence comparator offsets of $\frac{V_{ref}}{4}$ can be tolerated by the 1.5 bit/phase architecture. Errors due to comparator offsets reduce the correction range and do not result in missing decision levels.

5.2.2 Redundancy correction

Only 3 levels of the 2 bit output from each cycle is used and this gives the scheme its 1.5-bit characteristic. The output obtained from the cycles is not the output format which is required. Redundancy error correction is used to correct the output digital code for comparator and amplifier offsets. The LSB of the 2-bit digital code of a residue is overlapped with the MSB of the 2-bit code of the next residue and added. The redundancy addition is shown in figure 5.8

$b_{1(0)}\ b_{2(0)}$

$b_{1(1)}\ b_{2(1)}$

$b_{1(3)}\ b_{2(3)}$

……..

$b_{1(k)}\ b_{2(k)}$

$d_k \quad d_{k-1} \quad d_{k-2} \ \ldots \ d_1 \quad d_0$

Figure 5.8 Redundancy Error correction scheme

The following are the advantages of redundancy and error correction:

1. Insensitivity to decision errors
2. Simple, high-speed comparators can be used. This is because large comparator offsets can be tolerated.
3. Comparators need not wait for amplifier settling.
4. All offsets in the system translate into a net offset and do not result in non-linearity.

5.3 1.5 Bit/Phase Architecture

The 1.5 bit/phase switching scheme is introduced in this section. An alternative approach is also provided for comparison. As in the 1 bit case the operation is divided into 3 phases. The following describes the operation during these phases.

Reset Phase: Capacitors C_1 and C_2 are charged to the input voltage V_{in}. C_3 is the load capacitor to the amplifier that is reset. Also during this phase, V_{in} is compared with a reference which gives the MSB of the digital code. The reset phase is shown in figure5.9.

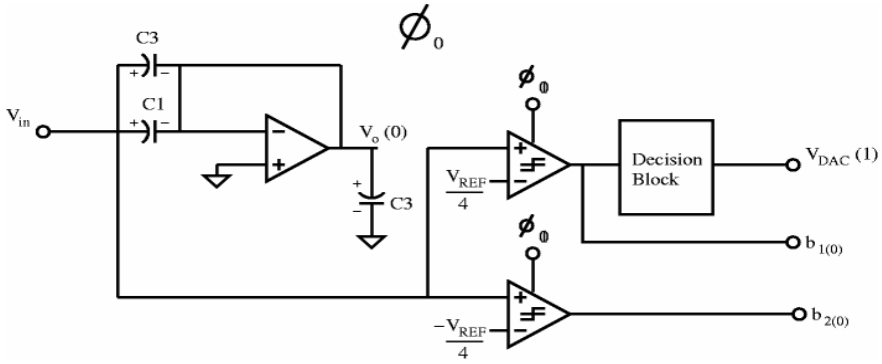


Figure 5.9 Reset phase

Phase 1: Capacitor C_1 is connected as the feedback to the amplifier and connecting one of capacitor C_2 to the DAC voltage does the reference subtraction. Hence C_2 discharges to the DAC voltage and the residual output of the amplifier is given by

$$V_o(k+1) = 2 \cdot V_o(k) - V_{DAC}(k+1)$$

where

$$V_{DAC}(k+1) = V_{ref} \text{ for } V_o(k) < V_{ref}$$

$$V_{DAC}(k+1) = -V_{ref} \text{ for } V_o(k) > V_{ref}$$

C_3 and C_1 are charged to the residual voltage. The residual voltage is compared with the reference to obtain the next bit in the conversion and thus decide the next

DAC voltage to be subtracted from the next residue. Phase 1 is shown in figure 5.10.

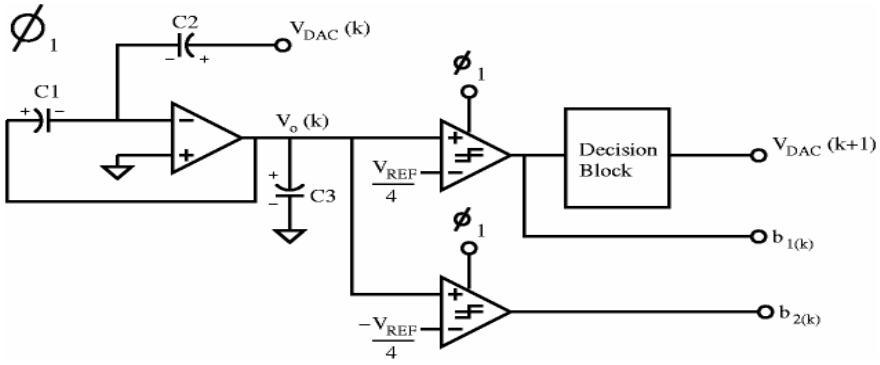


Figure 5.10 Phase 1

Phase 2: During this phase capacitors C_2 and C_3 are interchanged (C_1 and C_3 have the same potential stored on them), C_3 is connected to DAC voltage and the next residue is obtained. The next bit is obtained by comparing the residue to the reference. Phase 2 is shown in figure 5.11.

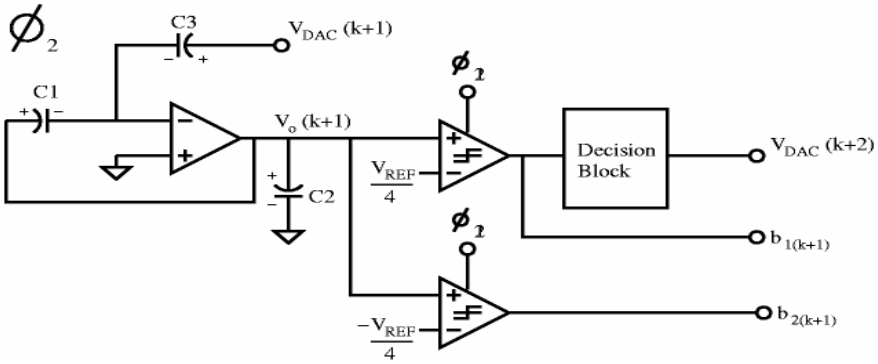


Figure 5.11 Phase 2

The outputs of both the comparators are used in the decision block to determine the DAC voltage to be subtracted from the input in next cycle.

5.4 An Alternative Approach

A pipelined converter proposed in "A 250-mW, 8-b, 52-Msamples/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers"[14] can also be used as an algorithmic A/D converter which is capable of providing 1.5 Bit/phase. The architecture of this converter is described in the following section.

This converter uses 4 capacitors and one amplifier. The switching arrangement is similar to the basic multiply-by-2 circuit described earlier.

Reset Phase: During this phase, the capacitors C_1 and C_2 are charged to the input voltage and the op-amp is connected in unity gain feedback (op-amp is in reset). Capacitors C_3 and C_4 are the load to the amplifier. Figure 5.12 depicts the reset phase.

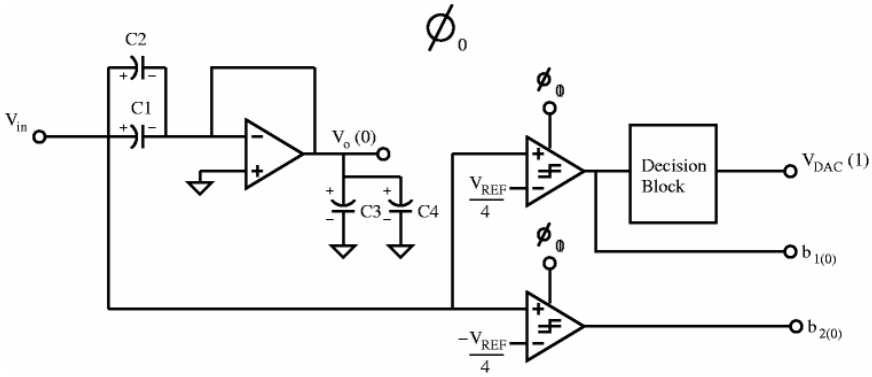


Figure 5.12 Reset Phase

The DAC voltage for the next conversion is also obtained during this phase using the 2 comparators.

Phase 1: In this phase, Capacitor C_2 is connected across the op-amp and C_1 discharges into C_2 to produce the desired residue and C_3 and C_4 act as load

capacitors and store the residual output. Figure 5.13 shows this phase. The residue is defined by the previous equations.

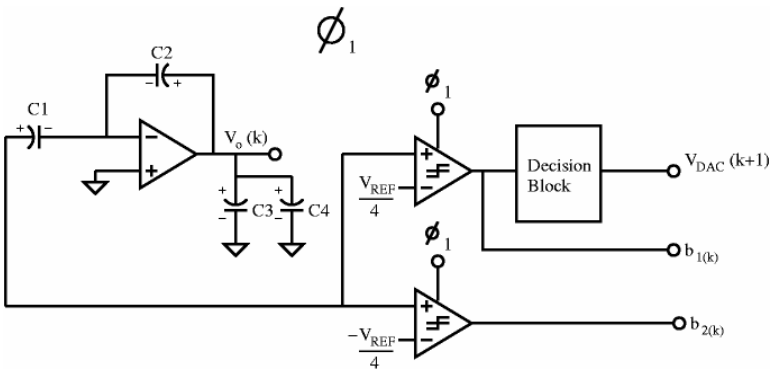


Figure 5.13 Phase 1

Phase 2: In this phase C_1 and C_2 are connected as the load to the amplifier. C_4 is connected across the amplifier and C_3 discharges into C_4 to produce the residue and this process continues. Figure 5.14 describes the operation in this phase.

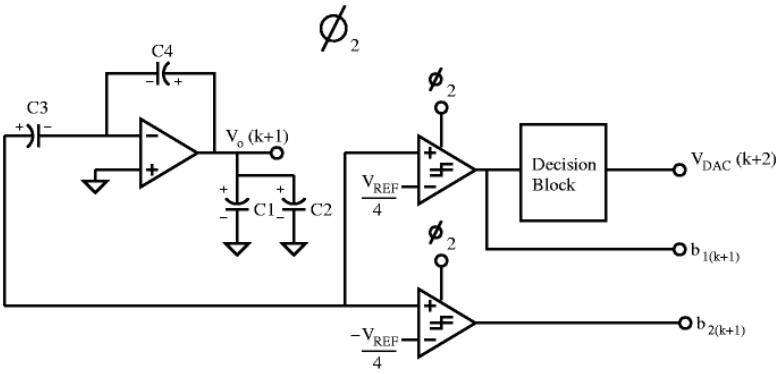


Figure 5.14 Phase 2

Only one amplifier is used and it is switched between both the phases. The operation is similar to the one described in figure 4.3. The use of 4 capacitors enables the 1.5-bits /phase.

The operation of both the architectures and their performances with respect to non-idealities is described in the next chapter. Also a comparison table is built for easy reference.

CHAPTER 6

Performance Limitations

This chapter deals with the non-idealities present in the system and gives solutions to overcome them. The two approaches described in chapter 5 are compared according to the non-idealities. The system level simulation for the proposed architecture was performed in C language and MATLAB was used to analyze the results.

6.1 Non-idealities

The SNR performance of a system is degraded by thermal noise in the system. Other non-idealities lead to greater INL and DNL in the system that leads to poorer distortion performance. The major causes of non-linearities can be divided as DC and dynamic.

Causes of DC non-linearity include amplifier and comparator offsets, capacitor mismatch, amplifier finite gain and non-linearity, capacitor non-linearity, charge injection.

Causes of dynamic non-linearity include amplifier settling, comparator insensitivity and charge injection.

6.1.1 Comparator offsets

Comparator offsets lead to a shift in the transfer curve as shown before and thus lead to non-linearity in the converter. 1-bit/phase architecture cannot tolerate comparator offsets since the residue goes out of bounds thus making it impossible to correct digitally. This makes the comparator design complex and leads to loss of

speed. This can be overcome by moving to 1.5-bit/phase architecture. Even though the transfer curve is affected, it affects the decision boundaries where the residue does not cross its bounds. A comparator offset greater than $\frac{V_{ref}}{4}$ is required for the residues to cross the analog bounds. Larger comparator offsets imply smaller correction range. Thus comparator design is simpler and does not trade off speed for accuracy.

In both the algorithmic approaches, 1.5-bit/phase architecture is used to overcome comparator offsets and redundant digital error correction is used to get the correct digital output code. Hence the performance of both the approaches with respect to comparator offsets is similar.

6.1.2 Amplifier offsets

Amplifier offset effect increases exponentially with each residue in both converter approaches.

6.1.2.1 Proposed approach

Figure 6.1 explain the effect of amplifier offset. Only amplifier offset is considered. During the reset phase, C_1 and C_2 are charged to $V_{in} - V_{os}$, where V_{os} is the offset of the amplifier. C_3 is charged to V_{os}. During phase 2, C_1 is connected across the op-amp and C_2 is connected to $V_{dac}(1)$ and hence the final output is given by $V_o(1) = 2V_{in} - V_{dac}(1)$. C_3 is charged to this voltage. Now in the next phase C_2 becomes the load and C_3 is connected between the virtual ground node of the op-amp and $V_{dac}(2)$. C_1 is always connected across the amplifier. The 2nd residue is given by $V_o(2) = 2V_o(1) - V_{dac}(2) + V_{os} = 2^2 V_{in}\text{-}2V_{dac}(1)\text{-}V_{dac}(2) + V_{os}$.

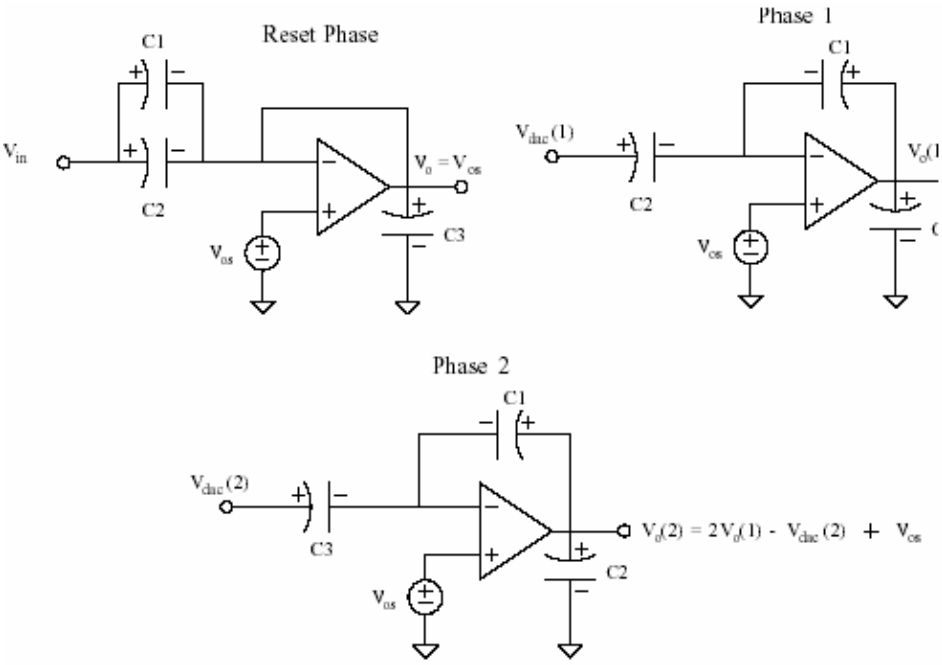


Figure 6.1 Effect of amplifier offset in the proposed approach

The following equations give the k[th] residue.

$$V_o(1) = 2V_{in} - V_{dac}(1)$$

$$V_o(2) = 2V_o(1) - V_{dac}(2) + V_{os}$$

$$= 2^2 V_{in} - 2V_{dac}(1) - V_{dac}(2) + V_{os}$$

$$V_o(3) = 2V_o(2) - V_{dac}(3) + V_{os}$$

$$= 2^3 V_{in} - 2^2 V_{dac}(1) - 2V_{dac}(2) - V_{dac}(3) + (2+1)V_{os}$$

.

.

$$V_o(k) = 2^k V_{in} - 2^{k-1} V_{dac}(1) - 2^{k-2} V_{dac}(2) - \ldots\ldots\ldots - V_{dac}(k) + (2^{k-2} + 2^{k-3} + \ldots\ldots + 1)V_{os}$$

$$V_o(k) = 2^k V_{in} - 2^{k-1} V_{dac}(1) - 2^{k-2} V_{dac}(2) - \ldots\ldots\ldots - V_{dac}(k) + (2^{k-1} - 1)V_{os}$$

Thus it is evident from the above equations that the offset effect increases exponentially. The input and the first residue are not affected by the offset and hence the MSB (first bit) and the 2[nd] bit are not affected by the offset.

If redundancy correction were not used, this exponential increase in offset would result in residues going beyond the analog bounds, and hence in error that cannot be corrected. But the correction makes the offset of the amplifier give rise only to an effective offset in the system. The transfer curve of the ADC shifts left or right depending on the sign of the offset. C code simulation of the architecture with redundancy correction gives the following plot in figure 6.2 for different offsets. The plot corresponds to 10 bit resolution with Vref = 1V.

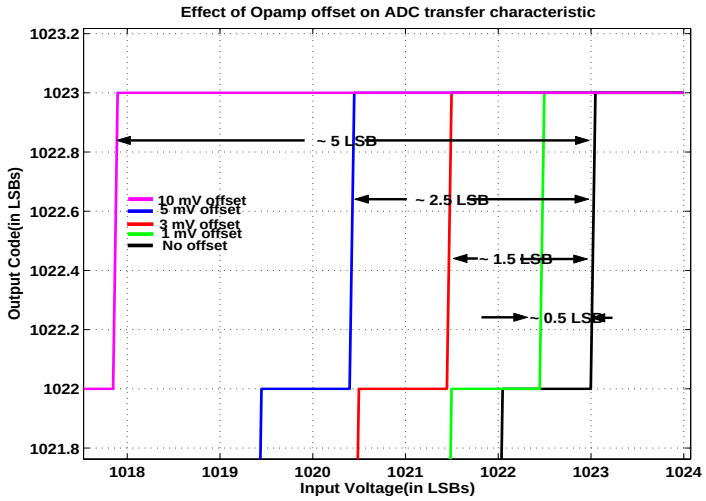


Figure 6.2 Amount of charcateristic curve shift due to offset with redundancy correction. 10 bit resolution and Vref = 1V

From the plot it can be seen that the final offset after redundancy correction is twice the original amplifier offset. Any fixed offset in a system can be corrected by calibrating it out. The output of a system with its input connected to zero or the common-mode is the output offset of the system, which can be stored digitally. For any other input, the offset can be subtracted form the output digitally. The effective dynamic range of the system is reduced by the presence of the offset since the ADC is overloaded for lower inputs. But the reduction in DR is very negligible since the reduction is in a few LSBs.

6.1.2.2 Nagaraj Approach

Figures 6.3 explain the effect of amplifier offset for the circuit of [14]. Only amplifier offset is considered. During the reset phase, C_1 and C_2 are charged to $V_{in} - V_{os}$, where V_{os} is the offset of the amplifier. C_3 and C_4 are charged to V_{os}. During phase 2, C_1 is connected across the op-amp and C_2 is connected to $V_{dac}(1)$ and hence the final output is given by $V_o(1) = 2V_{in} - V_{dac}(1)$. C_3 and C_4 are charged to this voltage. Now in the next phase C_1 and C_2 become the load to the op-amp, C_3 is connected across the amplifier and C_4 is connected between the virtual ground and $V_{dac}(2)$. The 2nd residue is thus given by

$$\begin{aligned} V_o(2) &= 2V_o(1) - V_{dac}(2) + V_{os} \\ &= 2^2 V_{in} \text{-} 2V_{dac}(1) \text{-} V_{dac}(2) + V_{os} \end{aligned}$$

The following equations give the effect of amplifier offset in Nagaraj architecture.

$$V_o(1) = 2V_{in} - V_{dac}(1)$$

$$\begin{aligned} V_o(2) &= 2V_o(1) - V_{dac}(2) + 2V_{os} \\ &= 2^2 V_{in} \text{-} 2V_{dac}(1) \text{-} V_{dac}(2) + 2V_{os} \end{aligned}$$

$$\begin{aligned} V_o(3) &= 2V_o(2) - V_{dac}(3) + 2(2+1)V_{os} \\ &= 2^3 V_{in} - 2^2 V_{dac}(1) - 2V_{dac}(2) - V_{dac}(3) + 2(2+1)V_{os} \end{aligned}$$

.

.

$$V_o(k) = 2^k V_{in} - 2^{k-1} V_{dac}(1) - 2^{k-2} V_{dac}(2) - \ldots\ldots\ldots - V_{dac}(k) + 2(2^{k-2} + 2^{k-3} + \ldots\ldots + 1)V_{os}$$

$$V_o(k) = 2^k V_{in} - 2^{k-1} V_{dac}(1) - 2^{k-2} V_{dac}(2) - \ldots\ldots\ldots - V_{dac}(k) + 2(2^{k-1} - 1)V_{os}$$

Fom the above equations the effect of op-amp ofset is double in Nagaraj's scheme compared to the proposed architecture. Most of the offsets which can cause errors in the system are reduced to a final offset due to the redundancy correction.

6.1.3 Finite Op-amp Gain

The finite gain of an op-amp in any system leads to the inverting input node of the op-amp not being a virtual ground. Consider the multiply-by-2 circuit shown in figure 6.4.

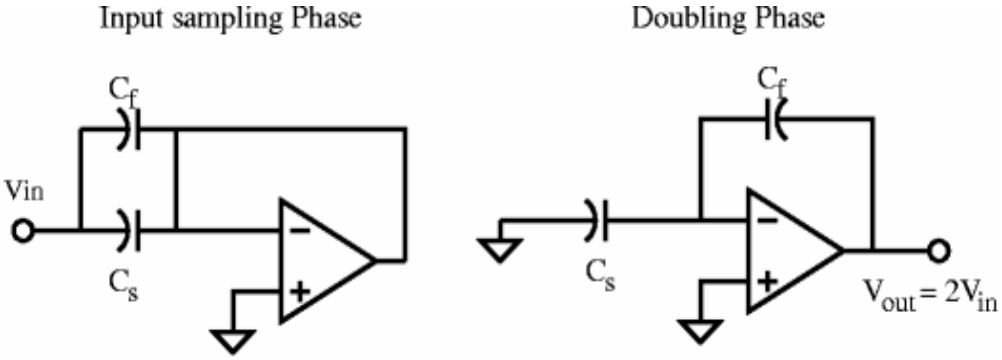


Figure 6.4 Multiply-by-2 circuit

In the ideal case where the op-amp gain is assumed to be infinite, the virtual ground of the op-amp is fixed at the common mode or analog ground, and hence the residue is given by $V_o = \frac{C_s + C_f}{C_f} V_{in} = 2V_{in}$ for $C_s = C_f$. With finite gain A of the op-amp, the potential of the virtual ground node changes with the residue at the output of the op-amp, and is given by $V_{vgnd} = \frac{V_o}{-A}$. This leads to a change in the gain of the circuits as given by the following equation

$$V_o = \frac{C_s + C_f}{C_f(1 + \frac{1}{A} + \frac{C_s}{C_f A})} V_{in} \approx 2(1 - \frac{2}{A})V_{in}$$

A parasitic capacitance is present at the virtual ground node of the op-amp. This is due to the parasitics of the capacitors and switches connected to that node and also due to the input capacitance of the op-amp. The parasitic capacitance drains out some of the charge from Cs and hence all of the charge of Cs does not

get transferred to Cf. The finite gain increases the effect of this parasitic capacitance. The output equation is modified as shown below

$$V_o = \frac{C_s + C_f}{C_f(1 + \frac{1}{A} + \frac{C_s + C_p}{C_f A})} V_{in} \approx 2(1 - \frac{1}{A} - \frac{C_p}{C_f A}) V_{in},$$

where C_p is the parasitic capacitance at the virtual ground node of the op-amp. This leads to a further reduction in the gain of the above stage. C_p is charged and discharged in each phase in the above structure and hence it does not carry the effect of one residue to another. So there is no memory effect.

A reduction in the gain of the above circuit leads to a deviation in the transfer curve from the ideal. The finite gain effect is reflected in change in the slope of the transfer curve between decision boundaries. Ideally the slope is 2. Figures 6.5 and 6.6 below show the effect of gain > 2 and a gain < 2 on the transfer curve for the 1.5-bit architecture.

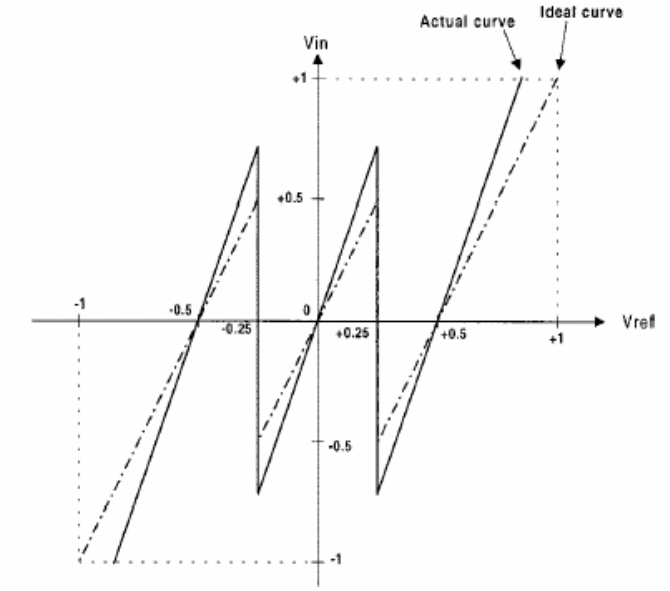


Figure 6.5 Transfer curve for an interstage gain > 2 [1]

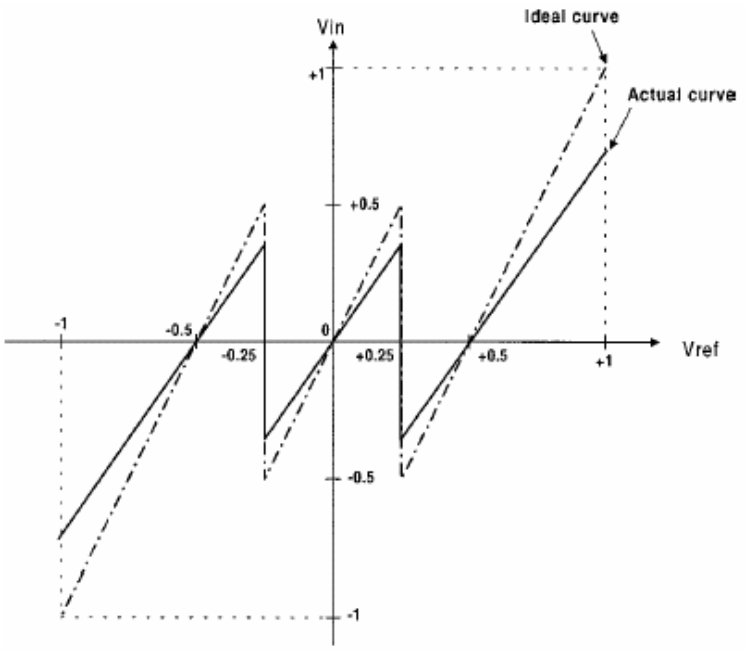


Figure 6.6 Transfer curve for gain < 2 [1]

For a finite gain op-amp used, the gain of the stage is always less than 2 and hence figure 6.6 is applicable.

Due to the change in the transfer curve codes with varying widths and missing codes may result and this leads to INL and DNL, thus leading to poor performance. Digital calibration can be used to correct for this error in the case of high-resolution converters. For lower resolutions, system level simulations can be performed to determine the gain of the op-amp for which the INL and the DNL < 1 LSB.

6.1.3.1 Proposed Approach

In the proposed approach, the finite gain of the amplifier causes the following modification in the residual voltage.

$$V_o(k) = \left[2 - \frac{1}{Ao}(3)\right] V_o(k-1) - \left[1 - \frac{1}{Ao}(2)\right] V_{dac}(k)$$

With a parasitic capacitance at the virtual ground node of the op-amp the equation changes to

$$V_o(k) = \left[2 - \frac{1}{Ao}\left(3 + \frac{C_p(1 - \frac{V_o(k)}{V_o(k-1)})}{C}\right)\right] V_o(k-1) - \left[1 - \frac{1}{Ao}\left(2 + \frac{C_p(1 - \frac{V_o(k)}{V_o(k-1)})}{C}\right)\right] V_{dac}(k)$$

The parasitic capacitance is never discharged in this approach, and hence two consecutive residues determine the change in the charge of the parasitic capacitance. This leads to a memory effect wherein one residue affects the next. System level simulations were performed on the architecture using C code and MATLAB was used to analyze the results. The minimum gain of the op-amp that can contain INL and DNL of the system within 1 LSB was determined to be about 70 dB. The simulations were done assuming all the three capacitors are equal and the parasitic capacitance is 20 % of the main capacitors. No other non-ideality was assumed to be present.

The following figures show the INL and DNL plots for different finite gains of the op-amp. For the simulations, capacitor mismatch of 0.2 % was assumed and a parasitic capacitance of 1.2 pF was assumed.

Figure 6.7 shows the plot for an op-amp of gain 60 dB (1000). The maximum INL exceeds the 1 LSB limit and hence a 60 dB gain will lead to a reduction in linearity performance.

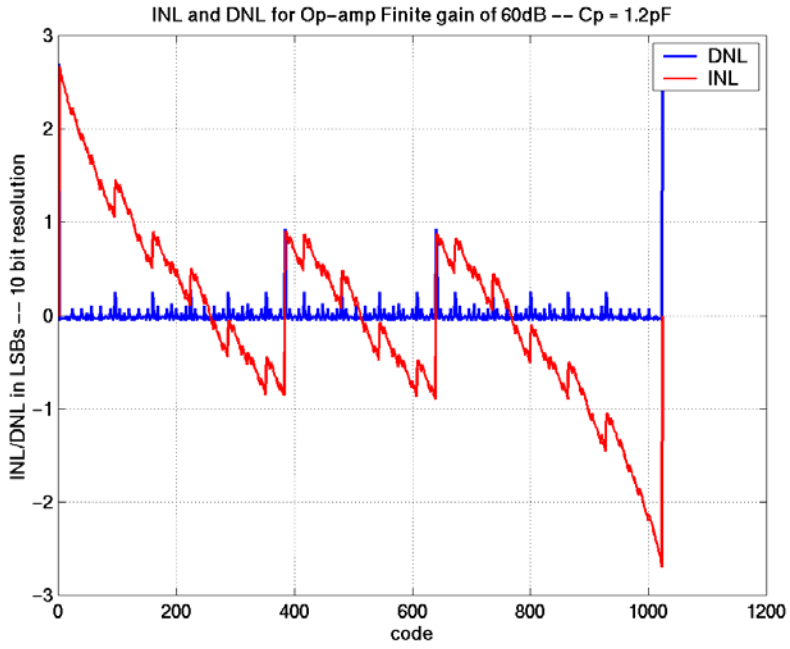


Figure 6.7 INL and DNL for op-amp gain of 60 dB

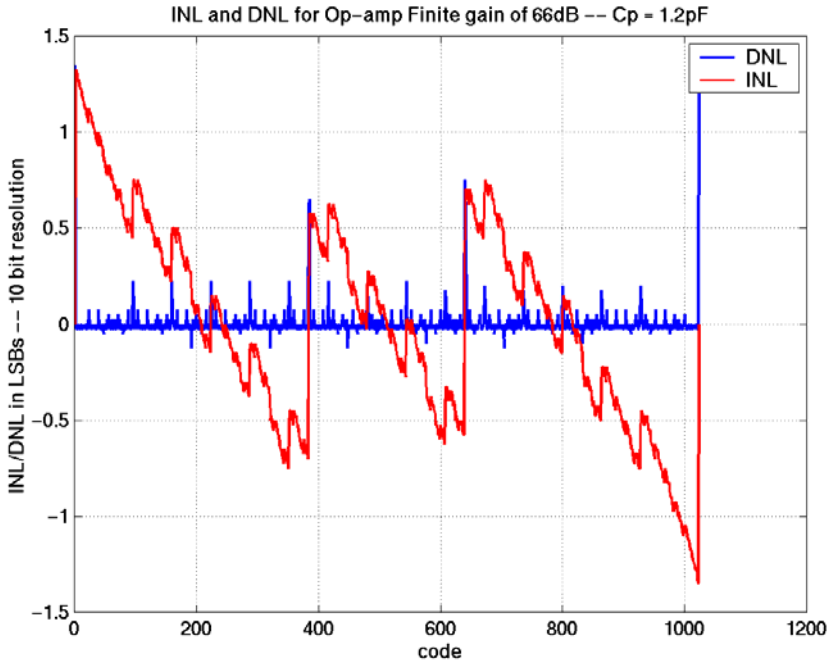


Figure 6.8 INL and DNL for op-amp gain of 66dB

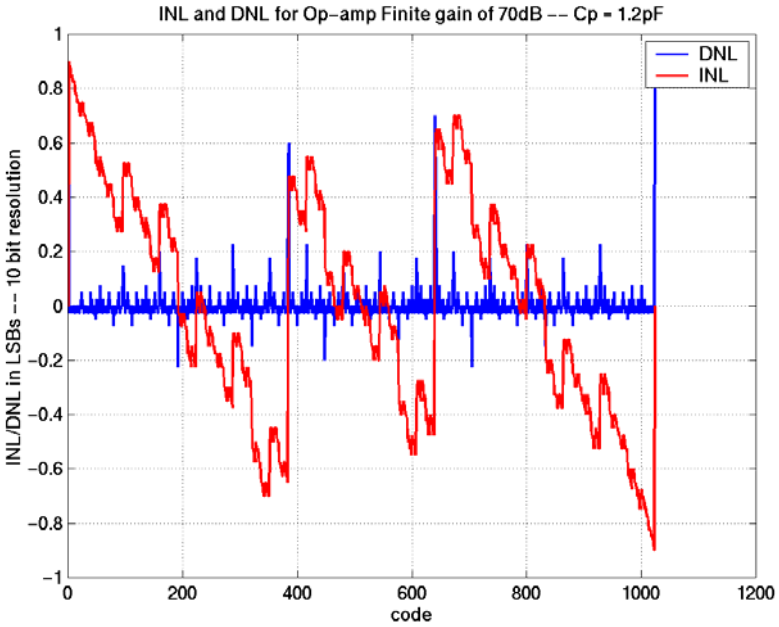


Figure 6.9 INL and DNL for op-amp gain of 70dB

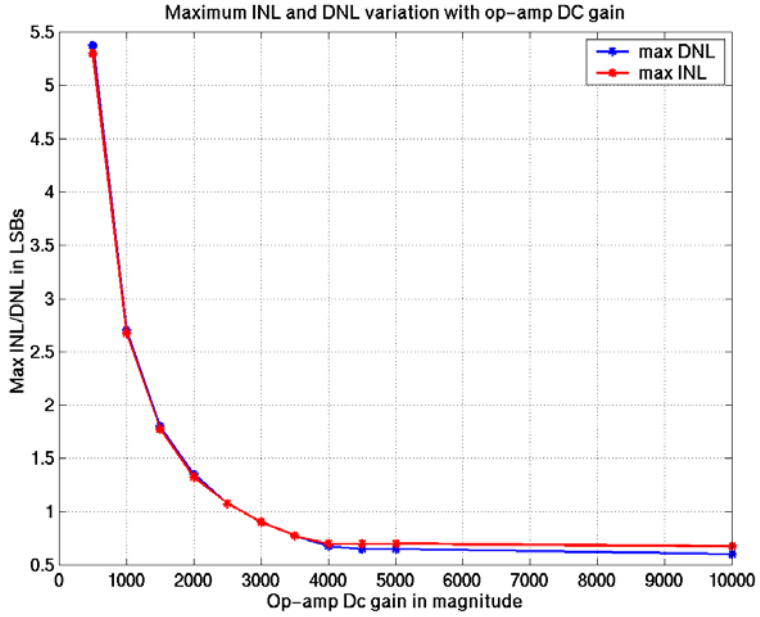


Figure 6.10 INL and DNL variation with op-amp gain

Figure 6.8 and Figure 6.9 above show the INL and DNL plots for a gain of 66dB and 70dB respectively. Thus from the plots and simulations the gain requirement of the op-amp is 70dB. Since the presence of capacitor mismatch and parasitic capacitance at the virtual ground node of the op-amp can increase the requirement the simulations were done in the presence of 2% capacitor mismatch and a parasitic capacitance of 0.3pF. This showed a gain requirement of 74dB for the op-amp. Figure 6.10 shows the variation of the maximum INL and DNL with op-amp DC gain.

6.1.3.2 Nagaraj Approach

The following equations show the effect of finite gain with and without parasitic capacitances respectively:

$$V_o(k) = \left[2 - \frac{1}{Ao}(4)\right] V_o(k-1) - \left[1 - \frac{1}{Ao}(2)\right] V_{dac}(k)$$

$$V_o(k) = \left[2 - \frac{1}{Ao}\left(4 + \frac{C_p(1 - \frac{V_o(k)}{V_o(k-1)})}{C}\right)\right] V_o(k-1) - \left[1 - \frac{1}{Ao}\left(2 + \frac{C_p(1 - \frac{V_o(k)}{V_o(k-1)})}{C}\right)\right] V_{dac}(k)$$

Thus the memory effect is present in this system too. The amount of memory effect is dependent on the change in the residues. The gain requirement of this approach was nearly equal to that of the proposed approach.

6.1.4 Capacitor Mismatch

Switched capacitor circuits need precise ratio of capacitors. The capacitance is usually given by $C = \frac{\varepsilon_{ox}}{t_{ox}} A$, where A is the area, ε_{ox} is the permittivity of oxide and t_{ox} is the oxide thickness. Under-etching[9][8] represents the major source of error in capacitor mismatch. Under etching leads to the resultant area being smaller than the required area. To over come this effect all capacitors are realized using unit capacitors. Thus under etching will be present in all the unit capacitors and the ratio will hence remain a constant.

The second major cause for mismatch is oxide gradient[9][8]. As shown in the above equation, any change in the oxide thickness will lead to a change in the capacitance. To overcome the thickness gradient a common centroid approach or interspersing approach can be used to match capacitors.

The bottom plate of a capacitor has a parasitic of about 20% and the top plate has a parasitic of about 5%. Thus noise coupling through the bottom plate is high. Hence only the top plate should be connected to critical nodes such as op-amp virtual ground.

Capacitor mismatch leads to gain error in the multiply-by-2 circuit. This leads to a change in the transfer curves and thus leads to INL and DNL as shown in section 6.1.3.

In a conventional algorithmic converter only two capacitors are involved and hence one mismatch factor. But in the proposed algorithmic converter, three capacitors are involved to increase the speed of the converter and this results in 2 mismatch terms. Thus mismatch affects the present design more than the conventional architecture.

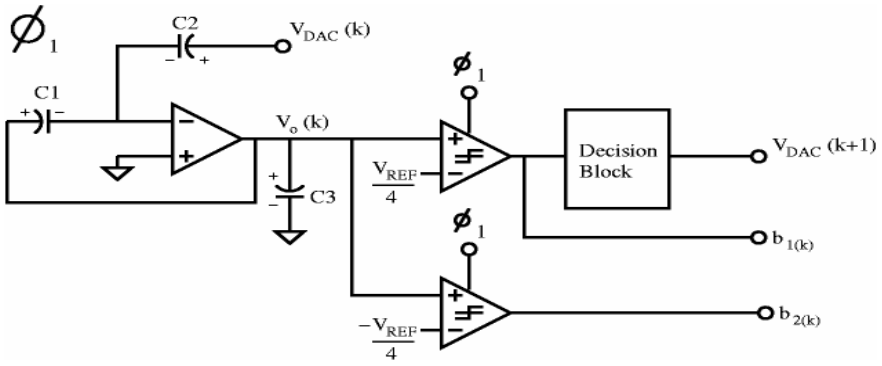


Figure 6.11 Phase 1 circuit configuration

During Phase 1 (figure 6.11), only C_1 and C_2 are involved in the charge transfer and produce the residue. For $C_2 = C_1(1+\alpha)$ the following equation represents the residue during this phase.

$$V_o(n) = V_{in} \cdot (2+\alpha)^{\frac{n-2}{2}} (2+\beta)^{\frac{n}{2}} - V_{dac}(1) \cdot (1+\alpha)(2+\alpha)^{\frac{n}{2}} (2+\beta)^{\frac{n-2}{2}}$$
$$- V_{dac}(2) \cdot (1+\beta)(2+\alpha)^{\frac{n-2}{2}} (2+\beta)^{\frac{n-2}{2}} \ldots\ldots - V_{dac}(n) \cdot (1+\beta)$$

During phase 2 (figure 6.12), C_1 and C_3 are involved. For $C_3 = C1(1+\beta)$, the following equation represents the residue during this phase.

$$V_o(n) = V_{in} \cdot (2+\alpha)^{\frac{n+1}{2}} (2+\beta)^{\frac{n-1}{2}} - V_{dac}(1) \cdot (1+\alpha)(2+\alpha)^{\frac{n-1}{2}} (2+\beta)^{\frac{n-1}{2}}$$
$$- V_{dac}(2) \cdot (1+\beta)(2+\alpha)^{\frac{n-1}{2}} (2+\beta)^{\frac{n-3}{2}} \ldots\ldots - V_{dac}(n) \cdot (1+\alpha)$$

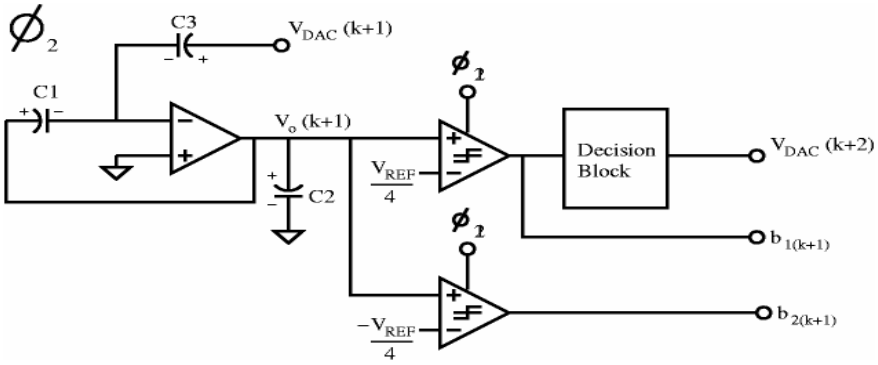


Figure 6.12 Phase 2 circuit configuration

Simulations were performed in MATLAB and C Language to determine the performance of the converter in the presence of capacitor mismatch. The INL and the DNL was plotted for different mismatch coefficients to determine the tolerance of the architecture. Figure 6.13 shows the plots for 0.2% mismatch. The converter resolution is 10 bits.

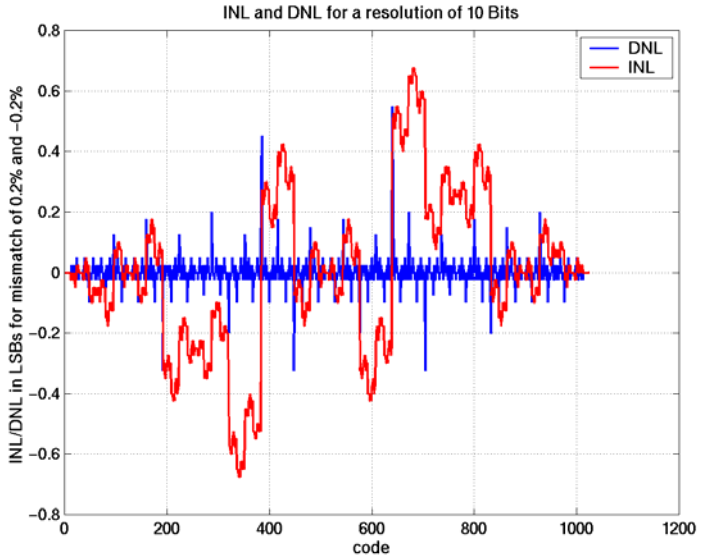


Figure 6.13 INL and DNL for cap mismatch of 0.2 %

The INL and the DNL of a converter should be less than 1 LSB for good linearity performance. The above plot shows that for $\alpha = 0.2\%$ and $\beta = -0.2\%$ the maximum INL and the maximum DNL of the system do not exceed 1 LSB. Hence the above mismatch is a tolerable mismatch for the resolution of the converter (10 bits). Figure 6.14 shows the INL and DNL for $\alpha = 0.3\%$ and $\beta = -0.3\%$.

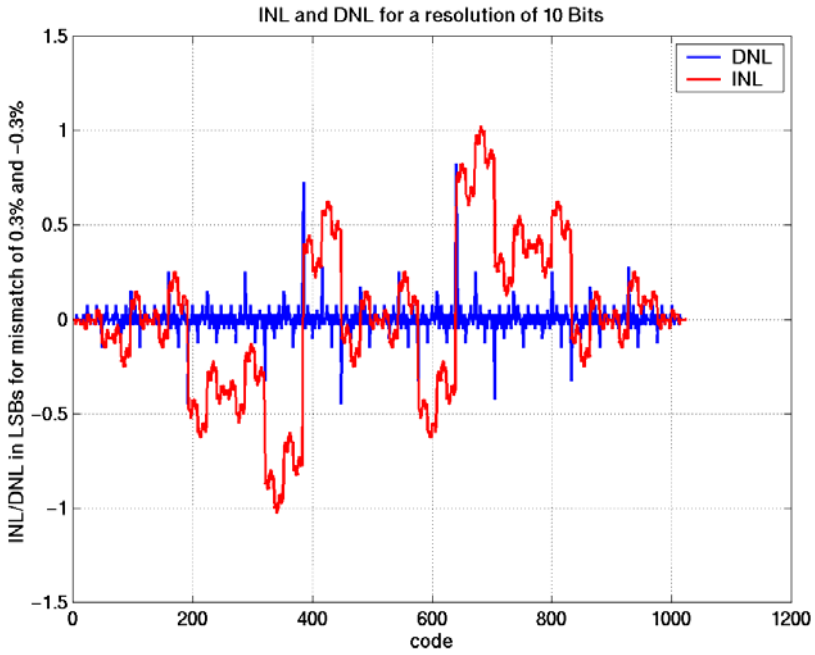


Figure 6.14 INL and DNL for cap mismatch of 0.3 %

As shown in the plot the maximum INL exceeds 1 LSB and hence this will result in more than tolerable non-linearity. Hence the proposed converter architecture can tolerate 0.2% capacitor mismatch.

The maximum INL and DNL were found to be less than above when the mismatches have the same sign. Hence simulations were performed for the worst case mismatches (both the mismatches of different sign).

The following plot (figure 6.15) gives the maximum INL and maximum DNL as a function of the mismatch percentage

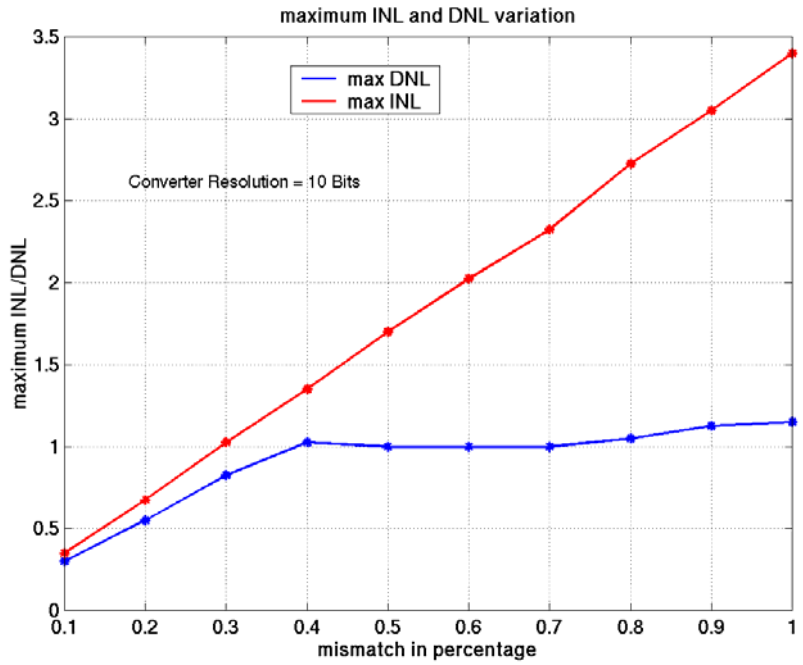


Figure 6.15 Maximum INL and DNL for varying capacitor mismatch

From the above plot, maximum INL varies linearly with respect to mismatch. The present design is done only for 10 bits of resolution and hence there is no need for calibration techniques to compensate for capacitor mismatch.

6.1.5 Thermal Noise

In a switched capacitor circuit, the R_{on} of the switch contributes the noise when it is ON. This noise is sampled and so folds and the mean square voltage noise of the sampled circuit is given by $\frac{kT}{C}$ where k is the Boltzmann constant, T is the absolute temperature and C is the capacitance.

Consider the multiply-by-2 circuit shown in figure 6.16. During phase 1, C_1 and C_2 charge to the noise voltage of the resistor which is given by $4kTR_{on}$ and the

effective integrated noise charge power across each of the capacitors is given by kTC_1 and kTC_2 respectively.

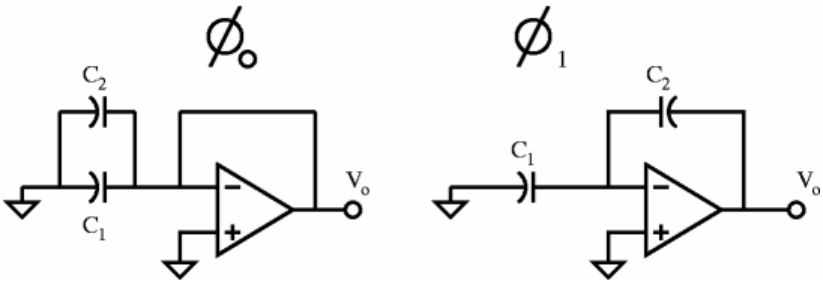


Figure 6.16 Multiply-by-2 circuit

During phase 2, C_1 and C_2 get another $kTC_1 + kTC_2$ noise charge and hence the total noise voltage at the output is given by $\frac{2kT}{C_2}\left(1+\frac{C_1}{C_2}\right) \approx \frac{4kT}{C}$ where $C_1 = C_2 = C$. Now the signal gain of the circuit is 2 and hence the total input-referred noise is given by $\frac{kT}{C}$.

The thermal noise of the op-amp must also be taken into account. Consider the op-amp in a feedback configuration as shown by figure 6.17

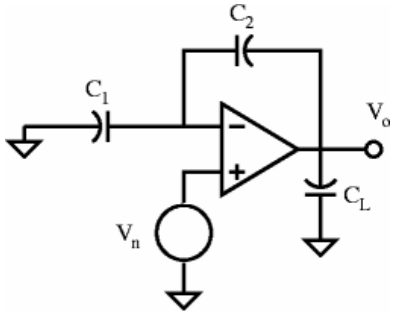


Figure 6.17 Op-amp in feedback

Assuming a parasitic capacitance C_p at the virtual ground node of the op-amp the effective load capacitance is given by $C_{L,eff} = C_L + \frac{C_2(C_1 + C_p)}{C_1 + C_2 + C_p}$. The thermal noise PSD of an op-amp is given by $\overline{V_n^2} = 2 \cdot 4kT \cdot \frac{2}{3} \cdot \frac{1}{g_m}(1 + N_f)$ where gm is the transconductance of the input pair and N_f is the noise factor given by the sum of ratios of the transconductance of other transistors and the input transconductance. The closed loop gain of the amplifier is given by $1 + \frac{C_1 + C_p}{C_2}$. Thus the input referred integrated noise power of the op-amp is given by

$$\text{Total input referred noise power of the op - amp} = \frac{4kT(1 + N_f)}{3C_{L,eff}} \cdot \frac{1 + \frac{C_1 + C_p}{C_2}}{\left(\frac{C_1}{C_2}\right)^2}$$

The input referred noise of the op-amp is dependent on the feedback factor and load capacitance and independent of the transconductance.

For $C_1 = C_2 = C$ and $C_p << C$, the total input referred noise of the multiply-by-2 circuit is given by $\overline{V_{n,stg}^2} = \frac{kT}{C} + \frac{8kT(1 + N_f)}{3C_{L,eff}}$. For an algorithmic converter, which has the above architecture, the total noise of the converter is given by $V_{n,tot}^2 = V_{n,1}^2 + \frac{V_{n,2}^2}{4} + \frac{V_{n,3}^2}{16} + ...$

In the above equation each term represents the noise contribution in each cycle.

6.1.5.1 Noise in the proposed architecture

In the proposed architecture, C_1 is not switched except in the first cycle. C_2 and C_3 are the switched capacitors. Hence after the first cycle, C_1 does not contribute of the noise of the system.

During the first cycle the noise is composed of switched noise of C_2 and C_3 and the amplifier's noise. The amplifier is in a feed back structure similar to the one shown in figure 6.17 but with C_1 and C_2 interchanged. C_1 acts as the feed back capacitor. The feedback factor, the effective load and the op-amp noise are given by the following equations

$$\beta = 1 + \frac{C_2 + C_p}{C_1}$$

$$C_{L,eff} = C_L + \frac{C_1(C_2 + C_p)}{C_1 + C_2 + C_p}$$

$$\text{Total input referred noise power of the op - amp} = \frac{4kT(1+N_f)}{3C_{L,eff}} \cdot \frac{1 + \frac{C_2 + C_p}{C_1}}{\left(\frac{C_2}{C_1}\right)^2}$$

For $C_1 = C_2 = C$, and for $C_p << C$, the above equation reduces to $\frac{8kT(1+N_f)}{3C_{L,eff}}$. The effective load of the op-amp reduces to $C_{L,eff} = C_L + \frac{C}{2}$. Thus only its effective load determines the noise of the op-amp. The noise of the switched structure is given by $\frac{kT}{C}$. For $C_1 = C_2 = C >> C_p$, the above equation reduces to $\frac{kT}{C}$. Thus the total noise in the first cycle is given by the following equation

$V_{n,1}^2 = \frac{kT}{C} + \frac{8kT(1+N_f)}{3C_{L,eff}}$. From the second cycle C_1 does not play any role in the noise of the system, since it is not switched from here on and hence the noise contribution is only by the switched ones. C_3 acquires a noise charge of kTC as a load of the op-amp and when it is connected between the virtual ground node and $V_{dac,}$ it acquires the same charge again and hence in the subsequent cycles the noise contribution due to switched capacitors is halved. The noise of subsequent stages is given by

$V_{n,i}^2 = \frac{kT}{2C} + \frac{8kT(1+N_f)}{3C_{L,eff}}$ where i represents i^{th} cycle. Each cycle of the converter has a gain of 2 and hence the noise of the subsequent cycles is reduced by the gain of the previous cycles and the total noise of the converter is given by the following equation.

$V_{n,tot}^2 = V_{n,1}^2 + \frac{V_{n,2}^2}{4} + \frac{V_{n,3}^2}{16} + ...$, where $V_{n,2}^2 = V_{n,3}^2 = ... = V_{n,i}^2 = V_{n,o}^2$. The total noise is given by $\frac{7}{6} \cdot \frac{kT}{C} + \frac{4}{3} \cdot \frac{8kT(1+N_f)}{3C_{L,eff}}$. For good optimization the op-amp noise is assumed to be equal to the noise due to the switched capacitors and the effective noise is $\frac{14}{6} \cdot \frac{kT}{C}$. The SNR of a N-bit converter is given by 6N and for a 10-bit conversion the required SNR is given by 60 dB. The capacitance C is determined from the following equations using the SNR required. The converter is run for 11 cycles and redundancy correction is used to bring it down to 10 bits. A margin of 3 bits is given for any non-ideality in determining the capacitance. Hence a 14 bit SNR is required.

$SNR(mag) = \frac{V_{ref}^2}{V_n^2}$.

$V_n^2 = 14\frac{kT}{C}\cdot\frac{f_o}{f_s}$, where f_O is the signal bandwidth and f_S the sampling frequency. A ratio of 0.1 is assumed for $\frac{f_o}{f_s}$. From the above equations it can be shown that, $C \geq 10^{0.6N}\cdot\frac{28kT}{6V_{ref}^2}$. For N = 14 bits, C > 1.16pF is required. Since the op-amp noise is half of the total noise the SNR is 81dB. Using the above procedure, the effective load of the op-amp is obtained to be >1.11pF. Since $C_{L,eff} = C_L + \frac{C}{2}$, the load CL of the op-amp is calculated to be > 0.53pF.

6.1.5.2 Noise in Nagaraj Approach

In this approach all the capacitors are switched and hence the noise in all the cycles are the same as given by $V_{n,1}^2 = \frac{kT}{C} + \frac{8kT(1+N_f)}{3C_{L,eff}}$. The total noise of the converter in this approach is given by $\frac{4}{3}\cdot\frac{kT}{C} + \frac{4}{3}\cdot\frac{8kT(1+N_f)}{3C_{L,eff}}$. Thus the noise in this converter is higher than the one proposed. Using the same procedure as above, the minimum capacitance requirements for C and CL are given by 1.326pF and 0.55pF. Thus the load on the op-amp is 4 times higher than in the proposed converter.

6.1.6 Switch Non-idealities

The MOS switches used in the system have the following non-idealities:

6.1.6.1 Non-zero ON resistance

The ON resistance of a MOS switch of size W/L is given by

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})}$$

where V_{gs} and V_{th} are the gate source and the threshold voltage of the switch respectively. This leads to a non-zero acquisition time for the switch given by $\tau = R_{on}C$, where C is the capacitor charged through the switch. More problematic is the signal dependent ON resistance of a switch connected to a varying node. This introduces distortion.

The size of the switch can be calculated using the time constant of the switch. In most switched capacitor applications the available charge time for the switch is known and is usually half the time period of the clock. Thus

$$\frac{W}{L} \geq \frac{28C}{T_{clk}\mu C_{ox}(V_{gs} - V_{th})}$$ for 0.1% accuracy

Usually CMOS transmission gates are used to give full range for the switch. For $V_{in} > V_{dd} - V_{thn}$, NMOS switches are OFF and for $V_{in} < V_{thp}$, PMOS transistors are OFF. Thus T-gates help in allowing a rail-to-rail input range.

6.1.6.2 Charge Injection

When a switch turns ON, a channel consisting of the major carrier is formed between the source and the drain region[6]. For a switch to turn OFF this charge has to become zero i.e. the charge has to flow out to the external circuit. Since the switch charges capacitors, some of the channel charge of the switch flows into the capacitor. This causes an error voltage step to occur in the potential across the capacitor.

The charge of a MOS switch is given by $Q_{ch} = WLC_{ox}(V_{gs} - V_{th})$. For switches connected to the input $V_{gs} = V_{in}$. The threshold voltage of a transistor is given by

$V_{th} = V_{tho} + \gamma\left(\sqrt{\left|V_{sb} + 2\phi_f\right|} + \sqrt{\left|2\phi_f\right|}\right)$, where Vsb is the source bulk potential. Since the source is at V_{in} for a switch connected to the input, this makes the threshold voltage a non-linear function of V_{in} and results in non-linear charge being dumped on to the capacitor. Harmonic distortion is the result of signal dependent charge injection. The charge from a switch can produce an offset, a gain error and non-linearity.

Consider the following switched capacitor circuit shown in figure 6.18. Switch S_1 is connected to the input whereas switch S_2 is connected to analog grounds or DC voltages. S2 will produce a constant charge being dumped into the capacitor thus producing only an offset that can be cancelled by CDS techniques. S_1 introduces non-linear charge injection. One way to reduce this effect is to cut off S_2 earlier than S_1, thus leaving the circuit open, and hence the charge of S_1 cannot affect capacitor. A delayed clock signal is used for S_1. The above technique is used in the design of the converter to reduce signal dependent charge injection.

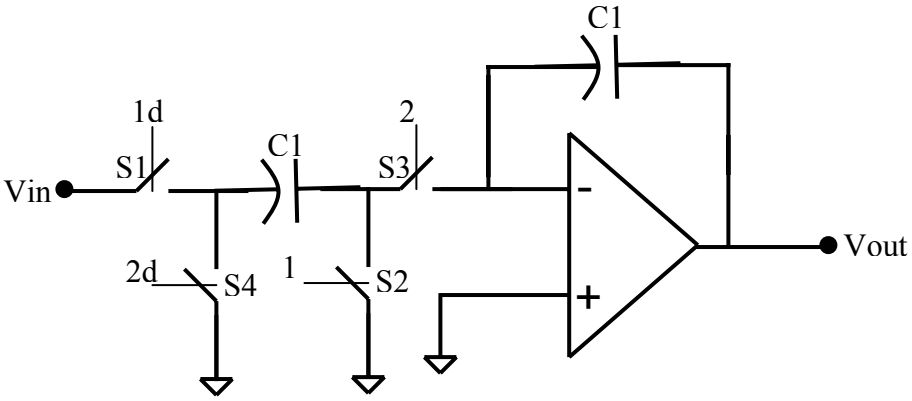


Figure 6.18 A switched capacitor integrator

6.2 Comparison of power requirements in the architectures

The effective load of the op-amp determines its power consumption. The unity gain bandwidth of the op-amp is related to the load as $UGBW = \frac{g_m}{C_{L,eff}}$, where gm represents the trans-conductance of the input pair. For 2 op-amps of same bandwidth but different loads the ratio of their trans-conductance is given by $\frac{g_{m1}}{g_{m2}} = \frac{C_{Leff1}}{C_{Leff2}}$. Also the trans-conductance of a MOS transistor in saturation is given by $g_m = \sqrt{2I\mu C_{OX}\frac{W}{L}}$, where I is the current through the transistor

μ is the mobility of the carriers

Cox is the oxide capacitance

W and L are the width and length respectively

Thus the currents through 2 transistors are related to their trans-conductance as $\frac{I_1}{I_2} = \left(\frac{g_{m1}}{g_{m2}}\right)^2 = \left(\frac{C_{Leff1}}{C_{Leff2}}\right)^2$. For the above 2 approaches the ratio is 4. Thus the power consumption in Nagaraj scheme is 4 times that of the power consumption in the proposed scheme.

6.2.1 Comparison Chart

The following table compares the 2 architectures

	Proposed Converter	**Nagaraj Converter**
Number of capacitors	3	4
Area	Area is smaller due to lesser capacitors and smaller capacitance	
Noise		Higher noise
Power in op-amp		16 times higher power

		consumption
Op-amp offset		2 times that in the other architecture

Table 6.1 Comparison of the proposed and Nagaraj approach

6.3 System level simulations with single tone inputs

In this section the FFT plots for the output with different input frequencies, capacitor mismatch and op-amp finite gain. The ideal SNR ofr the system is 61.96 dB. With mismatches the total noise represents the THD rather than the SNR of the system.

The following plots show the FFTs for ideal simulations for different frequencies. Figure 6.19 and 6.20 show the FFT plots for an OSR of 64 and 1 respectively.

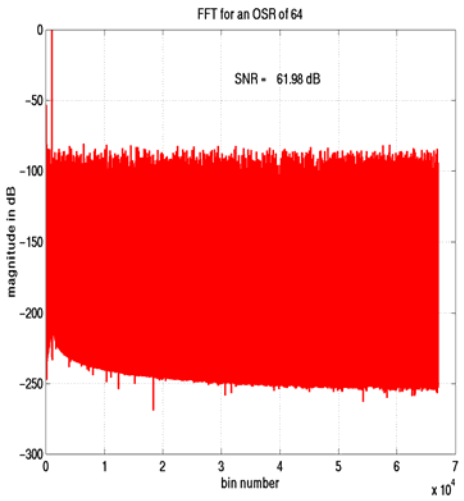


Figure 6.19 FFT at an OSR of 64

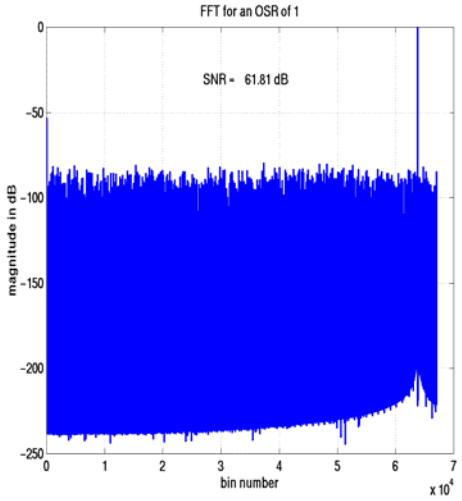


Figure 6.20 FFT at an OSR of 1

The SNR for the 2 over sampling ratios is 61.96 dB and 61.81 dB respectively. Thus the ideal SNR corresponds to 10 bit SNR of 60 dB.

The following plots show the FFT for different capacitor mismatch coefficients. The FFT for a mismatch of 0.1% is shown in figure 6.21. Figure 6.22 shows the FFT for mismatch of 0.2% and 0.3% mismatch is shown in figure 6.23.

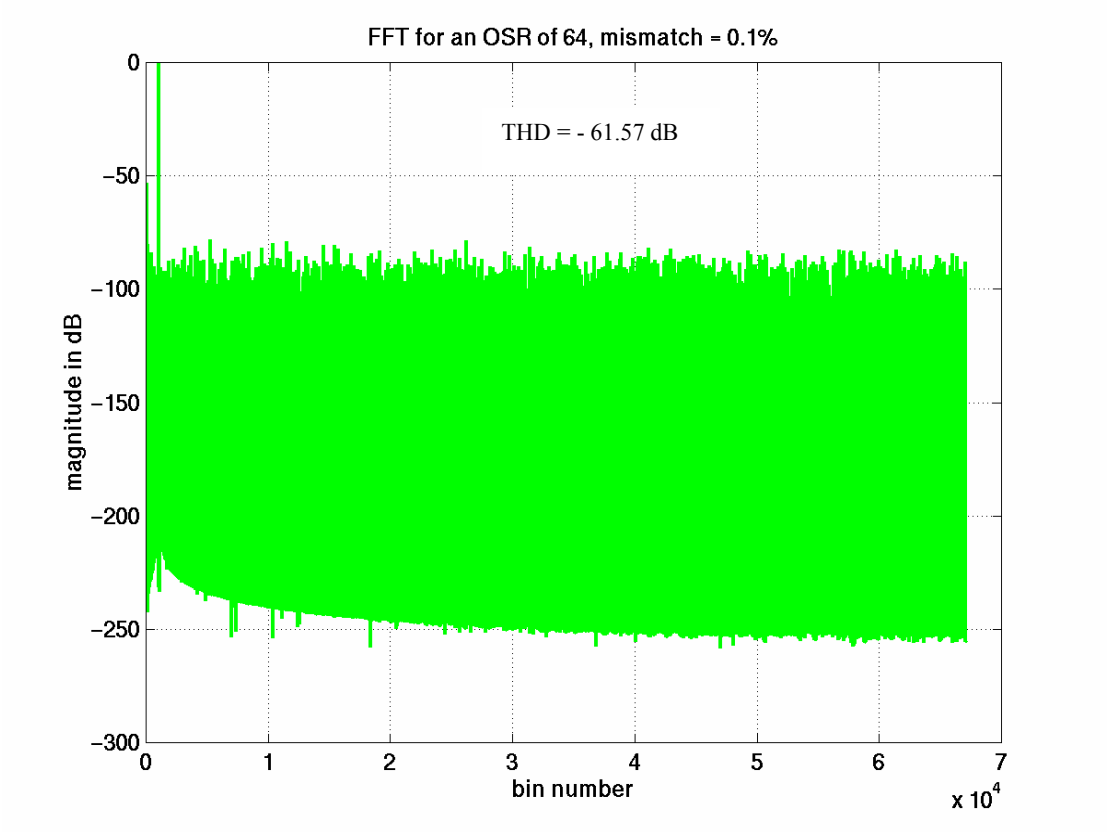


Figure 6.21 FFT for a mismatch of 0.1 %. THD = - 61.57 dB

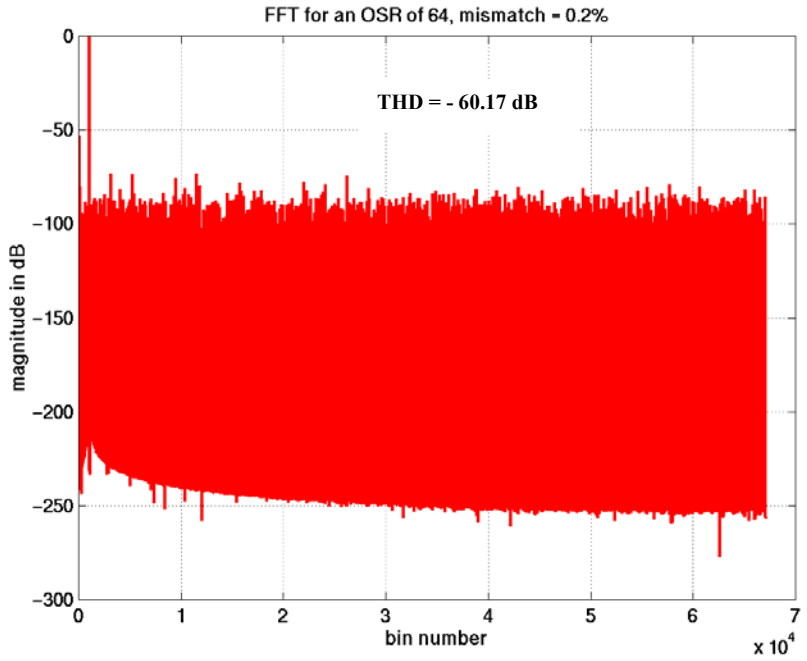


Figure 6.22 FFT for a mismatch of 0.2%. THD = - 60.17 dB

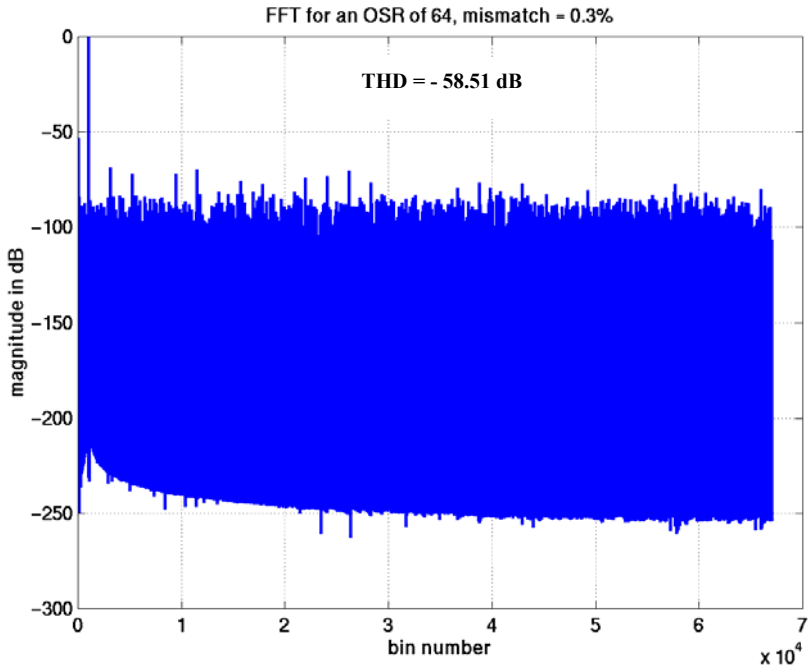


Figure 6.23 FFT for a mismatch of 0.3%. THD = -58.51dB

Thus from the above plots it can be seen that, the maximum allowable mismatch to get a THD of < 60 dB is 0.2 %

Simulations were also done for finite op-amp DC gain and the following plots (figures 6.24 – 6.26) show the FFT for op-amp gains of 60 dB, 66 dB and 70 dB respectively.

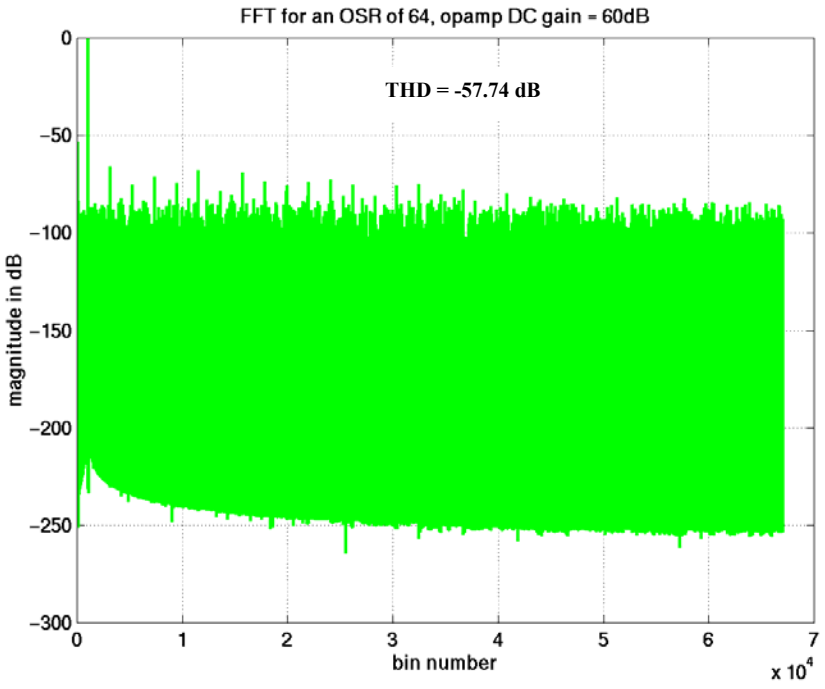


Figure 6.24 FFT for op-amp gain of 60dB

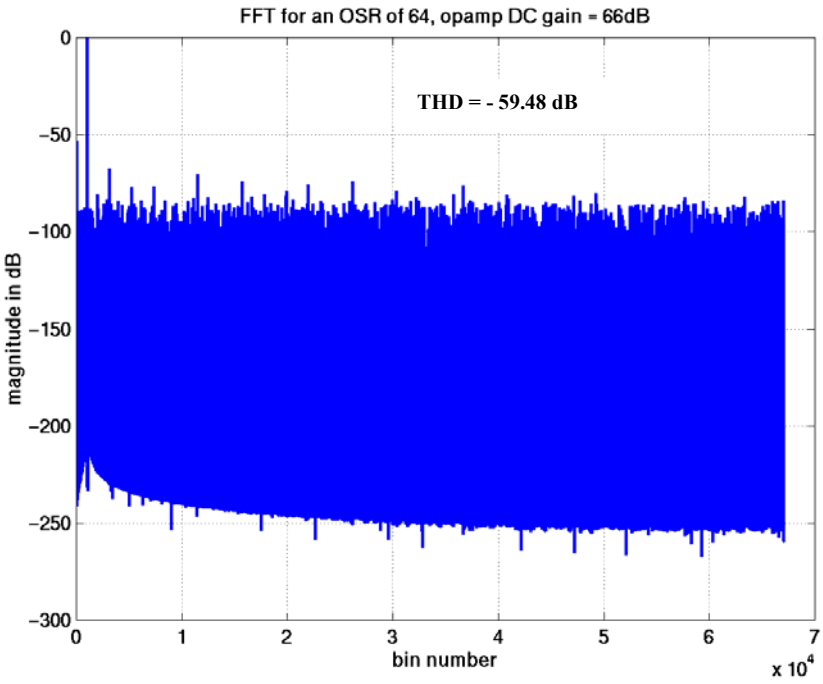


Figure 6.25 FFT for op-amp gain of 66dB

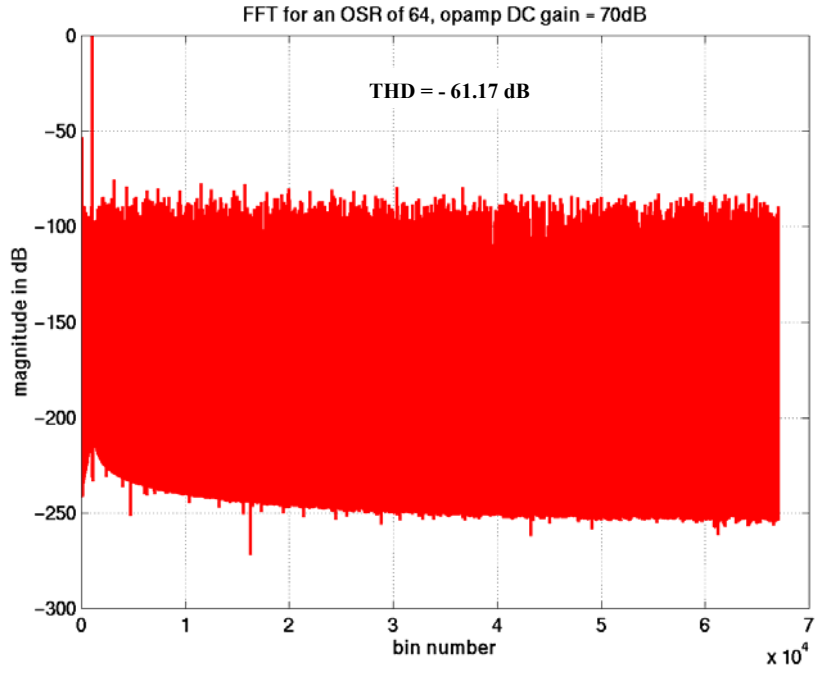


Figure 6.26 FFT for op-amp gain of 70dB

The above simulations were done in the absence of capacitor mismatch and they show that a DC gain of 70 dB is needed for the THD to be below 60 dB. Simulations were also performed with mismatch and finite DC gain and these show that with a mismatch of 0.2%, the DC gain requirement is 74 dB. The plot is shown in figure 6.27.

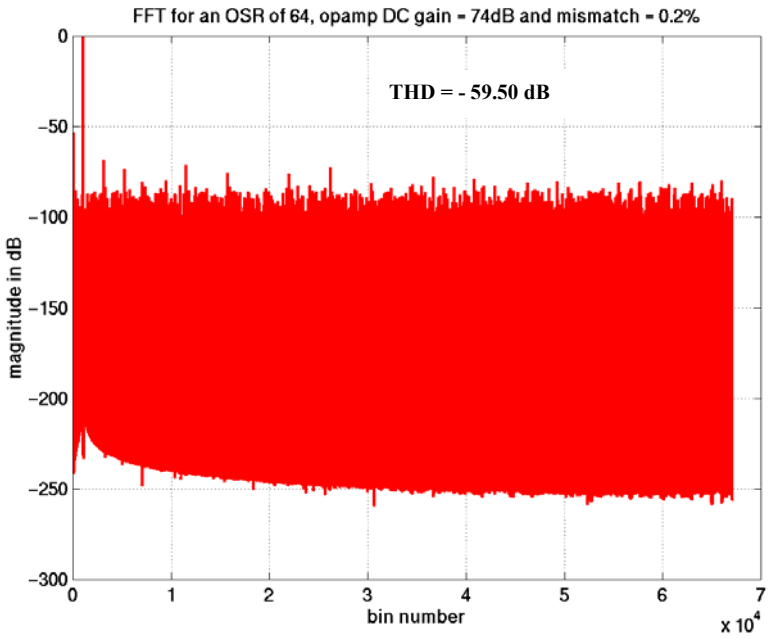


Figure 6.27 FFT with cap mismatch of 0.2 % and op-amp gain of 74dB

6.4 Conclusions

In this chapter the 2 approaches – the proposed and Nagaraj architectures were discussed in detail with respect to non-idealities and non-linearities in the system. System level simulations were performed and the plots were given for the proposed converter. A comparison chart was given and the proposed converter was found to be better than the other.

Chapter 7
Circuit Design

This chapter will discuss the circuit design of some important components of the converter. The design will be discussed for switches, references, op-amps and comparators. The performance of each component will be discussed for different processes and temperatures.

7.1 Op-amp Design

The load capacitance for the op-amp in the proposed approach was derived in the previous chapter. The capacitors $C_1 = C_2 = C_3$ were taken as 2 pF. Hence the maximum load on the op-amp is 3pF. For simulations a load capacitance of 4 pF was used. A two-stage op-amp was selected for this purpose due to the need for a large output swing and large gain requirement.

Since low power design was required the op-amp was designed in sub-threshold. Due to the ambiguity of models in the sub-threshold region, a saturation op-amp was also designed. The two op-amps can be switched externally.

7.1.1 Sub-threshold op-amp

Assuming a 14-bit settling requirement, the settling time required of the op-amp is < 30μs. The design was done for a settling < 25μs worst case. This leads to a design bandwidth of > 150 kHz. The op-amp design was for a bandwidth of 200 kHz worst case. Figure 7.1 shows the schematic of the subthreshold op-amp and figure 7.2 shows the bias circuitry with start-up.

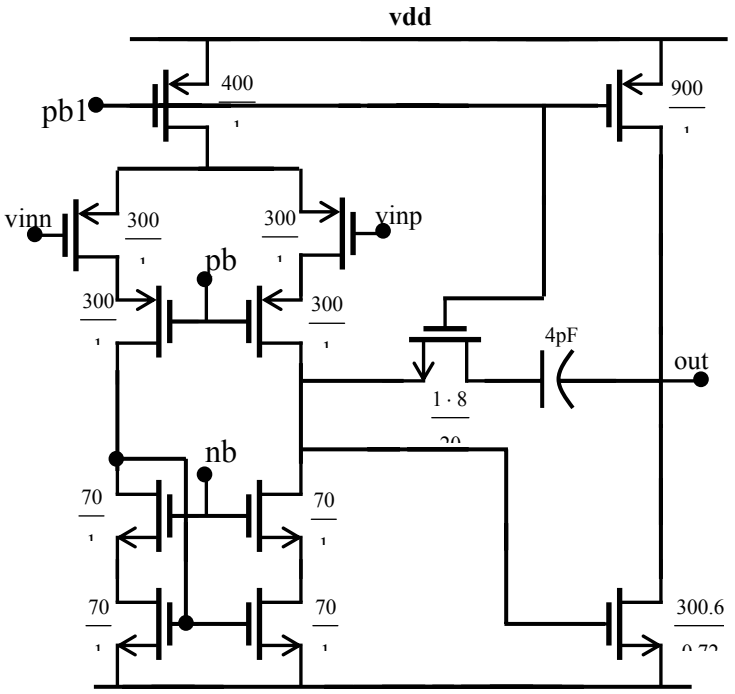


Figure 7.1 Sub-threshold 2-stage amplifier

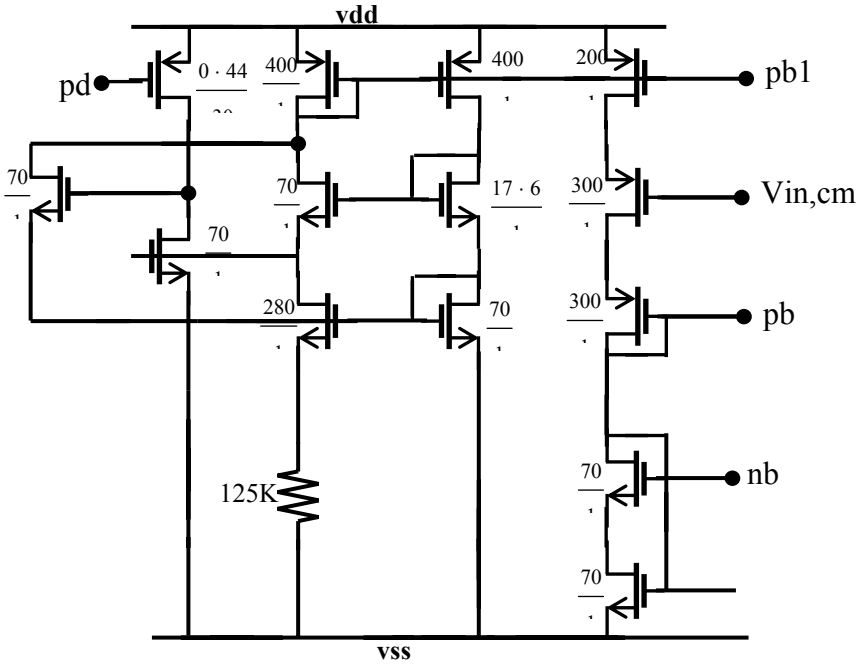


Figure 7.2 Bias circuitry for the above op-amp

All the lengths and widths are in microns. The op-amp was simulated for the worst case corners and the worst case power consumption was found to be 6.5µW and the typical consumption is 5µW. The following plots (figures 7.3 and 7.4) show the frequency response, phase response and the settling response of the op-amp respectively.

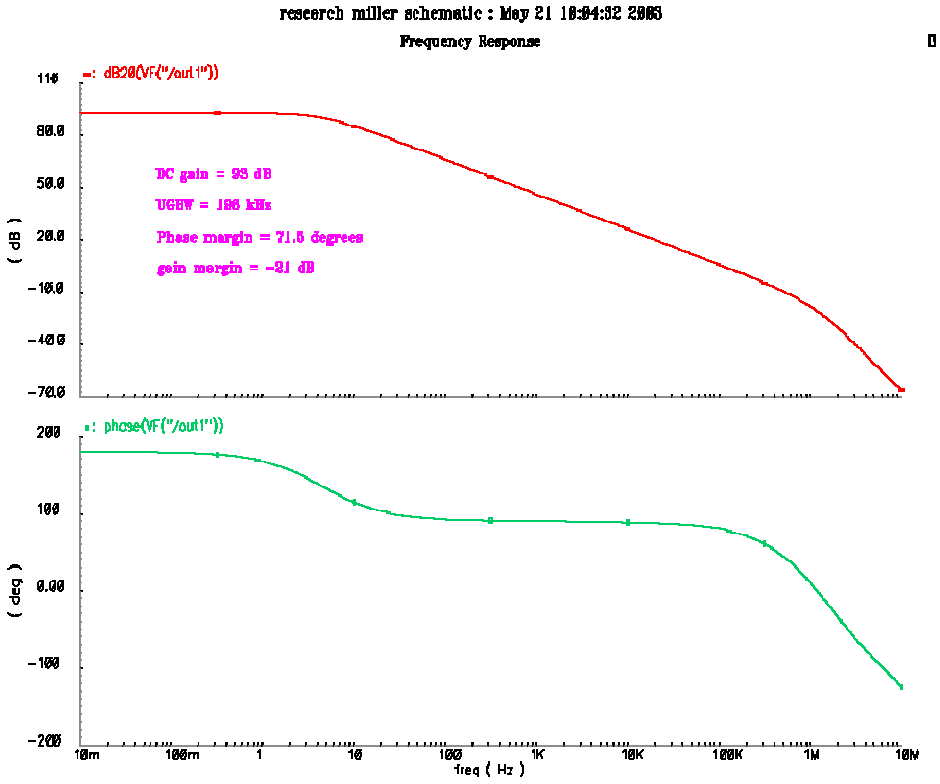


Figure 7.3 Magnitude and phase response of the amplifier

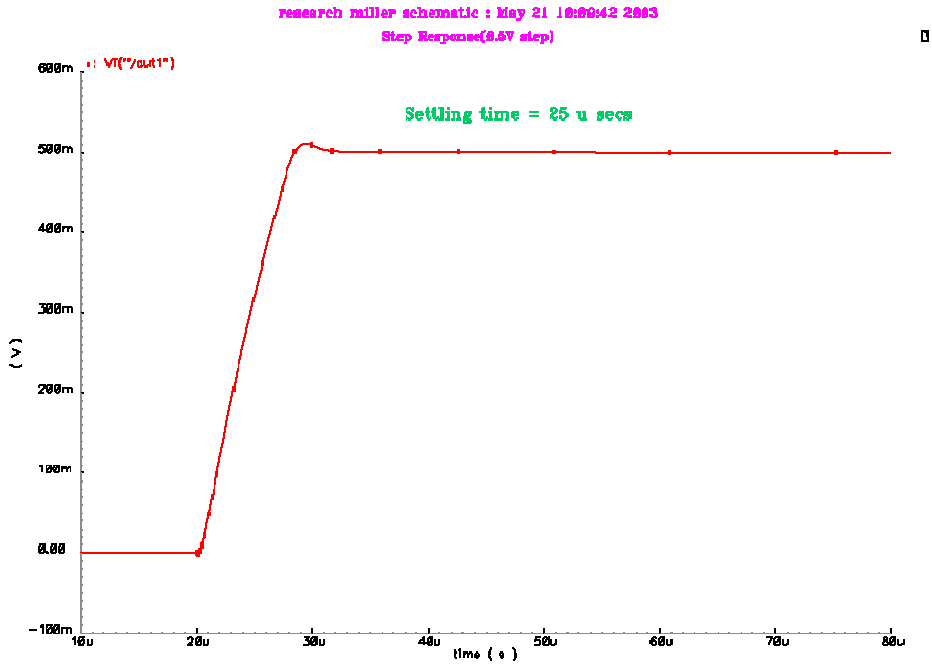


Figure 7.4 Settling response for the sub-threshold amplifier in unity-gain mode

The worst case settling time from the plot is 25μsecs and the worst case UGBW is 194kHz. The phase margin is 71.5 degrees and the gain is 96dB.

7.1.2 Saturation op-amp

The schematic of the saturation op-amp designed has the same structure as the sub-threshold op-amp but with different sizes. This op-amp was over-designed by a large margin. Figures 7.5,7.6,7.7 and 7.8 show the design, bias circuitry, frequency and phase responses and the settling response for the saturation op-amp.

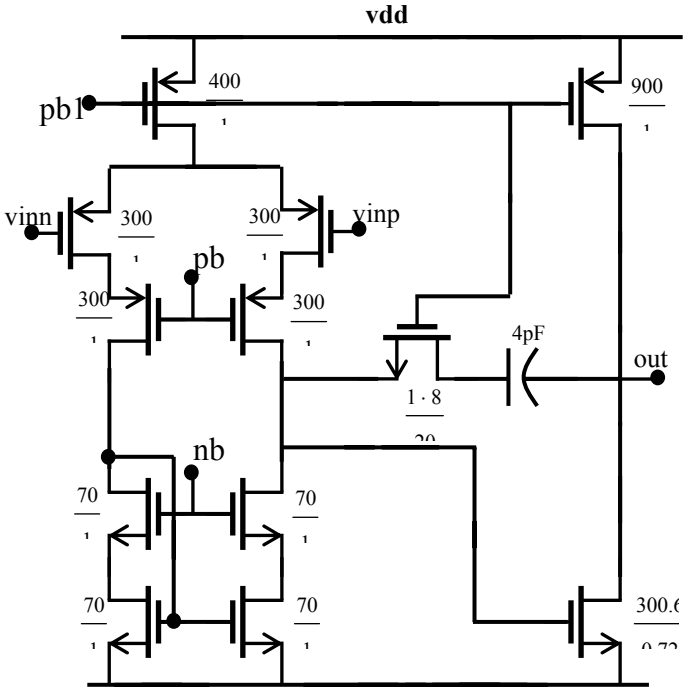


Figure 7.5 Saturation op-amp circuit

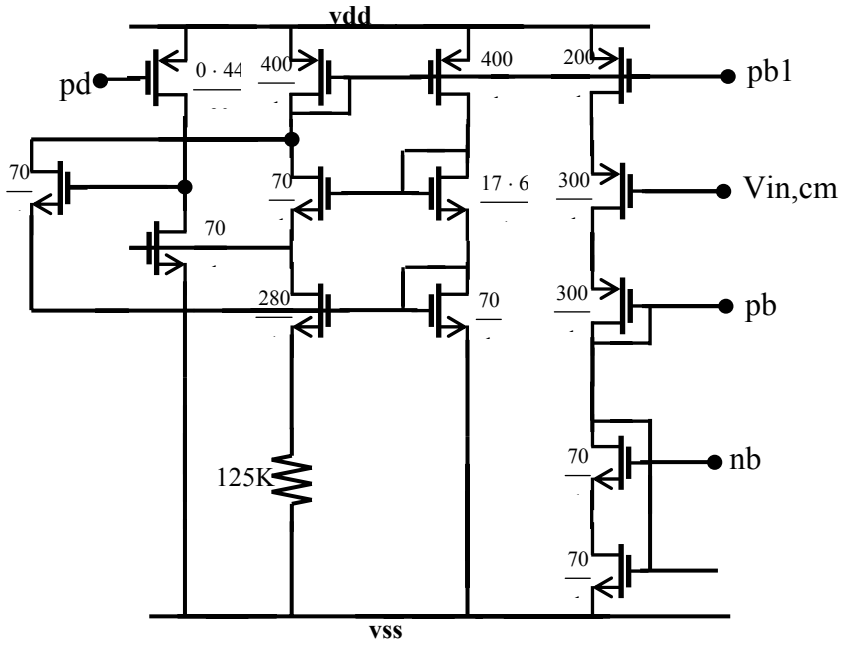


Figure 7.6 Start-up and bias for op-amp of Fig 7.5

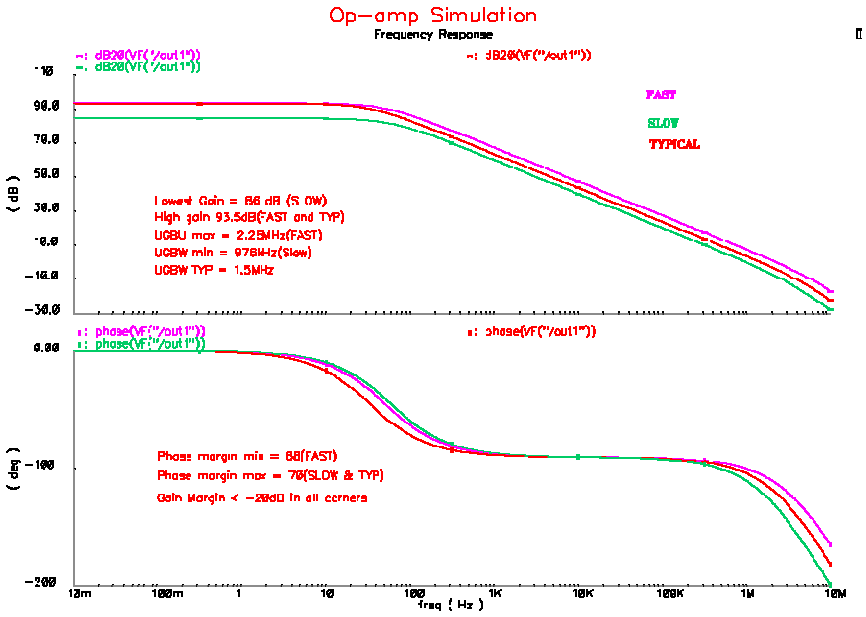


Figure 7.7 Magnitude and phase response

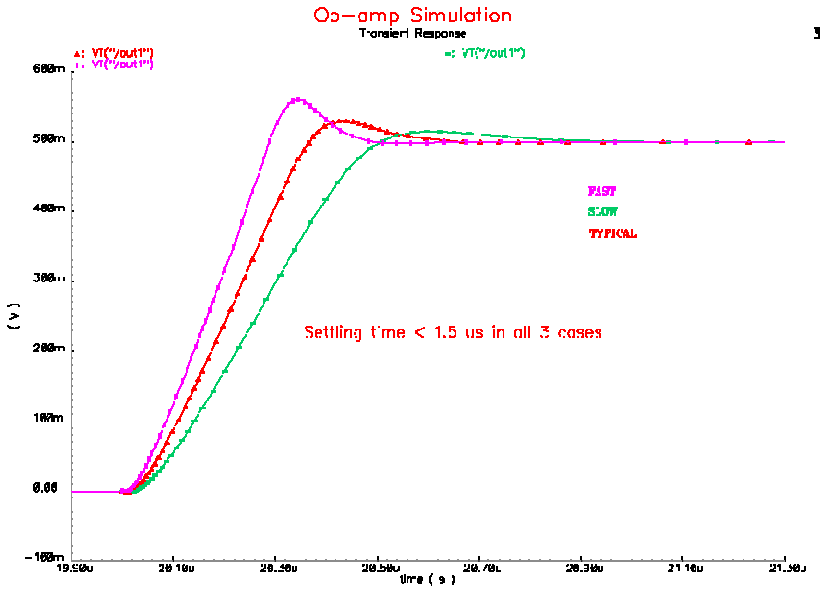


Figure 7.8 Settling response

From simulations the worst case gain is 86dB, UGBW is 1MHz. The op-amp has a maximum power consumption of 92μW and the settling time is < 1.5μsecs.

7.2 Comparator

Redundancy error correction reduces the offset requirement of the comparator and hence fast dynamic latches can be used as comparators. The references for the comparators are derived from a resistor string and hence kickback from the comparator causes the threshold voltages to shift. This was reduced with the help of a low gain pre-amplifier (gain = 5). Figure 7.9 shows the schematic of the designed comparator. Figure 7.10 shows the settling of the comparator. The comparator is fast and it settles within 100nsecs even though the available settling time is 50μsecs.

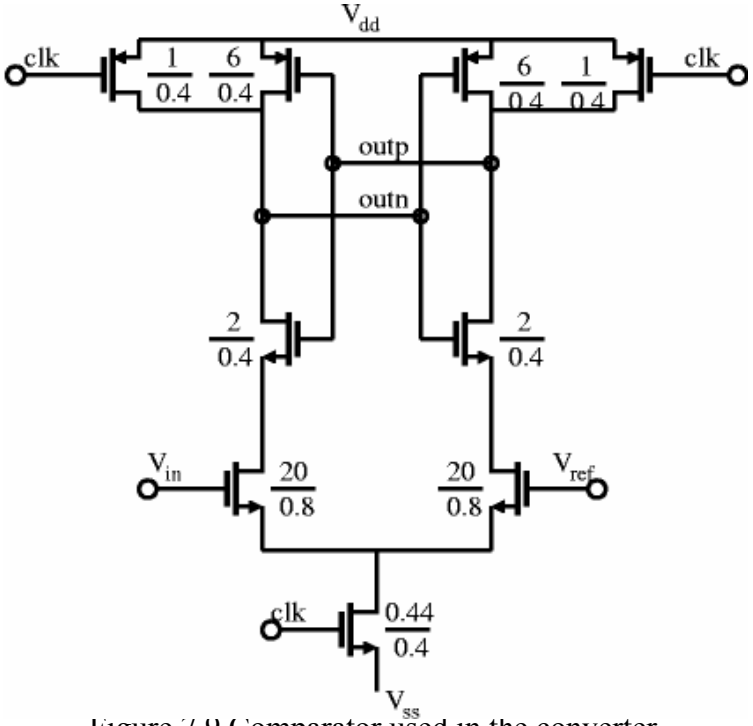


Figure 7.9 Comparator used in the converter

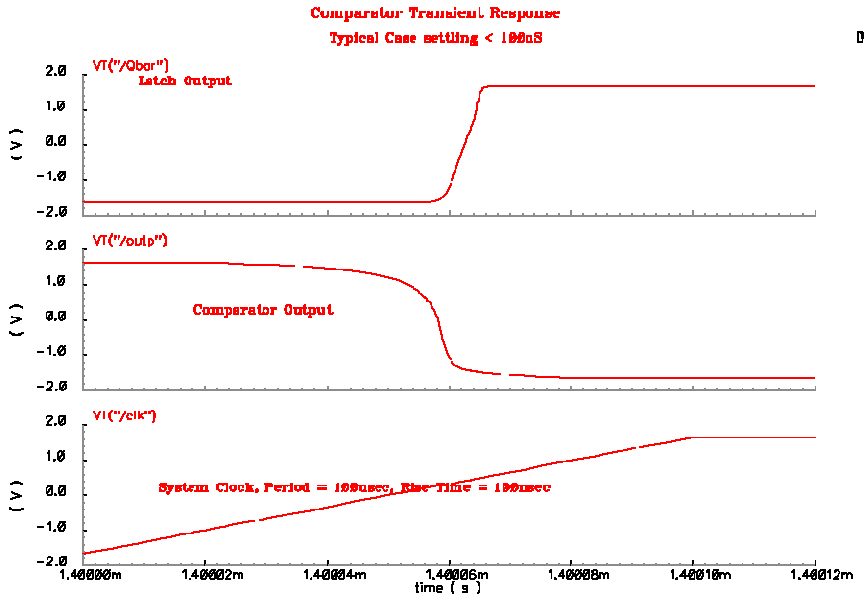


Figure 7.10 Settling response of the comparator

S-R latches were used to overcome the problem of meta-stability in the regenerative latch. The overall switching scheme is given in figure 7.11 and the simulations were performed for 3 process corners, 3 temperatures and 3 supplies.

7.3 References

The references for the comparator were derived using a resistor string and MOS transistors were used to cut off the resistor string during power-down.

7.4 Chip Layout

The chip was designed in 0.18µm CMOS process. Figure 7.11 shows the chip micrograph. Figure 7.12 shows the Algorithmic A/D converter fabricated. The chip is presently under test.

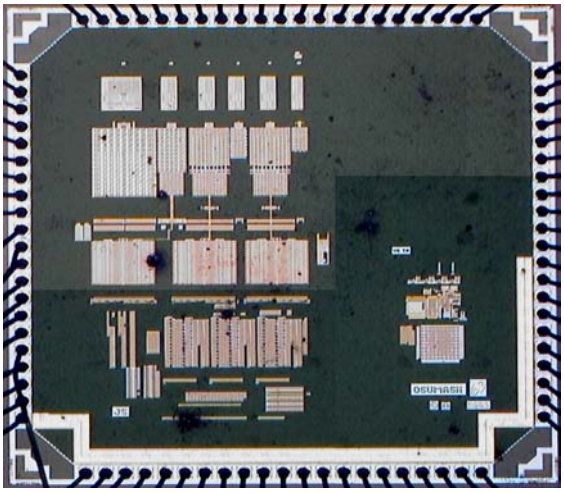


Figure 7.11 Entire chip

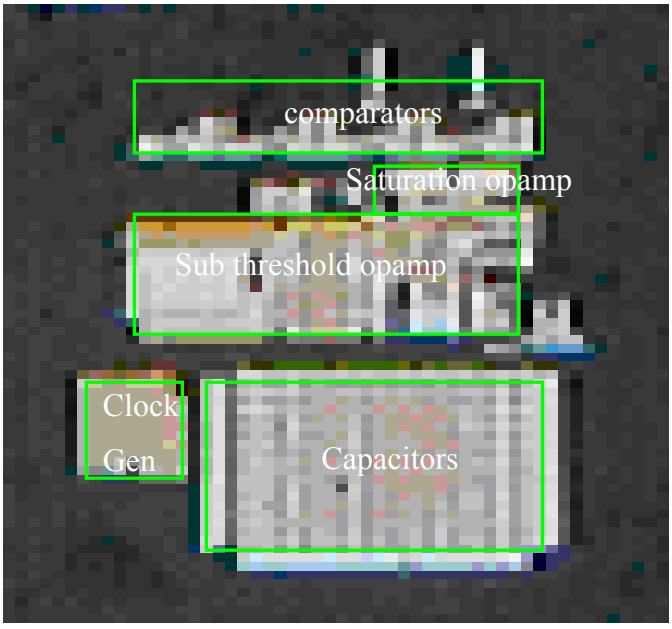


Figure 7.12 Algorithmic A/D converter

Chapter 8
Conclusions

The conclusions from this research are:

1. This thesis presented a novel algorithmic converter.
2. The converter is capable of 1.5 bits per phase, making it twice as fast as the existing converters.
3. An alternative approach by Nagaraj was used for comparing the proposed architecture with a the state-of-art.
4. The comparison was done with respect to non-idealities in the converter.
5. The proposed approach was found to be better with respect to power and area.
6. System-level simulations with some of the non-idealities gave the component specifications. The circuit design was done and some important circuit components were discussed

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