Low Power High Resolution Data Converter in Digital CMOS Technology

by

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A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed January 28, 1999
Commencement June 1999

ACKNOWLEDGEMENTS

I would like to express my most sincere gratitude to Prof. Gabor C. Temes. I have been very honored and privileged to have worked under his supervision and have benefited greatly from his deep intuition for circuits and systems. I wish to thank him for his guidance, patience, and support and for providing an excellent environment for research. Many thanks to Prof. Un-ku Moon. I appreciate his advice and encouragement and many enlightening technical discussions.

Special thanks to Prof. Michael E. Kassner for his support and encouragement on my concurrent degree study and research. Also thanks to Prof. Gordon M. Reistad, Prof. Timothy C. Kennedy, Prof. William Warnes, DyAnn McVicker, Debra A. Jimmerson and other ME department faculty for their support and encouragement.

Many thanks to Prof. Robert J. Schultz of Civil, Construction, & Environmental Engineering Department for taking time out of his busy schedule to serve as the Graduate Council Representative of my committee.

I would also like to thank my graduate committee members: Prof. Un-Ku Moon, Prof. John T. Stonick, Prof. Gabor C. Temes.

I would like to thank Prof. David J. Allstot for many inspiring discussions and comments on my ECE study and research. I would express my thanks to Prof. John T. Stonick for his wonderful communication classes.

Thanks to Rita Wells, Sarah O'Leary, Kim Rowe, Jodi Nickerson, Sharon Ortiz, Jennifer Heim, Otto Gygax, Andy Payne, Roger Traylor and other ECE department staff for their support and help.

Thanks to the National Science Foundation (NSF) Center for the Design of Analog/Digital ICs (CDADIC) and Catalyst Foundation for their generous support.

I would like to thank the people in our research group: Andreas Wiesbauer, Bo Wang, Emad Bidari, Jose Silva, Lei Wu, Min Shen, Mustafa Keskin, Peter Kiss, Tetsuya Kajita, Tao Sun, Xiangping Qiu for their friendship and useful technical discussions during the weekly meetings. I would like to acknowledge the help from Tao Shui and Haiqing Lin.

I would like in particular acknowledge Bo Wang and Yunteng Huang for their suggestions and advice, and patience with my questions; Lei Wu for share of his knowledge and many bright discussions; Jose Silva for tool support and many discussions, reviewing the report. Special thanks to Dwight Popline and Takao Inoue for their help on my start of ECE study.

Thanks to my Chinese friends and fellow Huibo Liu, Biao Shou, Ben Chen, Yun Ge, CSSA etc, with whom I shared wonderful time here.

Finally, I am grateful to my parents, my grandparents, my uncles, my brothers and my friends for their love and support throughout my life.

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Low Power High Resolution Data Converter in Digital CMOS Technology

Chapter 1. Introduction

This thesis discusses the current trend in integrated circuits, and the function of data converters. Some design techniques for implementing low power high resolution A/D converters are investigated, and the non-ideal effects of switched capacitor (SC) circuit for A/D converters are explored. Then two kinds of A/D converters are proposed. One is an error cancellation successive approximation A/D converter, the other is a ratio-independent cyclic A/D converter. Simulation results are presented to demonstrate the effectiveness of the above techniques.

1.1 Motivation

Analog-to-digital converters are key components for the modern signal processing and information systems. They perform the interface between the analog world and the powerful digital computers. The role of an analog interface in a VLSI digital system is clearly shown in Fig.1.1 [1]. An analog-to-digital converter performs three conceptually

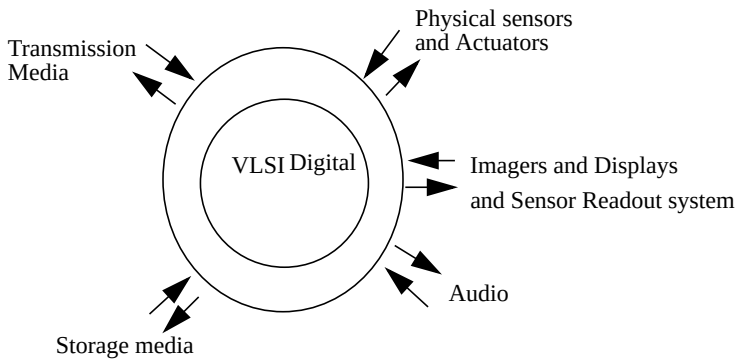


Figure 1.1: Role of analog interfaces in VLSI digital

distinct operations. First, it samples a continuous-valued, continuous-time signal; second, it quantizes the sampled signal to a number of levels; third, it assigns a code to the related quantized level [2].

With the increasing use of digital computing and signal processing, data converters have been extended to many applications such as medical imaging, instrumentation, consumer electronics, and communications. The data converter also follow the current trend of low-power portable design [3].

A SC circuit is a good solution for low-power high resolution design, but it has many non-ideal effects such as finite gain-bandwidth of the opamp, clock feed-through and charge injection of switches, and parasitic capacitance of capacitors. There are many existing techniques to compensate these effects, such as correlated-double-sampling (CDS), fully differential implementation, and predictive sampling. These techniques will be discussed and applied in the proposed A/D converters.

1.2 Thesis Organization

Chapter 2 studies the analog-to-digital converter architectures, especially the architectures suitable for low power application. An overview of correlated double sampling techniques and other techniques to compensate the non-ideal effects of SC circuits are also provided.

Chapter 3 deals with a new ratio independent multiply-by-two operation, which is achieved by differentially sampling instead of double sampling. The gain offset compensation and charge injection prevention techniques are also implemented in the proposed A/D converters.

Chapter 4 presents a new successive-approximation A/D converter with a new error cancellation and gain-offset compensation technique. Parasitic insensitive operation is also described. This A/D converter needs only one op-amp.

Chapter 5 summarizes the thesis work and plans for future work.

Chapter 2. Low Power Analog-to-Digital Converter Architectures

In this chapter, we will review several analog-to-digital converters that are suitable for low-power high-resolution applications. We will also give a general review of other kinds of A/D converter structures. Following this, the non-ideal effects of SC circuits, which are good low-power circuitry for A/D converters, are discussed.

2.1 Analog-to-Digital Converter Architectures

An analog-to-digital converter is a key part of an interface between the analog world and a digital system. It usually is also the bottleneck in data processing applications. We will investigate some A/D converter architectures commonly employed in low-power high-performance systems. We do not intend to cover all architectures.

2.1.1. Cyclic (Algorithmic) A/D Converter

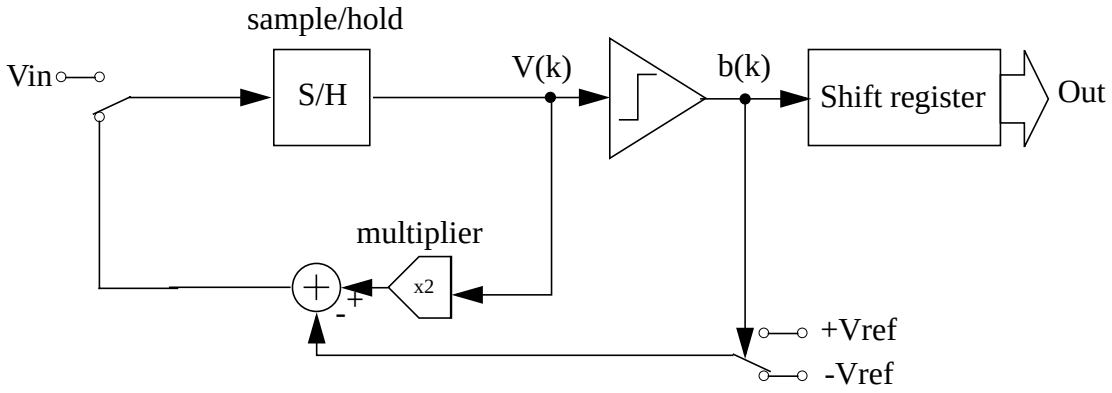


Figure 2.1: Cyclic A/D converter.

The cyclic analog-to-digital converter, also known as algorithmic or recirculating converter has been known and utilized in various forms [4][5]. A general block diagram is shown in Figure 2.1, which incorporates “digital corrections”, sometime it is called as “1.5

bit /stage" Converter. This structure needs only a small amount of circuitry since it uses the same function blocks repeatedly [6]. The above block diagram implements the algorithm:

$$V(1) = Vin \tag{2.1}$$

$$V(k+1) = 2V(k) + b(k) \bullet Vref \tag{2.2}$$

where

$$b(k) = -1 \quad \text{if} \quad V(k) \geq 0 \tag{2.3}$$

$$b(k) = 1 \quad \text{if} \quad V(k) < 0 \tag{2.4}$$

The operation of this converter is that at the first cycle it samples the input, which is considered an error voltage at the second cycle. During the following cycle, it doubles the remaining error voltage $V(k)$, and adds or subtracts a reference voltage $Vref$ depending on the comparator output $b(k)$ at the former conversion. Then it makes a decision on the new remaining error voltage.

2.1.2. Successive Approximation A/D Converter

Successive-approximation A/D converters are popular approaches for realizing A/D converters due to their reasonably quick conversion time, yet moderate circuit complexity [6]. Figure 2.2 illustrates a successive-approximation A/D converter. The converter consists of a sample-and-hold amplifier, a comparator, a D/A converter (DAC) and a digital control block, usually called a successive-approximation register. The converter operates according to

$$V(1) = Vref/2 \tag{2.5}$$

$$V(k+1) = V(k) - (-1)^{b_k} 2^{-(k+1)} Vref \tag{2.6}$$

where

$$b(k) = 1 \quad \text{if} \quad V(k) \geq Vin \tag{2.7}$$

$$b(k) = 0 \quad \text{if} \quad V(k) < Vin \tag{2.8}$$

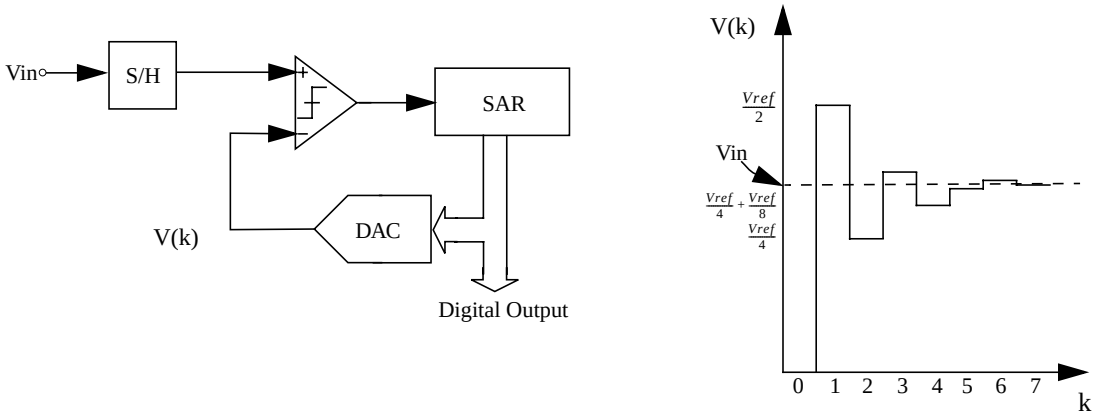


Figure 2.2: A general successive approximation A/D converter

Shown in the right part of Figure 2.2 is v(k) during a general conversion. First the DAC is set to the middle of Vref/2, then it compares with the sampled Vin. Then decision logic stores the comparator output in the MSB of the successive-approximation register. If $V(k) \geq Vin$ then $b(1) = 1$; otherwise, $b(1) = 0$. This way, the converter produces the MSB. During the following consecutive conversion, the DAC is set to the specific reference level according to Eq. (2.6), then the converter makes a decision on the corresponding bits until the LSB, the least significant bit, is reached. After the data converter gets all the bits for the current data, it samples another input and continues with the new conversion.

2.1.3. Other Data Converter Structure

Delta-sigma is also a good candidate for low-power high-resolution application. It is not focus of this thesis. We will not go into detail for the delta-sigma modulator. For further information, refer to [7][8].

There are many other types of A/D converters including flash, two-step, interpolating, folding, pipelined and interleaved architectures. Most of them can offer very high-speed conversion, but they are very power-hungry. Therefore, we will not consider them for low-power application. We will not discuss them in detail.

2.2 Design Techniques for Compensation of Component Imperfections in Switched-Capacitor Circuit

Switched capacitor circuits are widely used in high performance analog, mixed-mode IC system for their high accuracy [9]. But there are many component imperfections that degrade the performance of an SC circuit. One is noise effects that corrupt the signal. The most important ones includes thermal noise, op-amp 1/f noise, charge injection noise. These effects can not be removed, but can be minimized through careful design. There are also linear transfer function error effects such as finite op-amp gain, parasitic capacitance and capacitor mismatch. The third group is associated with the nonlinear behavior of components, which causes signal distortion. They include op-amp's nonlinear voltage transfer characteristics and slewing, and the capacitors' voltage dependence.

With today's ICS moving towards the direction of low power and low cost, low supply voltages are commonly used in mixed-mode IC systems. There exists a trade-off between dynamic range and power consumption. In SC circuits, signals are processed in the charge domain, which relies on accurate charge transfer. In this kind of application, an op-amp is often used to establish a virtual ground, whose voltage is forced to constant potential with very high input impedance. But the above mentioned non-ideal effects would degrade the virtual ground. This in turn affects the performance of the system. Several well-developed techniques will be reviewed here for the design of high-performance switched-capacitor circuits with high dynamic range and low power consumption.

2.2.1. The Basic Principle of CDS Techniques

The basic idea behind the correlated double sampling (CDS) is to sample the error quantity (noise, offset as well as finite-gain-induced signal at the opamp input node) first, then subtract it from the corrupted signal at the opamp input or output [10].

The concept of CDS will be shown in Figure 2.3 through an offset-compensated comparator. Assuming that the opamp has infinite gain, the op-amp input referred noise and offset is denoted as v_n. When ϕ_1 is high, the capacitor C is charged to the voltage v_n, and this value is then subtracted from the input voltage v_{in} when ϕ_2 goes high. A simple analysis shows that the output is related to v_n by

$$V_{out}(z) = (1 - z^{-1}) \cdot V_n(z) \tag{2.9}$$

the corresponding transfer function in the frequency domain is given by

$$|H_n| = 2 \cdot \left| \sin\left(\frac{\omega T}{2}\right) \right|. \tag{2.10}$$

This is a high-pass function which suppresses the low-frequency component of v_n such as dc offset voltage and much of the input-referred 1/f noise. Note that thermal noise is wide-band, its noise power is not reduced but increased in the baseband due to aliasing.

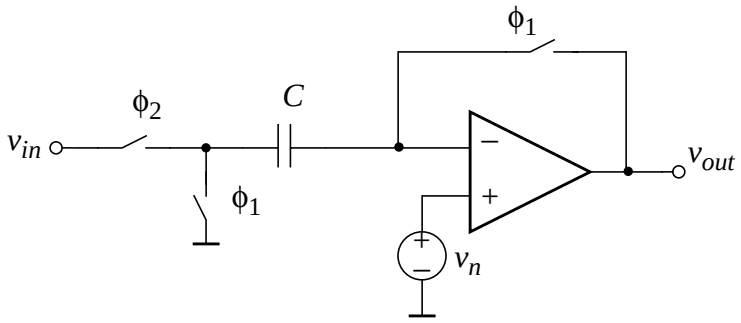


Figure 2.3: A simple offset-compensated comparator

The above technique is called correlated double sampling (CDS), since it cancels the low-frequency error signal by sampling twice and producing the difference of the correlated samples. Further discussion will focus on the offset compensation, gain and offset compensation (GOC), and predictive GOC compensation.

2.2.2. Offset-Compensation CDS Techniques

To show the effect of CDS, a uncompensated SC voltage amplifier will be shown in Figure 2.4 and discussed briefly here [11]. The ideal output is $v_{out} = -(C_1/C_2)v_{in}$. Taking the finite gain and offset into account, the actual output is

$$v_{out} = \frac{G_{ideal}}{1 + (1 + C_1/C_2)/A} \cdot v_{in} + (1 + G_{ideal}) \cdot v_{os}, \qquad (2.11)$$

where G_{ideal} is the ideal gain $-C_1/C_2$. For a typical situation, a gain error of 1% and an output dc offset of 100 mV may occur. This may be unacceptable in a high-performance application such as a data converter; also the offset would be a big challenge to the small allowed signal swing, especially in low-voltage low-power application.

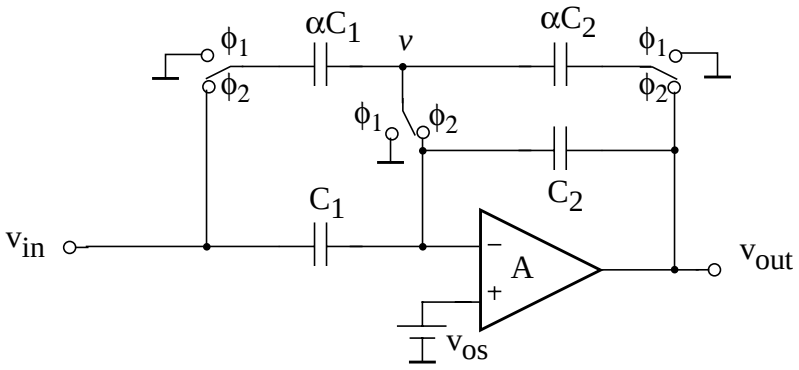
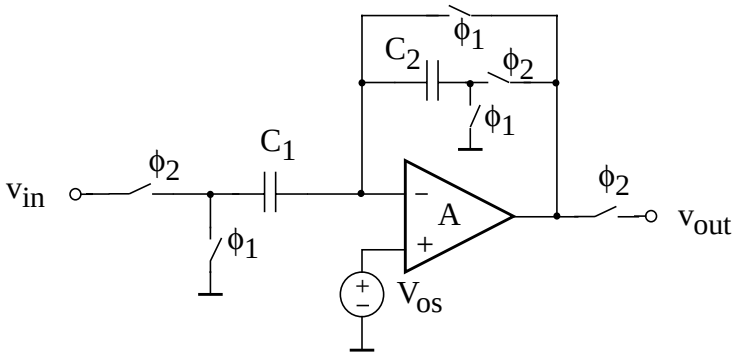


Figure 2.4: An uncompensated SC voltage amplifier

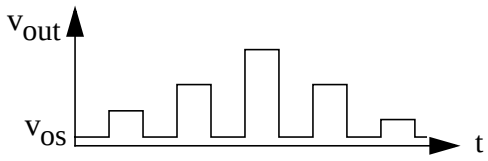
The solution is to use the CDS technique in a simple offset-compensated amplifier as shown in Figure 2.5 [12]. The output of this amplifier is

$$v_{out} = \frac{-C_1/C_2}{1+(1+C_1/C_2)/A} \cdot v_{in} + v_{os} \cdot \frac{(1+C_1/C_2)}{A} \qquad (2.12)$$

Clearly, the offset of the opamp and its input referred 1/f noise is reduced by the op-amp open loop gain. But further analysis, as shown in Figure 2.7 (b), shows that the opamp output is reset to V_{os} when ϕ_1 is high, thus the opamp must have a high slew rate. Also the stage gain is still affected by the finite dc gain of opamp.



(a) The SC amplifier with offset compensation



(b) Output waveform for the SC amplifier

Figure 2.5: A SC amplifier with offset compensation.

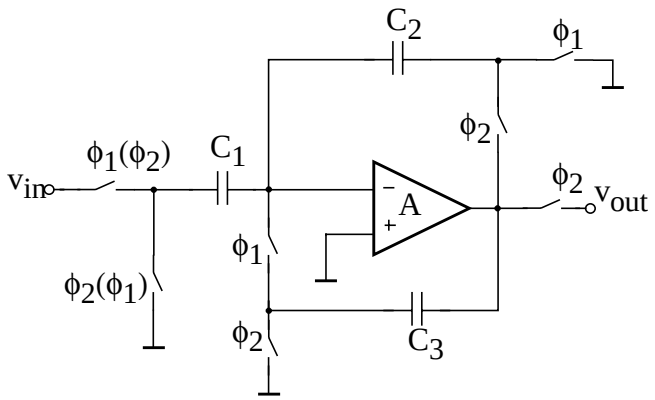
2.2.3. Gain and Offset Compensation CDS Technique

An SC amplifier with narrow-band gain and offset compensation is shown in Figure 2.6(a) [13]. In this structure, the holding capacitor with two switches replaces the feedback reset switch in Figure 2.5(a). Assume that the circuit uses the clock phase outside of the parentheses. Then, when ϕ_2 is high, C_1 discharges into C_2, and produces the valid output. At the same time, C_3 samples the output. When ϕ_1 goes high again, C_3 becomes the feedback capacitor and hold the output amplifier, C_1 samples the input, and C_2 discharges. In a practical SC circuit application, the signal bandwidth is much smaller than fs/2, i.e. the signal is highly oversampled, so v_{out} doesn't vary much between two succeeding phases. Thus the samples of the induced error signal $-v_{out}/A$ at the virtual ground are very correlated, therefore cancelled by C_1 and C_2 with the CDS scheme.

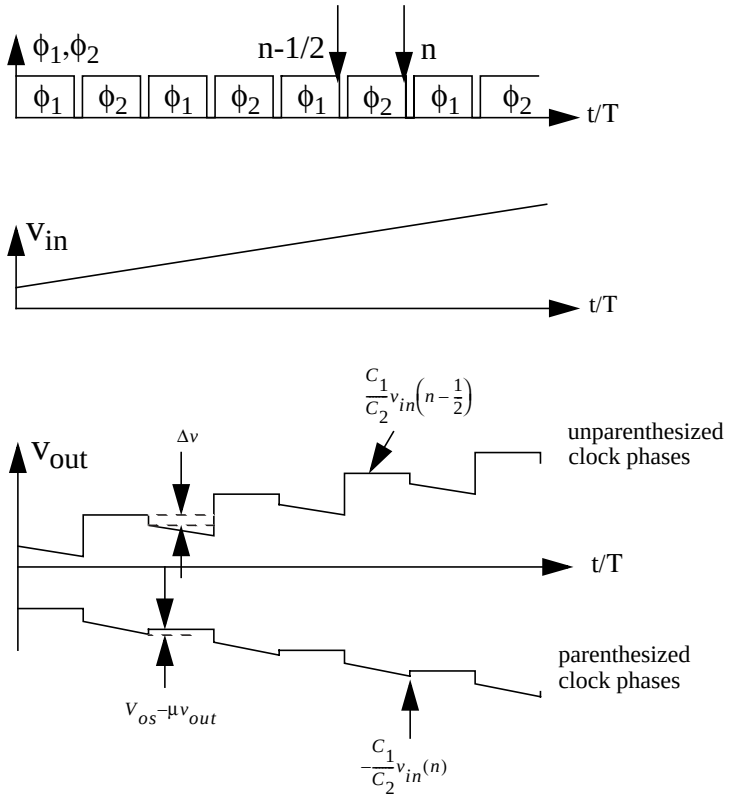
Figure 2.6 (b) shows the clock phases and waveforms of the amplifier. When ϕ_1 goes high and enters the reset period, there is a small step $\Delta v = V_{os} - \mu v_{out} - (C_1/C_3)\Delta v_{in}$ in the output voltage, where Δv_{in} is the change in v_{in} while ϕ_2 is high. Here $\mu \equiv 1/A$. This structure doesn't require a fast settling or a high slew rate from the opamp since the step is very small, usually on the order of a few mV. The dc output offset is just $\mu\,(1+C_1/C_2)\,V_{os}$.

Detailed analysis [13] shows that the gain is insensitive to the frequency response of the opamp since the CDS has the virtue of high-pass effect. The dc gain is

$$H(z)_{z=1} = \frac{-C_1/C_2}{1 + (1 + C_1/C_2)\mu^2} \quad . \tag{2.13}$$



(a) The compensated SC amplifier



(b) Clock and signal waveforms

Figure 2.6: A SC amplifier with narrow-band offset and gain compensation.

2.2.4. Predictive CDS Technique

The above CDS is very effective in compensating a slowly-varying error signal such as input-referred 1/f noise, opamp offset and finite opamp gain. However, when the input signal frequency is high, the input induced signal will vary rapidly. The CDS must predict the fast-changing input signal, so prediction will be incorporated with the CDS technique. Some predictive CDS techniques will be discussed here.

A wide-band gain- and offset-compensated SC amplifier is shown in Figure 2.7. This circuit consists of two signal paths. One is the prediction path with C_A and C_B, which predicts the output voltage and stores the error voltage in C_1 during ϕ_2; the other is the main signal path with C_1 and C_2, which amplifies v_{in} and subtracts the error voltage held by C_1. Thus it generates the accurate amplifier output during ϕ_1 [14]. Typical input and output waveforms are shown in the Figure 2.7(b). The exact analysis shows that

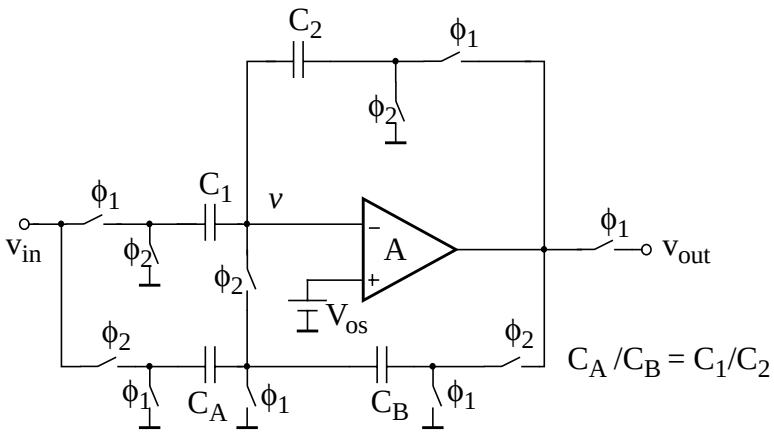
$$v_{out} \approx \frac{-C_1/C_2}{1+(1+C_1/C_2)^2/A^2} \cdot v_{in}(n) + V_{os} \cdot \frac{(1+C_1/C_2)}{A}. \qquad (2.14)$$

But this structure is less effective in suppressing the finite gain compared to the circuit in Figure 2.6, since it has another factor of $1+C_1/C_2$ in the denominator.

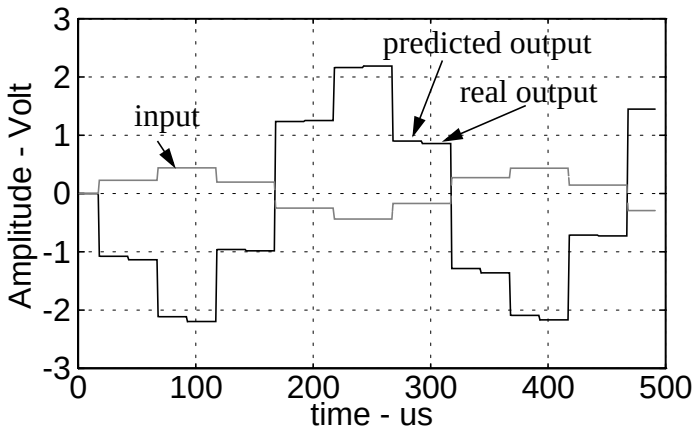
An improved SC amplifier is shown in Figure 2.8 [15]. The only difference is that three of the switches in the prediction path have been omitted. Its operation is similar to that of Figure 2.7, but the performance is much improved, which is shown clearly in Figure 2.10.

An error storage capacitor can be used in the gain amplifier to achieve gain- and offset- compensation as shown in Figure 2.9 [16]. When ϕ_2 is high, the predictive path predicts the opamp output. Meanwhile, C_I samples the error voltage of ($-V_{out}/A+V_{os}$).

Then, when ϕ_1 goes high, the left plate of capacitor C_I provides an error-free virtual ground and the main signal path generates the valid output voltage. The performance of this circuit is similar to that in Figure 2.7. This circuit will be used in the data converter design in the following Chapter.



(a) The compensated SC amplifier.



(b) Input and output signal waveforms.

Figure 2.7: A wide-band predictive GOC SC amplifier.

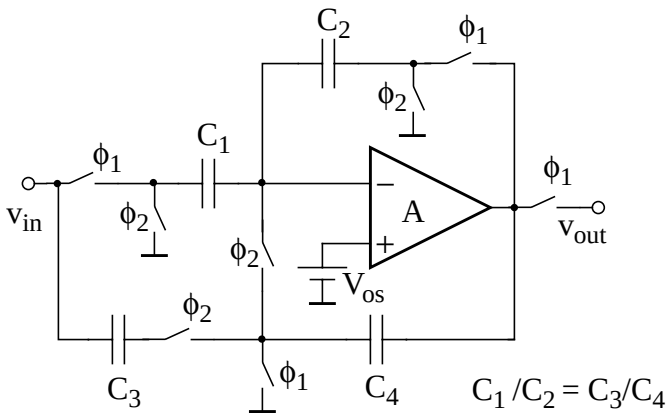


Figure 2.8: An improved predictive SC amplifiers.

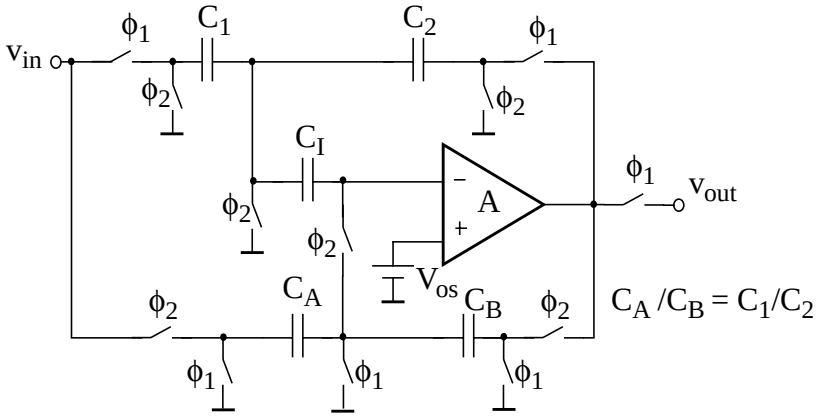


Figure 2.9: A compensated SC amplifier using a storage capacitor.

Gain errors frequency responses for the SC amplifiers presented in this session are shown in Figure 2.10 [17]. In the simulation, the ideal gain is 5, and the finite opamp gain is 40 dB. The gain of the SC amplifier can be expressed as $G_{prac} \cong -G_{ideal}(1-e)$, where e is the gain error. Under DC condition, for the uncompensated gain stage in Figure 2.4, the gain error is $e \cong (1 + G_{ideal})/A$; for the narrow-band CDS circuit of Figure 2.6, the gain error is just $(1 + G_{ideal})/A^2$, which is very small; the wide-band CDS technique in Figure 2.7 and Figure 2.9 has error of $(1 + G_{ideal})^2/A^2$, which also holds for the improved CDS structure in Figure 2.8. From Figure 2.10, we find that the narrow-band CDS is very effective in suppressing low-frequency error, while the wide-band CDS achieves reasonable gain error in all the frequency range, and the improved version attains the best overall performance.

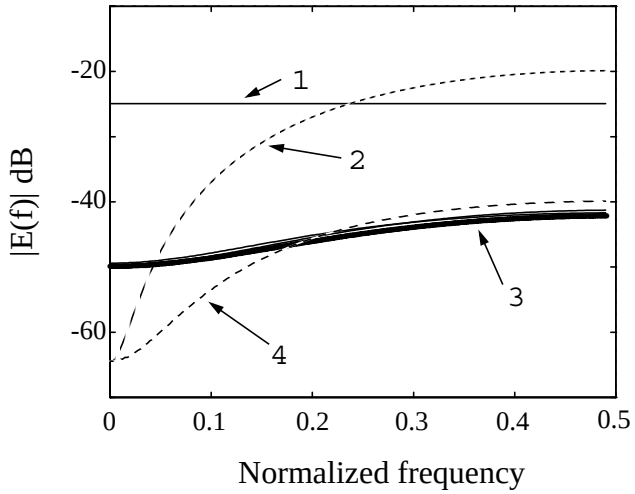


Figure 2.10:Gain errors versus signal frequency for the SC amplifiers.

2.3 Conclusions

Several data converter structures have been discussed in this Chapter. They are simple, and use the same functional blocks. They can achieve high performance with very low power consumption.

A variety of CDS techniques was reviewed here for compensating the nonideal effects of opamps such as input-referred noise, offset, finite opamp gain. They can improve the performance of the system very much. They will be incorporated into the data converter presented in the following Chapter.

Chapter 3. A New Ratio-Independent Cyclic A/D Converter

This chapter describes the design and implementation of a cyclic A/D converter with a new ratio-independent scheme. In the switched-capacitor circuit, the resolution of the data converter is usually limited by non-ideal effects such as gain error, offset, capacitance inaccuracy and charge injection [11]. Capacitance inaccuracy is a dominant non-ideal effect that limits the resolution of ADC's to about 10 bits, if no error cancellation is used. Laser trimming, self-calibration, and error averaging have been developed to overcome these errors [4][18]. They either need special processing at an increase the cost, or need complicated digital circuitry, which increases the die area and needs more power consumption. Reference refreshing and ratio independent techniques can make the error independent of capacitor mismatch, but they still need high dc gain for the amplifier, which can be impractical, especially in a low-power, low-voltage application [4][20]. A ratio-independent and gain-insensitive algorithmic ADC that combines the gain-offset compensation and ratio-independent scheme has been used to reduce the requirements of the opamp and eliminate the capacitance mismatch. The dc gain requirement of the opamp has been reduced from $(6n + 16)$ dB to $(3n + 6)$ dB for a n-bit resolution ADC at the cost of 7 clock phases to complete one conversion [21].

In contrast to the conventional ratio independent scheme, which is implemented by double sampling, we propose a new multiply-by-two scheme using differential sampling, to overcome the capacitor mismatch effects. A cyclic A/D converter is designed to implement the above scheme. Gain-offset compensation is included to reduce the dc gain requirement of op-amp. Therefore, the power consumption is significantly reduced. We also use design techniques to prevent other non-ideal effects such as parasitic capacitances and charge injection, which will be described in detail in the next Chapter.

In this Chapter, a ratio-independent scheme is discussed. Techniques to compensate other non-ideal effects are exploited. Then, a 16 bit resolution cyclic ADC is designed and simulated in SWITCAP.

3.1 Cyclic A/D Converter Operation Principle

We have discussed the structure of a cyclic ADC in chapter 2. We repeat some of the discussion here again for convenience. A general block diagram of a 1.5-bit per stage cyclic ADC, which incorporates digital error correction, is shown in Figure 3.1

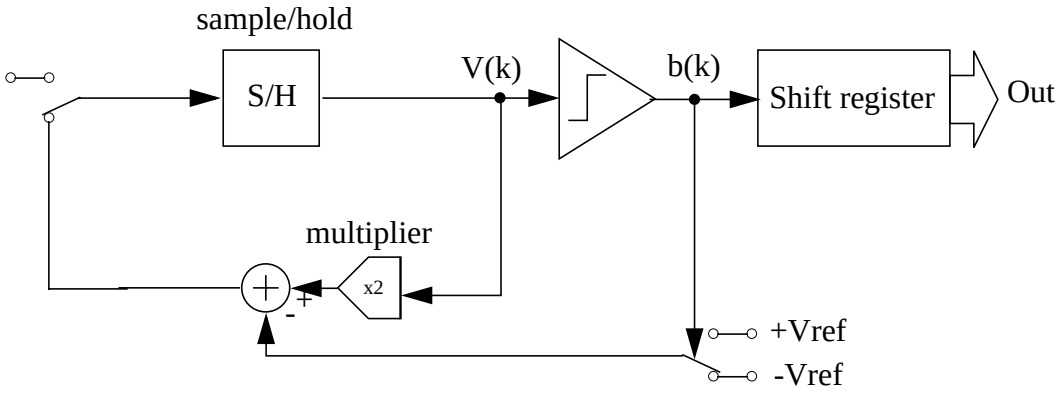


Figure 3.1: A cyclic A/D converter

The switched capacitor implementation of Figure 3.1 will be subject to the following non-ideal effects [21]-[23]:

1 - Capacitor mismatch
2 - Finite-gain error and offset of opamp
3 - Parasitic capacitance
4 - Charge injection and clock feedthrough by switches

In the following section, we will discuss how to eliminate or reduce these effects.

3.2 Ratio-Independent Multiply-by-Two to Compensate Mismatch

3.2.1. A Conventional Ratio-Independent Multiply-by-Two Using Double Sampling

The algorithmic converter doubles the error voltage while leaving the reference unchanged. A high-precision algorithmic converter will be constrained by the accuracy of the multiply-by-two gain amp. Fortunately, we can sample the input signal twice using the same capacitor. This is the conventional ratio-independent multiply-by-two implemented by the double sampling technique. The operation is shown in Figure 3.2 [19].

i) Initial condition: Begins at the end of Step 3 of last conversion.

Assume that we have $V(i)$ on C_1. C_2 discharges, C_3 samples $V(i)$.

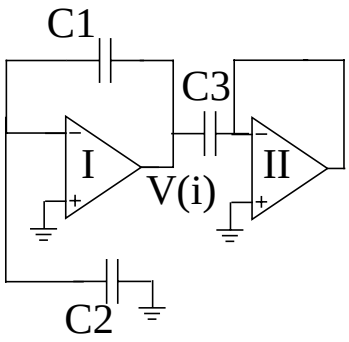
ii) Step 1: C_1 transfers $q1 = C1 \bullet V(i)$ into C_2, C_3 holds $V(i)$.

iii) Step 2: C_1 samples $V(i)$ held by stage II, gets the charge $q2 = C1 \bullet V(i)$

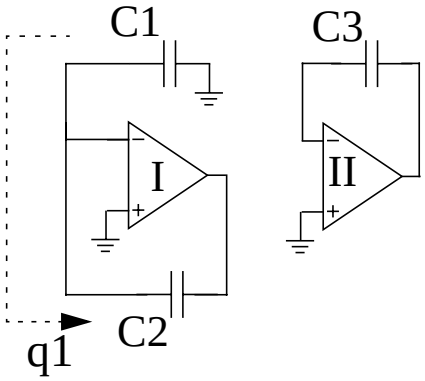
iv) Step 3: C_2 discharges the stored $q1 = C1 \bullet V(i)$. Thus C_1 has a total charge $q = q1 + q2 = C1 \bullet V(i) + C1 \bullet V(i) = 2C1 \bullet V(i)$, hence, the voltage on C_1 is $V(i+1) = 2 \bullet V(i)$.

Note that the reason why the operation is independent of capacitor mismatch is that the signal is sampled twice by the same capacitor; the conversion between charge and voltage is always performed by the same capacitor C_1. The conversion is not affected by C_2 since C_2 is only a charge-storage capacitor.

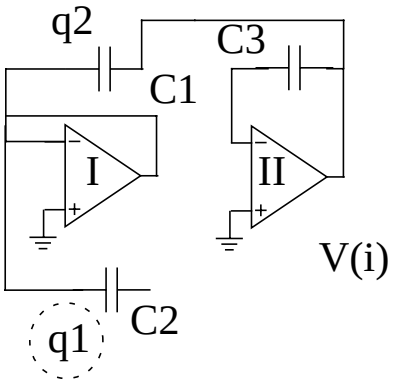
(i) Initial (former step 3)



(ii) Step 1



(iii) Step 2



(iv) Step 3

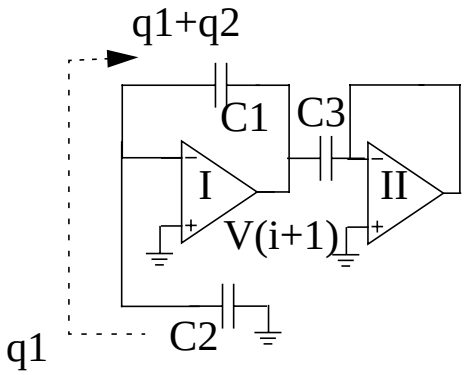


Figure 3.2: A conventional ratio-independent multiply-by-two using double sampling

3.2.2. A new Ratio-Independent Multiply-by-Two Using Differential Sampling (in Single-Ended Structure).

Most high-precision SC circuits are implemented in a fully differential structure, with two complementary signals, which are equal in amplitude, opposite in sign. Based on this assumption, another ratio-independent multiply-by-two scheme, using differential sampling, is proposed.

For simplicity, this scheme will be described for a single-ended structure first. Note that, as shown in Figure 3.3, the circuit requires an inverter that is not needed for differential operation. Ratio-independent operation is as follows.

i) Initial condition: Begins with the end of Step 3 of the last conversion.

   Assume that we have $V(i)$ on C_1. C_2 discharges, C_3 samples $V(i)$.

ii) Step 1: In stage II, C_3 holds $V(i)$, inverter provides $-V(i)$.

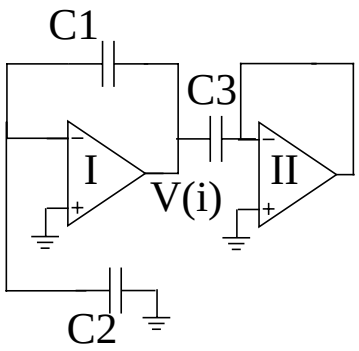
   In stage I, C_1 switches its right plate from the output of opamp I to the inverter output, which is at $-V(i)$. Thus C_1 charges from $V(i)$ to $-V(i)$, and the differential charge $q = C1 \bullet [V(i) - (-V(i))] = 2C1 \bullet V(i)$ flows from C_1 to C_2.

iii) Step 2: C_1 discharges, C_2 stores the charge q.

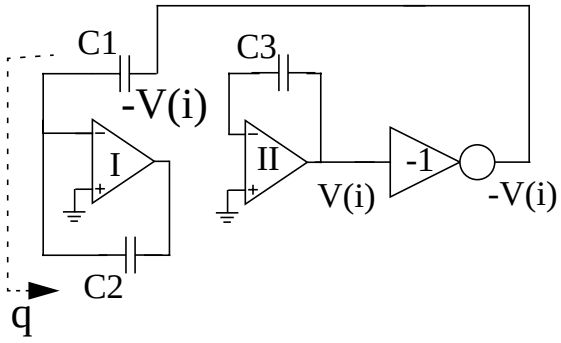
iv) Step 3: C_2 returns the charge $q = 2C1 \bullet V(i)$ to C_1. Hence the voltage on C_1 is $V(i+1) = 2 \bullet V(i)$.

This scheme is independent of any capacitor mismatch for the same reasons as described for the previous structure.

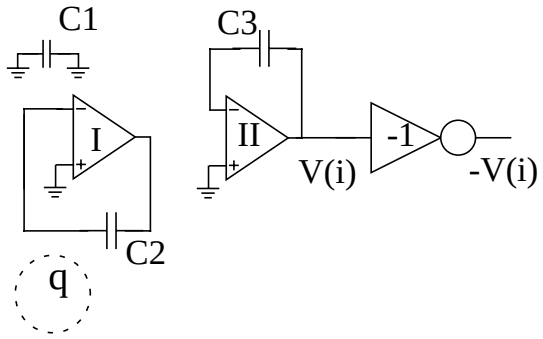
(i) Initial (former step 3)



(ii) Step 1



(iii) Step 2



(iv) Step 3

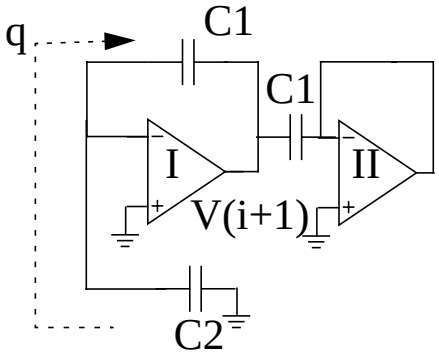


Figure 3.3: A new ratio-independent multiply-by-two using differential sampling (in single-ended structure)

It is straightforward to implement Figure 3.3 in a fully differential structure as shown in Figure 3.4, which makes the voltage inversion used in the single-ended circuit unnecessary. The operation of Figure 3.4 is the same as that of Figure 3.3, except that we take $-V(i)$ from the inverting terminal of the fully differential structure, instead of the output of the inverter. The same result as for the single-ended version, $V(i+1) = 2 \bullet V(i)$, holds for the circuit of Figure 3.4. Including the DAC output, $\pm Vref$, which is decided by the output sign of comparator, we get

$$V(i+1) = 2 \bullet V(i) \pm \frac{1}{2} \bullet \left(\frac{C41}{C11} + \frac{C42}{C12} \right) \bullet Vref \qquad (3.1)$$

The $\frac{1}{2} \bullet \left(\frac{C41}{C11} + \frac{C42}{C12} \right) \approx 1$ term only causes a gain error for the entire A/D conversion, but it doesn't cause any harmonic distortion. We will find that this gain error is compensated during the sampling process of Vin.

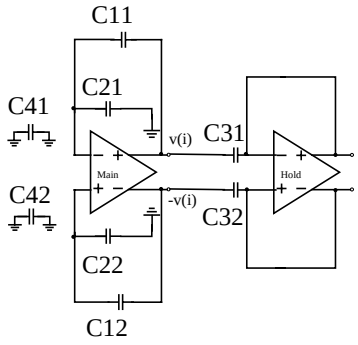
A similar configuration can be used to achieve the function of sample and hold as shown in Figure 3.5. Compared with Figure 3.4, C_{41} and C_{42} samples Vin instead of digitized output $\pm Vref$; C_{11} and C_{12} are open and do nothing instead of sampling the former error voltage $V(i)$. Thus, compared with the transfer function (3.1) for Figure 3.4, we can write a similar voltage transfer function for Figure 3.5:

$$V(1) = \frac{1}{2} \bullet \left(\frac{C41}{C11} + \frac{C42}{C12} \right) \bullet Vin \approx Vin \qquad (3.2)$$

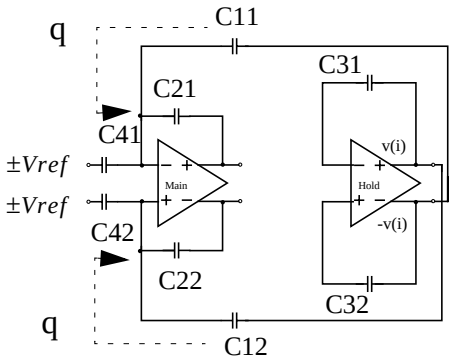
As expected, since the circuit of Figure 3.5 uses the same caps as Figure 3.4, the gain error of Equation (3.2) cancels the gain error of Equation (3.1) exactly. Both Vin and $\pm Vref$ has the same gain error when they enter ADC system, there is not any other gain error once they are sampled into ADC, we can get the absolute value of Vin at the end of conversion. This converter has thus the property of absolute accuracy, which is very important in some specific applications such as instrument measurement.

The ratio-independent multiply-by-two attains multiply-by-two scheme uses only one capacitor to double $V(i)$. It is independent of any capacitor ratio, thus this scheme is not limited by the accuracy of capacitor. In other words, it is insensitive to capacitor mismatch if the circuit operates correctly.

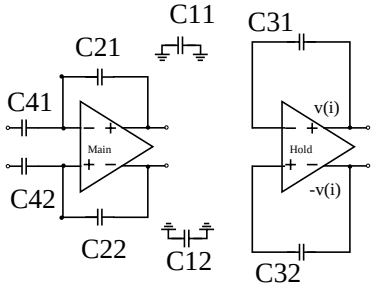
(i) Initial (former step 3)



(ii) Step 1



(iii) Step 2



(iv) Step 3

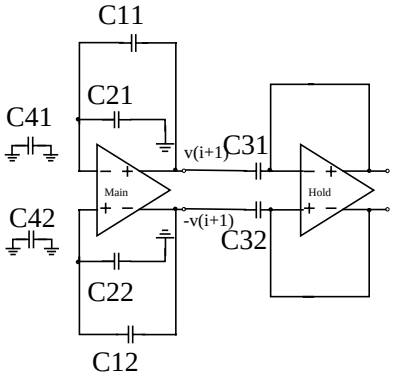
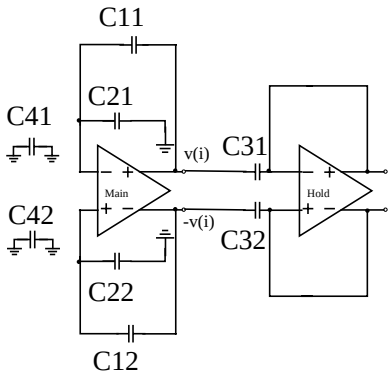
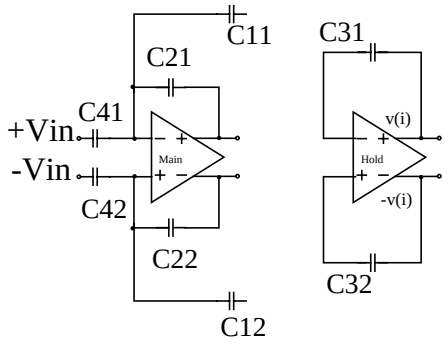


Figure 3.4: A new ratio-independent multiply-by-two using differential sampling (multiply-by-two in fully-differential structure)

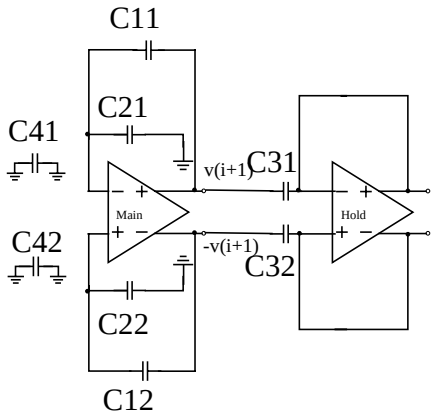
(i) Initial state (former Step 3)



(ii) Step 1



(iii) Step 2



(iv) Step 3 (Get the Vin)

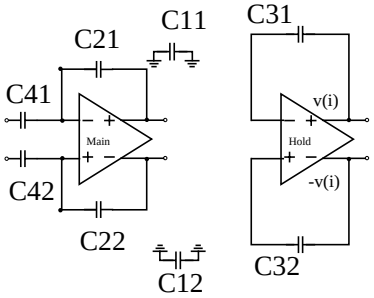


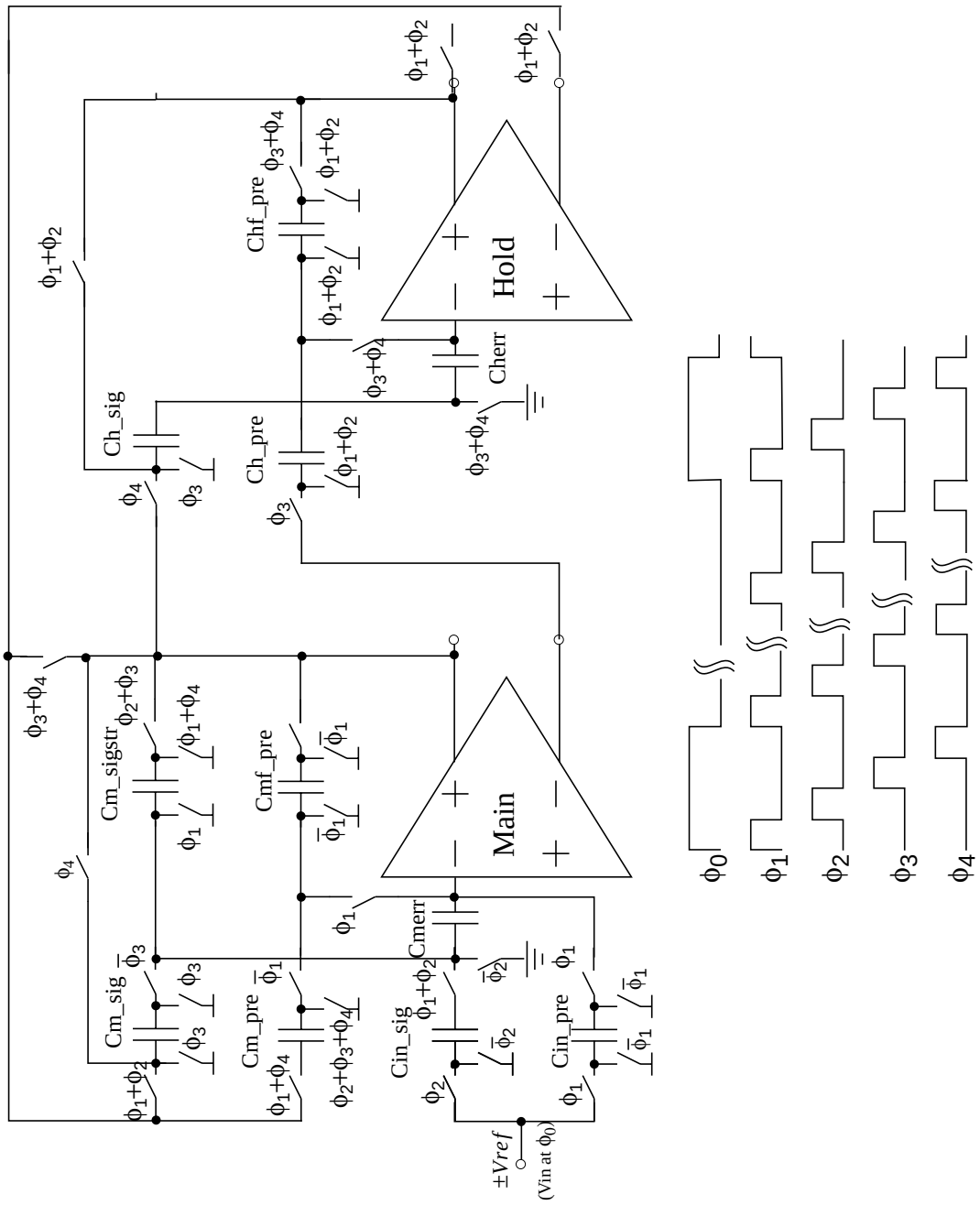
Figure 3.5: A new ratio-independent multiply-by-two scheme using differential sampling (sample and hold in fully-differential structure)

Using double sampling, it takes 3n cycles to implement ratio-independent cyclic A/D without gain-offset compensation[19], but it takes 7n cycles to implement GOC, ratio independent cyclic A/D [21]. In contrast to double sampling, the differential sampling allows us to implement it with the gain-offset compensation technique, which can reduce the dc gain requirement of the opamp, with only 4n clock cycles. We will discuss its application in an A/D in the next session.

3.3 A GOC, Ratio-Independent ADC Using Differential Sampling

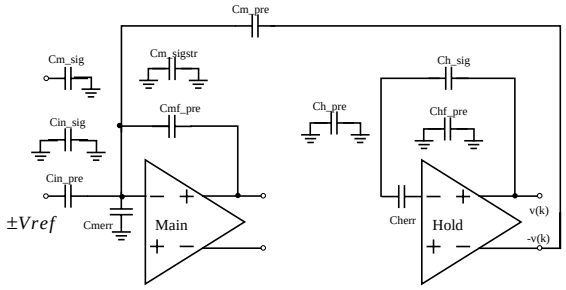
As mentioned before, there are many non-ideal effects in SC circuits. We have discussed and dealt with the main ones, capacitor mismatch and gain requirement. Other non-ideal effects will be discussed in the next chapter. The parasitic capacitance effect can be prevented by never charging or never discharging them [11], critical node isolation, critical node pre-charge or pre-discharge. The charge injection effects can be reduced by using differential structure, delayed clock phases, and dummy switches.

Based on the circuit of Figure 3.4, an extra duplicate path is needed to achieve the gain-offset compensation. Combining the above techniques, a gain-offset insensitive, ratio-independent ADC with fully differential structure is proposed as shown in Figure 3.6. Only one side of the fully differential structure is shown here for clarity. The corresponding multiply-by-two and sample-and-hold operations are shown in Figure 3.7 and Figure 3.8 respectively. The analysis is similar to Figure 3.4 and Figure 3.5 except that we use gain-offset compensation to attain a high quality virtual ground, and thus reduce the dc gain requirement of the opamp, and repress the 1/f noise and offset of the opamp. A straightforward analysis shows that the opamp gain error has been reduced from 1/A to $1/A^2$, thus the power consumption of the opamp can be greatly reduced.

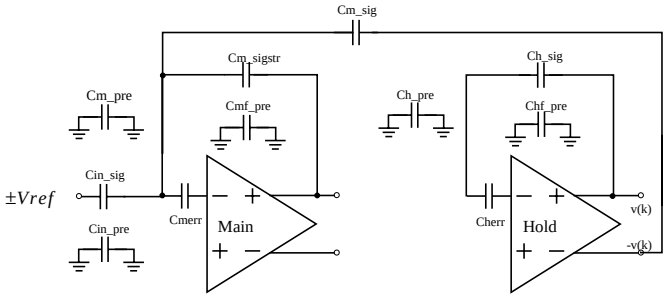


'igure 3.6: The circuit diagram of the gain-offset compensated, ratio-independent cyclic ADC

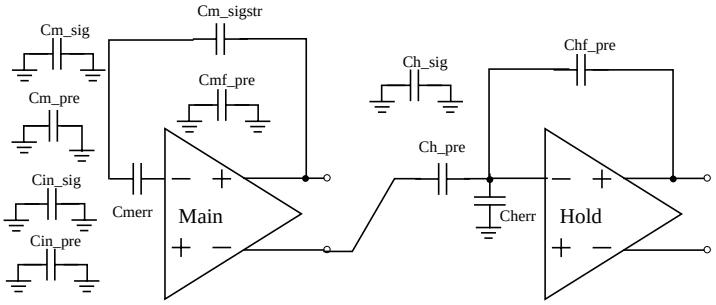
(i) ϕ_1 Predict $2v(k)\pm Vref$



(ii) ϕ_2 Store $2v(k)\pm Vref$



(iii) ϕ_3 Hold $2v(k)\pm Vref$



(iv) ϕ_4 Get $v(k+1) = 2v(k)\pm Vref$

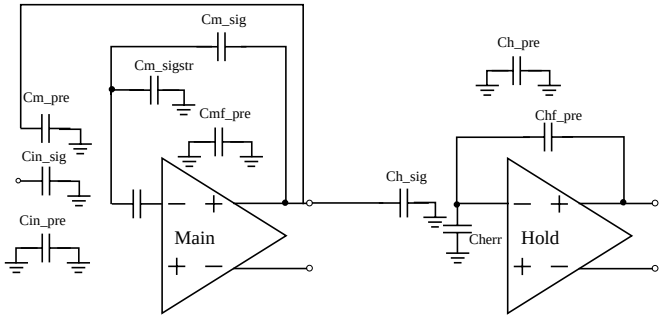
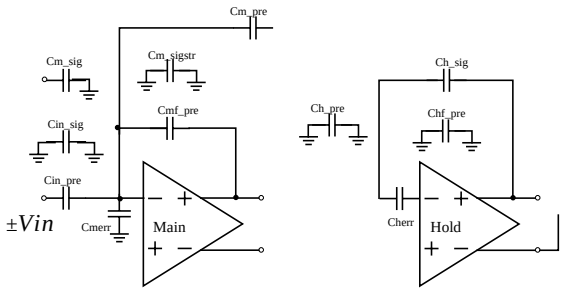
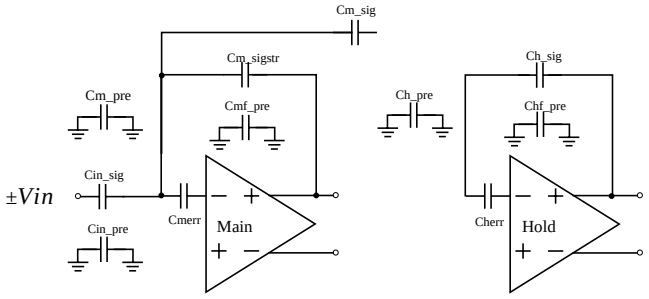


Figure 3.7: Multiply-by-two stage in a GOC, ratio-independent ADC

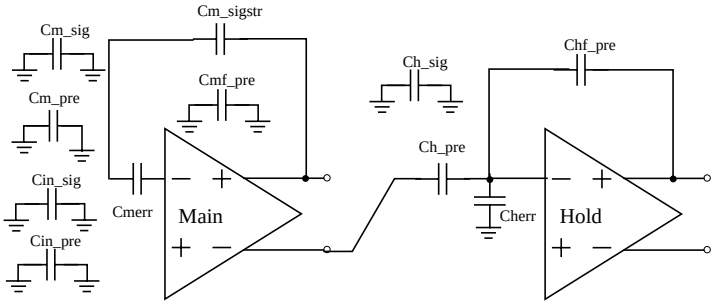
(i) ϕ_1 Predict *Vin*



(ii) ϕ_2 Store *Vin*



(iii) ϕ_3 Hold *Vin*



(iv) ϕ_4 Get *Vin*

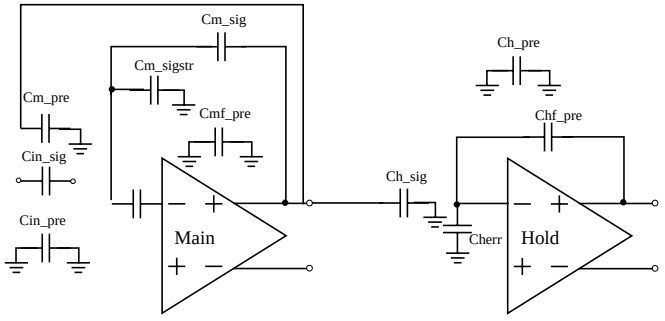


Figure 3.8: Sample and hold stage in a GOC ratio-independent ADC

3.4 Simulation Results for the GOC, Ratio-Independent Cyclic A/D Converter

To verify the validity of the previous discussions and functionality of the circuit realization, the SC circuits were simulated extensively in SWITCAP2, a SC circuit analysis program which uses simplified models for switches and capacitors.

The dc gain of the opamp is 66 dB and the offset of the opamp is 20mV.

The nominal capacitor value is 2pF. The capacitors of the SC circuit are assigned by a Gaussian function generator $C = 2 + 2 \bullet 0.01 \bullet randn(11, 1)$, that gave[2.0097, 1.9881, 1.997, 1.9913, 1.9984, 2.0307, 1.9879] for the capacitors in Figure 3.6. The variance of the Gaussian function generator is 1% of the nominal value, which results in a 3% mismatch between maximum and minimum capacitor. The capacitors for the other side of the fully differential structure are [1.9874, 2.0107, 2.0111, 1.9959, 1.9589, 2.0027, 2.00319].

The parasitic capacitance for each node in the SC circuit is also assigned by the Gaussian function generator $C = 2 \bullet 0.1 \bullet randn(52, 1)$ with a variance of 10%, and mean value of 0.2pF. These values are pessimistic compared with the actual situation. In the clock feedthrough model, the gate-source capacitance *Cgs* and gain-drain capacitances *Cgd* were about 1.5% of the nominal value; *Csb, Csd* were 2.5% of the nominal value.

Under the above assumption, the simulation result is shown in Figure 3.9. It gives after compensation

SDNRin=101.88 dB,
SDNRout=87.2 dB,
HD=-111.10 dB
Dominant harmonic: third

Without compensation

After compensation

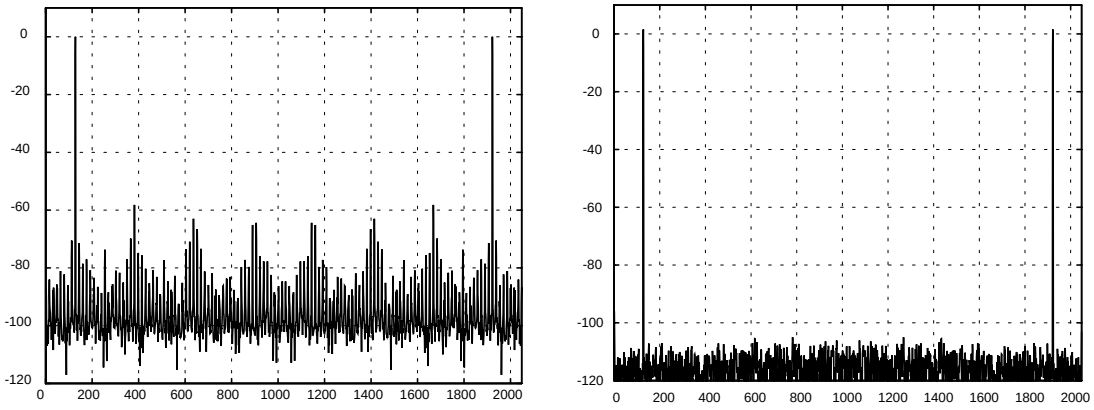


Figure 3.9: Output spectrum of ADC

The simulation results with different capacitor mismatch ratios are shown in Table 3.1.This shows that the proposed ADC is a ratio-independent A/D converter since capacitor mismatch doesn't affect the performance

.

Table 3.1: The simulation result with different mismatch ratio

Mismatch (Standard deviation)	± 0.1%	± 0.5%
SNR_input source	101.8 dB	
SNR adc output	97.4	97.7
Maximum HD	-112.8 dB	-112.8 dB
Dominant harmonic	3rd	3rd

The simulation results with different values of parasitic capacitances are shown in Table 3.2. We can see that the proposed ADC effectively reduces the effects of parasitic capacitance.

Table 3.2: The simulation result with different parasitic capacitance

Parasitic Capacitance	1% of nominal value	10% of nominal value
SNR_input source	101.8 dB	
SNR adc output	97.4	87.2
maximum HD	-111.8 dB	-104.8 dB
Dominant harmonic	3rd	3rd

3.5 Conclusions

By utilizing a gain-offset compensated, ratio-independent multiply-by-two stage with correlated double sampling, fully differential structure and other techniques briefly discussed above, a cyclic A/D converter can achieve very high resolution with relatively low dc gain requirement for the opamp, and attain insensitivity to capacitor mismatch and other non-ideal effects. Because the proposed A/D converter structure is simple, it is good candidate for low-power high accuracy application.

Chapter 4. Capacitor Mismatch Error Cancellation Technique for a Successive-Approximation A/D Converter

An error cancellation technique is described for suppressing capacitor mismatches in a successive approximation A/D converter. At the cost of a 50% increase in the conversion time, the first-order capacitor mismatch error is cancelled. Methods for realizing gain- and offset-compensated opamps are explained. With all schemes incorporated into a SWITCAP simulation, a 16-bit SAR ADC achieved an SNDR of 82.6 dB under non-ideal conditions including a 0.5% nominal capacitor mismatch, 10% randomized parasitic capacitors, 66 dB opamp gain, and 30 mV opamp offset.

4.1 Introduction and Background

Switched-capacitor data converters commonly suffer from the finite matching accuracy of their analog integrated capacitors. Because of this unavoidable physical limit, a variety of techniques have been proposed to minimize this problem. The most recent among them are mismatch-shaping techniques [24]-[27]. However, a recent work by Rombouts and Weyten [28] proposed a technique to essentially eliminate the capacitor mismatch error (first-order cancellation). A nearly distortion-free converter is obtained by employing additional signal processing.

In this chapter, another capacitor mismatch error cancellation is proposed in the context of a successive-approximation ADC. In the proposed technique, the first-order error is cancelled at the cost of a 50% increase in the conversion time, instead of the two-fold increase described in [28]. In the context of a SAR ADC, the N clock cycles nominally required for an N-bit converter are increased to 1.5 N clock cycles. In the example to be presented, 24 cycles are required for a 16-bit SAR ADC.

Parasitic capacitances can deteriorate the performance of a system. The never charge or discharge stray insensitive scheme has been widely used to eliminate this effect [11]. But it is not practical due to unavoidable changes in the node potential in some specific applications. Self calibration was also used to reduce the effect of parasitic capacitance with an N-bit binary-weighted capacitor array [29]. It needs complex control logic and one extra DAC. Furthermore, it may either increase the capacitor ratios or lower the noise performance due to compensation of the small parasitic capacitance by N-bit binary-weighted capacitor. In this thesis, critical node isolation and critical node pre-charge or pre-discharge techniques are proposed to compensate parasitic capacitances or to transform parasitic errors into mismatch errors, which can be compensated by the above mentioned mismatch error cancellation scheme.

One of the novel aspects of the proposed technique is that while the error cancellation is carried out, opamp gain boosting as well as opamp offset cancellation also occurs. This allows the usage of lower-gain wider-bandwidth opamps while ensuring high-accuracy data conversion. It will also be shown that the error cancellation techniques absorb any small error that may ordinarily be caused by top-plate parasitic capacitors. In the proposed SAR ADC, no extra clock phase is needed for the implementation of parasitic compensation.

4.2 Successive-Approximation ADC Architectures

The structure of the SAR ADC has been addressed in Chapter 2. A general block diagram of a SAR ADC is shown in Figure 4.1(a). The operation is straightforward; the sampled input voltage is continually compared to the output of the internal DAC. For a given input sample, that is only acquired once in a conversion period, the conversion will take place in N cycles (for an N-bit converter). According to the digital output (high or low) of the comparator, the successive-approximation register (SAR) selects the DAC's input

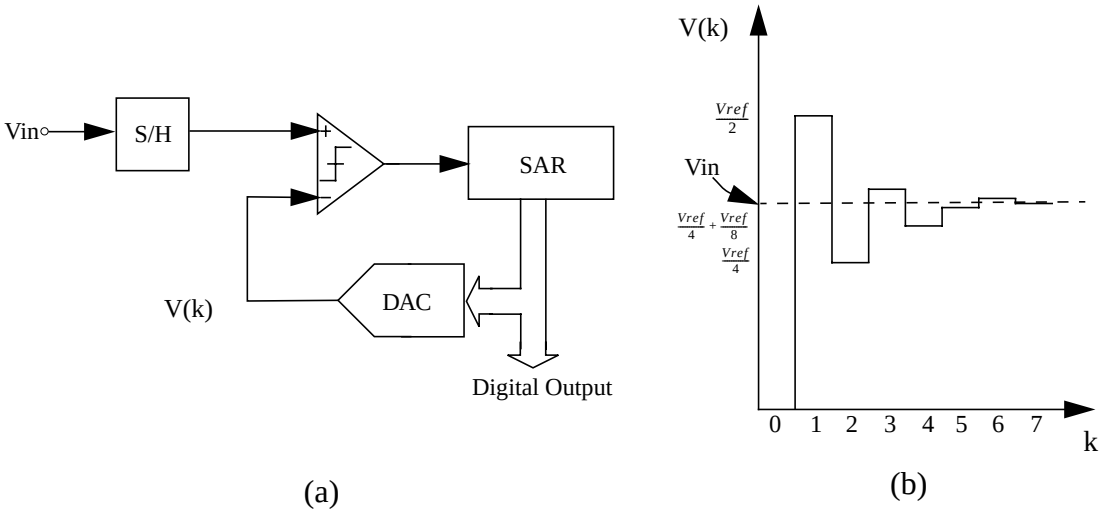


Figure 4.1: General successive-approximation ADC

data bits. Operation starts from finding the MSB in the first clock cycle, then progresses down to the LSB at the last N-th clock cycle. Figure 4.1(b) illustrates a possible scenario for an input sample.

In a SAR ADC, the internal DAC plays a highly critical role, as the accuracy of the converter is mainly defined by the DAC's accuracy. Therefore, it is essential that any error that may originate from the DAC be avoided. The switched capacitor implementation of the data converter will be subject to the following parasitic effects:

1 - Capacitor mismatch
2 - Finite-gain error and offset of opamp
3 - Parasitic capacitance
4 - Charge injection and clock feedthrough by switches

Before discussing how to cope with these issues in the following sections, we will introduce the proposed DAC to be used in the context of SAR ADC, as shown in Figure 4.2 [30]. The operation is as follows. (Assume, for now, that the opamp gain is very high and the offset is zero.) At the beginning of the conversion cycle, the capacitor C_1 is initially precharged to $Vref$, and C_f and C_2 are discharged. In the first clock cycle after the initial

reset, capacitors C_1 and C_2 share the charge that was stored on C_1, while dumping an equal and opposite charge into integrating capacitor C_f. This occurs if the data is high (MSB=1 as controlled by the SAR), and $\phi_x = \phi_1$. If the data is low (MSB=0), the ϕ_x switch stays open and the charge on C_1 (which is now half of what it had been previously) is preserved. The following data bits control the same set of operations for other bits. For an N-bit converter, the final DAC output is reached after N clock cycles (2N phases). For this specific simplified single-ended example, the output range of the structure is 0 to $-Vref$.

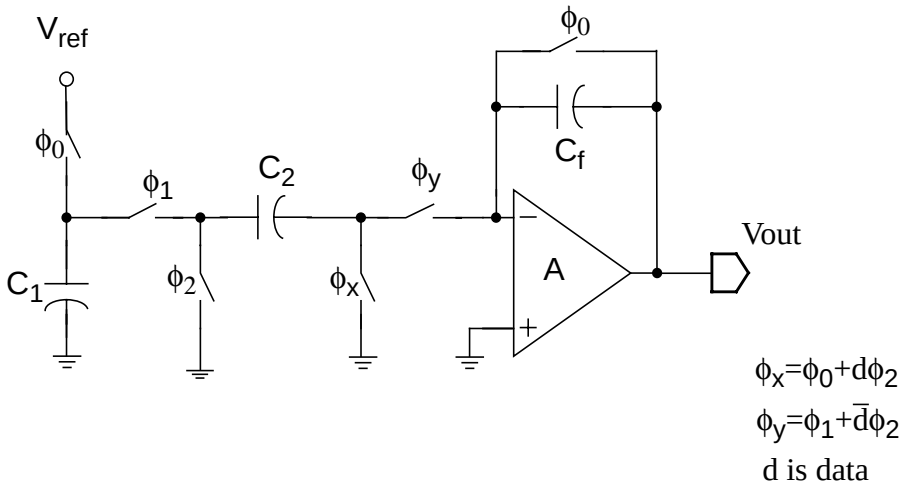


Figure 4.2: Two-capacitor charge-redistribution DAC

4.3 Capacitor Mismatch Error

For the DAC's operation described in the above, the capacitor mismatch between C_1 and C_2 has a direct impact on the linearity of the overall converter. Let's begin with the operation shown in Figure 4.3. Assuming that $C_1 = (1-\alpha)C$ and $C_2 = (1+\alpha)C$, the mismatch is defined by α. The errors resulting from the DAC may be fully described in terms of α. (The polarity of α is unimportant as long as it is consistent.) First consider the operation outlined in Figure 4.3(a). Given that the charge initially stored on C_1 in ϕ_1 is q, the amount of charge transferred to C_{int} during ϕ_2 is $-\frac{q}{2}(1+\alpha)$, equal and opposite to the

charge on C_2. The charge remaining on C_1, on the other hand, is $\frac{q}{2}(1-\alpha)$. If this process continues into the next clock phase, as shown in Figure 4.3(b), C_2 is discharged during ϕ_1, and the same operation occurs with the given initial charge of $\frac{q}{2}(1-\alpha)$. Thus, the charge transferred to C_{int} during ϕ_2 is $\frac{q}{4}(1-\alpha)(1+\alpha) \cong \frac{q}{4}$, and the remaining charge on C_1 is $\frac{q}{4}(1-\alpha)(1-\alpha) \cong \frac{q}{4}(1-2\alpha)$. We can see that error charge is directly related the capacitor mismatch α and the operation sequence. Based on the capacitor mismatch error contribution to the total DAC error as given above, the next step is to consider ways to properly manipulate their contributions so that the total error in a conversion period is suppressed.

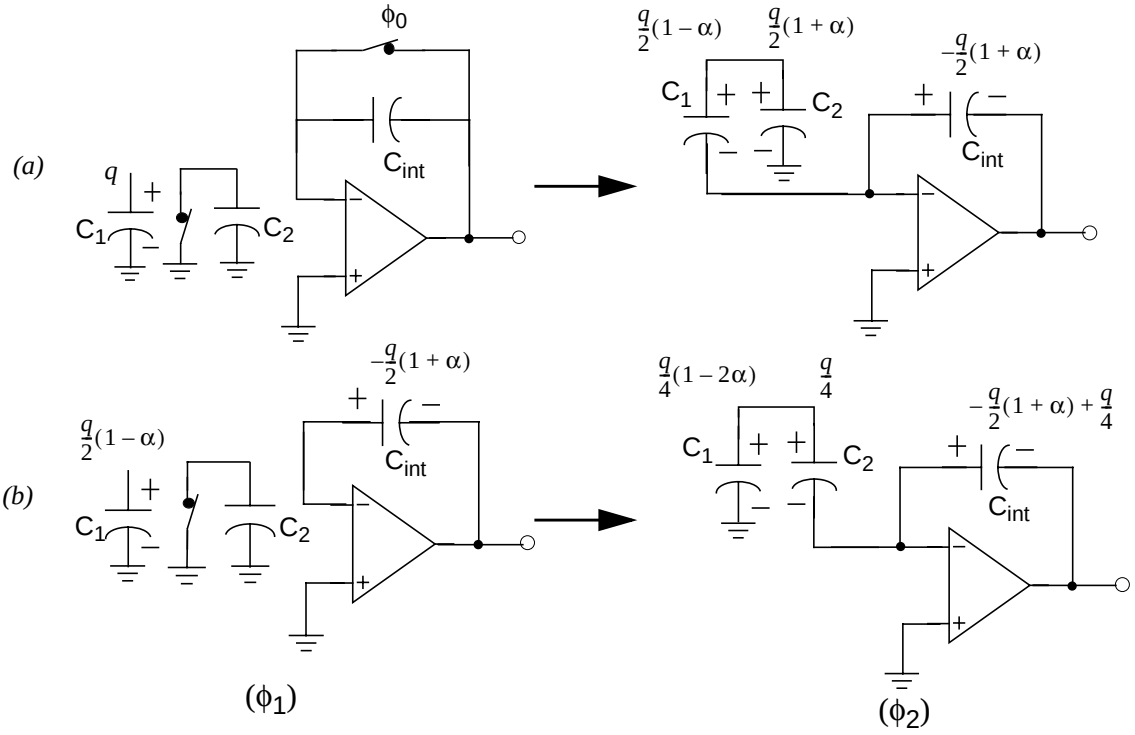


Figure 4.3: Capacitor mismatch error resulting from DAC

4.4 Mismatch Error Cancellation Algorithm

The accumulation error given in the previous section relates to a very specific operation, where the initial charge is always stored on $C_{1,}$ C_2 or C_1 is connected to the virtual ground in the next phase, as the charge is shared between C_1 and C_2. The available choice of which capacitor retains the charge and which capacitor connects to the virtual ground provides additional degrees of freedom for how much capacitor mismatch error is injected into the integrating capacitor C_{int}. In the differential configuration, another degree of freedom exists where the capacitors switched to virtual ground may be cross-coupled for changing the polarity of the charge transfer into C_{int} [31].

From all possibilities, four sets of sequences can happen in the SAR ADC of Figure 4.1 during two consecutive operations, as shown in the Table 4.1. That is, after the input has been sampled at the beginning of conversion, the output of the comparator (Figure 4.1) directs the next operation—either an *add* or a *subtract*, equivalent to selecting the MSB to be either 1 or 0. The bit/polarity selecting process continues until the LSB is resolved.

Table 4.1: Sets of operations in two consecutive conversions

Set	1	2	3	4
1st operation	ADD	ADD	SUB	SUB
2nd operation	ADD	SUB	ADD	SUB

Neglecting the parasitic effect, the error cancellation can be explained by a set of ADD/ADD operations (Figure 4.4). All possible events for the mismatch error cancellation algorithm are depicted in Table 4.2. Referring to Figure 4.4, the ADD/ADD illustrates the scenario where the comparator outputs are high twice in a row (giving digital data “1 1”).

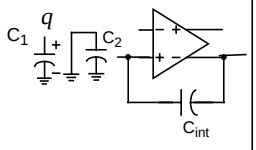
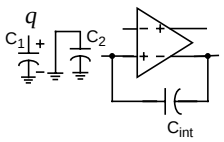
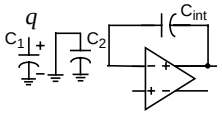
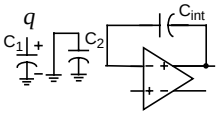
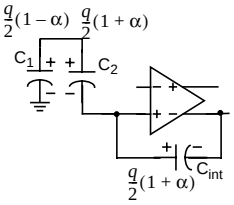
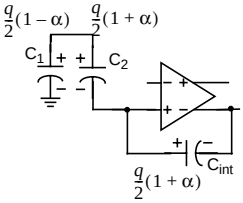
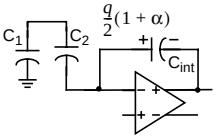
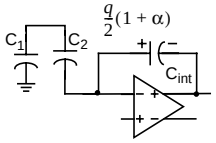
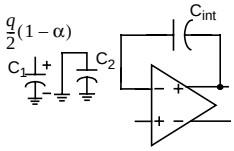
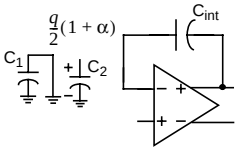
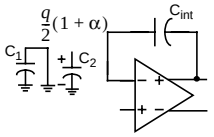
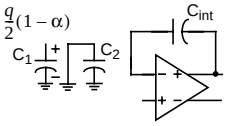
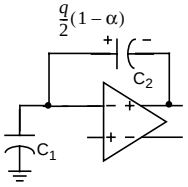
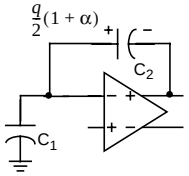
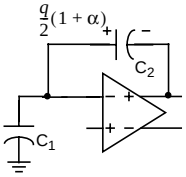
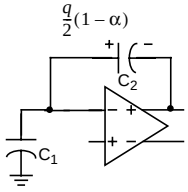
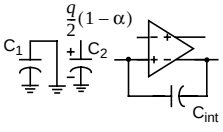
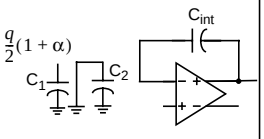
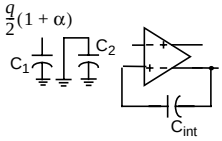
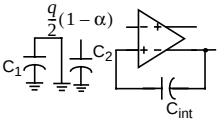
Observe that, at step 1(ϕ_1=1), C_2 is discharged and the initial charge is stored on C_1. At step 2(ϕ_2=1), the charges are shared and C_2 is connected to the opamp input. Note that C_2 is cross-coupled to maintain the positive (ADD) polarity. At this point, the charge transferred to C_{int} differentially (and the charge transferred to C_2) is $\frac{q}{2}(1+\alpha)$, and $\frac{q}{2}(1-\alpha)$ remains on C_1. At step 3(ϕ_1=1), C_2 is discharged. At step 4(ϕ_2=1), the charge from C_1 is transferred to C_2. At step 5(ϕ_1=1), C_1 is reset. Finally, at step 6(ϕ_2=1), when the charge is shared between C_1 and C_2, the charge transferred to C_{int} (equivalent to the charge transferred to C_1) is $\cong \frac{q}{4}(1-2\alpha)$, and $\cong \frac{q}{4}$ remains on C_2.

The above error analysis is approximate to the first order. The net result of this ADD/ADD operation is that after (1.5 cycle/per bit) $\times$ 2 bit = 3 clock cycles, the total charge transferred to the output (C_{int}) differentially is, to a first-order approximation, $\frac{q}{2}(1+\alpha)+\frac{q}{4}(1-2\alpha)=\frac{q}{2}+\frac{q}{4}$, and an error-free charge (to the first order) $\cong \frac{q}{4}$ remains on C_2, from which the next two bits of data may be processed.

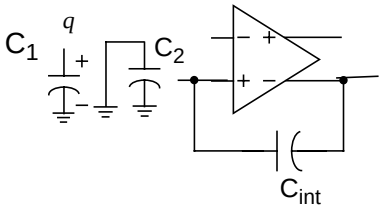
The error cancellation algorithm for the other three cases, (ADD/SUB, SUB/ADD, and SUB/SUB), as stated in Table 4.1 is outlined in Table 4.2. It shows that we again achieve the goal of zero net error injected to the output (C_{int}), and an error-free remaining charge $\frac{q}{4}$ to be used for the next pairs of bits.

One important aspect of the steps specified in the four columns in Table 4.2 is that the capacitor which is connected to the opamp virtual grounds is always the same one throughout all three cycles. The appropriate polarity is controlled by cross-coupling the capacitor to the inverting or noninverting input terminal of the opamp. The reason for maintaining the use of the same capacitor is to avoid any error that may result from the small top-plate parasitic capacitors. The issue of parasitic capacitance will be addressed in the next section.

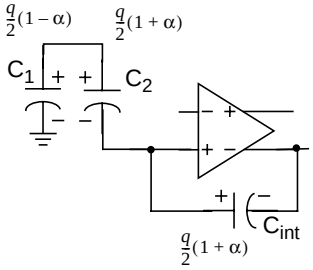
Table 4.2: Switching sequences for proper mismatch error cancellation

	ADD/ADD	ADD/SUB	SUB/ADD	SUB/SUB
step-1 (ϕ_1)				
step-2 (ϕ_2)				
step-3 (ϕ_1)				
step-4 (ϕ_2)				
step-5 (ϕ_1)				

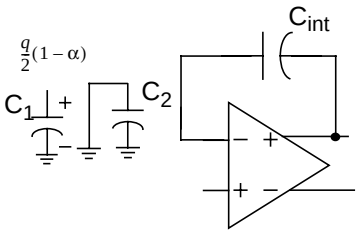
(i) Step 1 (ϕ_1)



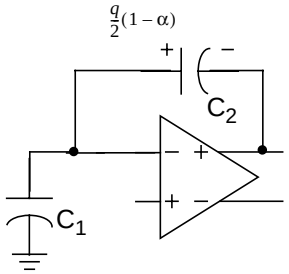
(i) Step 2 (ϕ_2)



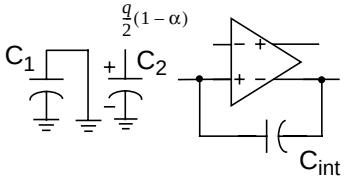
(i) Step 3 (ϕ_1)



(i) Step 4 (ϕ_2)



(i) Step 5 (ϕ_1)



(i) Step 6 (ϕ_2)

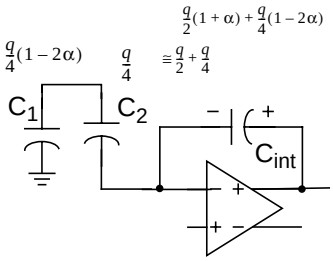
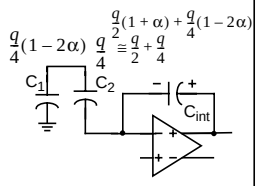
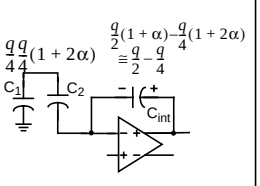
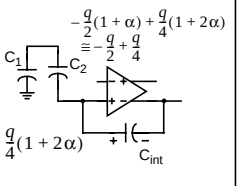
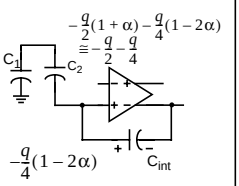


Figure 4.4: A case of mismatch error cancellation algorithm (ADD/ADD)

Table 4.2: Switching sequences for proper mismatch error cancellation

step-6 (ϕ_2)				

4.5 Parasitic Capacitance Compensation

In the last section, we have mentioned parasitic capacitance compensation. As we examine Figure 4.4 carefully, we can find that there is another parasitic sensitive operation. At step 4 (ϕ_2=1), when the charge from C_1 is transferred to C_2, the parasitic capacitance of the right plate of C_2 is charged. Thus, the charge on the parasitic will enter C_{int} at step 6 (ϕ_2=1), which degrades the error cancellation. We will discuss the compensation of parasitic capacitance in this section.

4.5.1. A Parasitic Insensitive Technique

The most widely used parasitic insensitive scheme is never charging or never discharging as shown in Figure 4.5. Because parasitic sensitive node ❶ is grounded during both phases, the parasitic does not affect the operation of circuit [11]. But it can not be used in some applications such as Figure 4.4, since the potential at the top and bottom plate of capacitor C_1 and C_2 changes during operation.

As pointed out, a self-calibration technique was proposed earlier [29] to compensate the effect of parasitic capacitances. But it either increases the capacitor ratios

or lowers the noise performance, and needs requires complex control logic and one extra DAC. Hence, another parasitic capacitance compensation technique will be exploited.

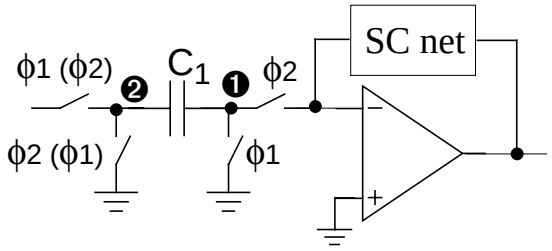


Figure 4.5: Operation sequence of mismatch error toward zero ADC

4.5.2. The Same Path Charge Flowing

In the last Section on mismatch error cancellation, we have mentioned using the same capacitor to avoid any error that may result from the top-plate parasitic capacitors. This is illustrated in Figure 4.6. The two possibilities for the data converter operation, ADD and SUB operation, are shown in the figure. The top part of Figure 4.6 is the initial condition; the left part is parasitic sensitive ADD and SUB operation; the right part is the parasitic insensitive ADD and SUB operation.

If the capacitors that connect to the opamp are interchanged for the ADD and SUB operations as shown in the left portion of the Figure, the charges transferred to C_{int} in the two cases (ADD and SUB) are

$$\Delta q_{ADD} = \frac{c_1}{c_1 + c_{1p}} \bullet \frac{c_2 + c_{2p}}{c_1 + c_{1p} + c_2 + c_{2p}} q = \frac{c_1}{c_1 + c_{1p}} \bullet (1 + \alpha)\frac{q}{2} \qquad (4.1)$$

$$\Delta q_{SUB} = \frac{c_2}{c_2 + c_{2p}} \bullet \frac{c_2 + c_{2p}}{c_1 + c_{1p} + c_2 + c_{2p}} q = \frac{c_2}{c_2 + c_{2p}} \bullet (1 + \alpha)\frac{q}{2}. \qquad (4.2)$$

The additional terms $\frac{c_1}{c_1 + c_{1p}}$ and $\frac{c_2}{c_2 + c_{2p}}$ resulting from the top-plate parasitic

capacitances (C_{1p} and C_{2p}) will produce error when applied to the first-order cancellation algorithm. Even though the effect of the top-plate parasitic mismatch (more specifically, the mismatch of the ratios) may be small, any amount of mismatch in the order of the nominal capacitor mismatch (α) or greater significantly degrades the first-order cancellation.

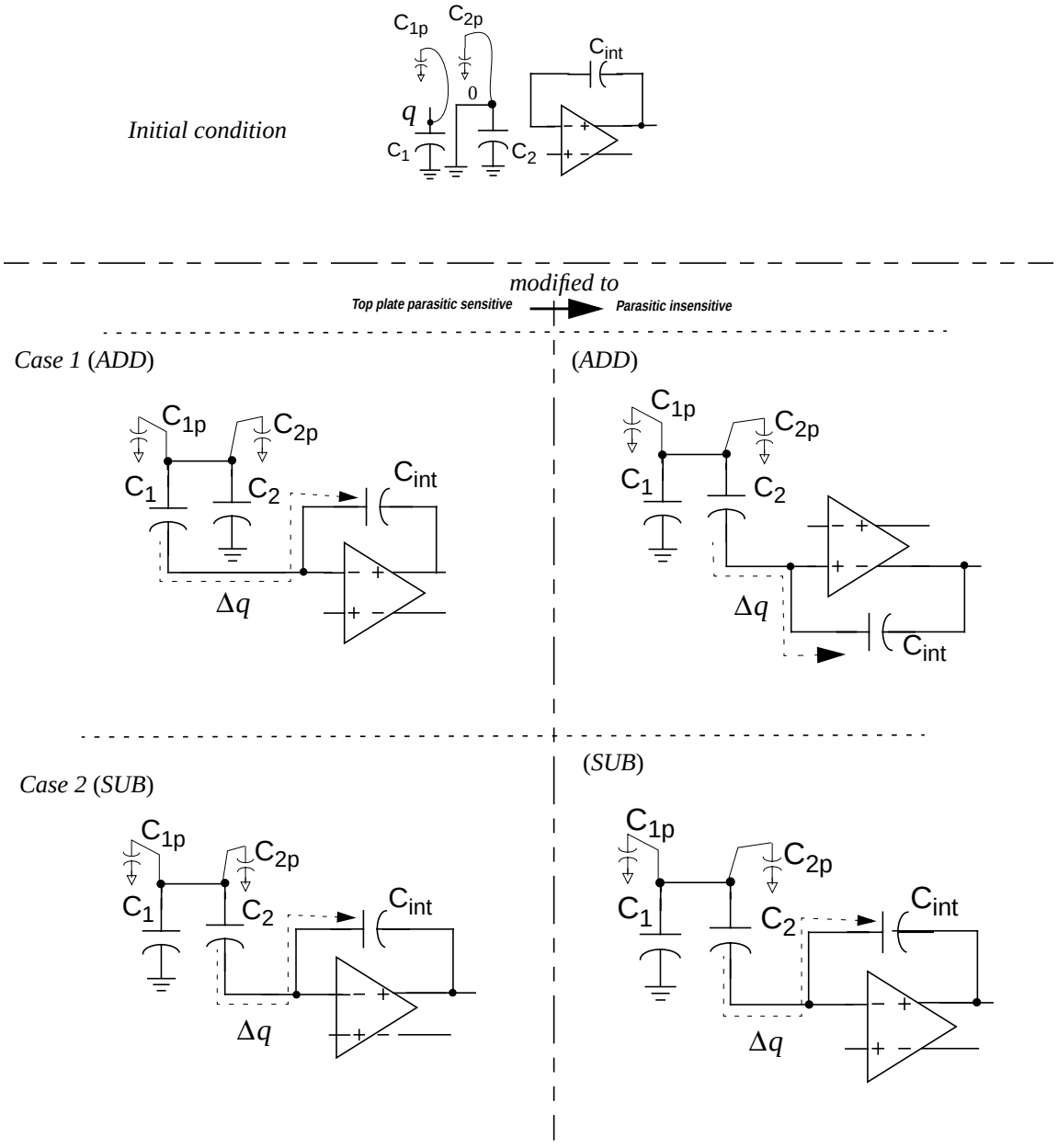


Figure 4.6: The same path charge flowing (top-plate parasitic insensitive technique)

Shown in the right portion of Figure 4.6, is the proposed scheme, following the rules specified in Table 4.2. Due to allowing only C_2 to connect to the opamp, the charges transferred to C_{int} in the two cases (ADD and SUB) have the absolute values:

$$\Delta q_{ADD} = \frac{c_2}{c_2 + c_{2p}} \bullet \frac{c_2 + c_{2p}}{c_1 + c_{1p} + c_2 + c_{2p}} q = \frac{c_2}{c_2 + c_{2p}} \bullet (1 + \alpha)\frac{q}{2} \qquad (4.3)$$

$$\Delta q_{SUB} = \frac{c_2}{c_2 + c_{2p}} \bullet \frac{c_2 + c_{2p}}{c_1 + c_{1p} + c_2 + c_{2p}} q = \frac{c_2}{c_2 + c_{2p}} \bullet (1 + \alpha)\frac{q}{2}. \qquad (4.4)$$

The appropriate polarity of the charge transferred to C_{int} (differentially) is ensured by the cross-coupling option. The top-plate parasitic mismatch issue no longer exists with the proposed scheme. It can be shown that the term $\frac{c_2}{c_2 + c_{2p}}$ only contributes an overall gain error to the ADC and does not degrade the converter linearity.

4.5.3. Parasitic Capacitance Predischarge or Precharge

In this Section, we will deal with the bottom-plate parasitic capacitances. First we examine the left part of Figure 4.7. At step 4, parasitic capacitance C_{2p} is charged. At step 5, we leave the C_2 alone. Then, at step 6, the error charge will go to C_{int}. The bottom parasitic capacitance introduces an error charge that degrades the system performance.

We can simply discharge the parasitic capacitance C_{2p} so that we can get rid of the error charge. Then the bottom plate parasitic insensitive operation is as shown in the right portion of Figure 4.7, which is exactly the same as step 4 to 6 of Figure 4.4. It shows that at step 5, there is no error charge on C_{2p} that would otherwise enter C_{int} and degrade the circuit performance.

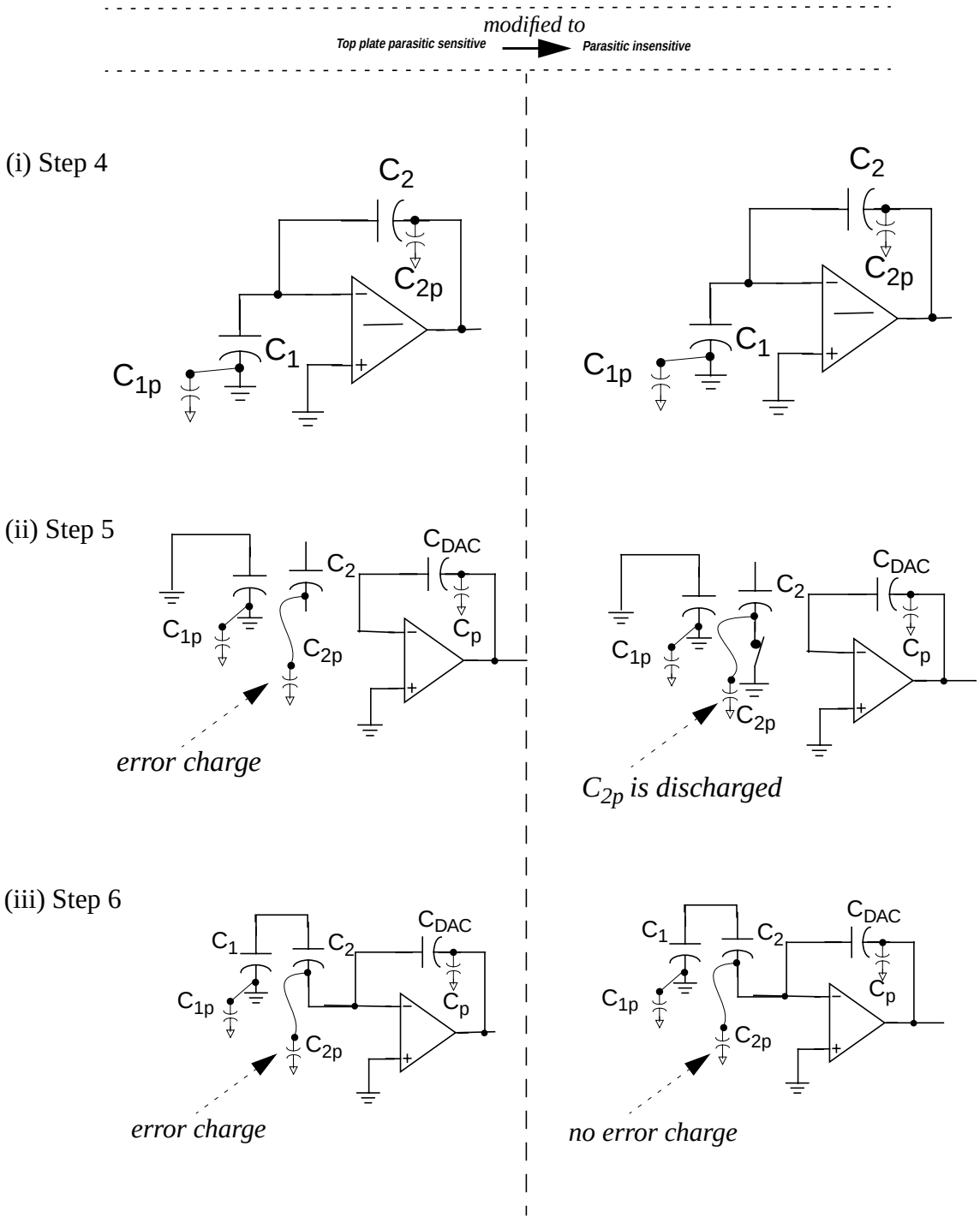


Figure 4.7: Parasitic predischarge or precharge (bottom-plate parasitic insensitive technique)

4.5.4. Parasitic Isolation

Note that the issue in this Section is not encountered in our design. The issue and the corresponding technique are discussed to remind us of the effect of parasitic coupling that may degrade the performance.

As shown in Figure 4.8(a), the voltage divider is extremely sensitive to the parasitic capacitance C_{p3} at node ☞, since C_{p3} can either charge from C_1 or C_2, and discharge to C_1, C_2 or *GND*. C_{p1} and C_{p2} are coupled through C_{p3}, which results in harmonic distortion. The parasitic insensitive structure is shown as Figure 4.8(b). C_{p3} is eliminated and C_{p1} and C_{p2} are also isolated by switch S_0. The effect of C_{p1} and C_{p2} only introduces gain error effect and mismatch error, which can be cancelled by the mismatch error cancellation algorithm presented before.

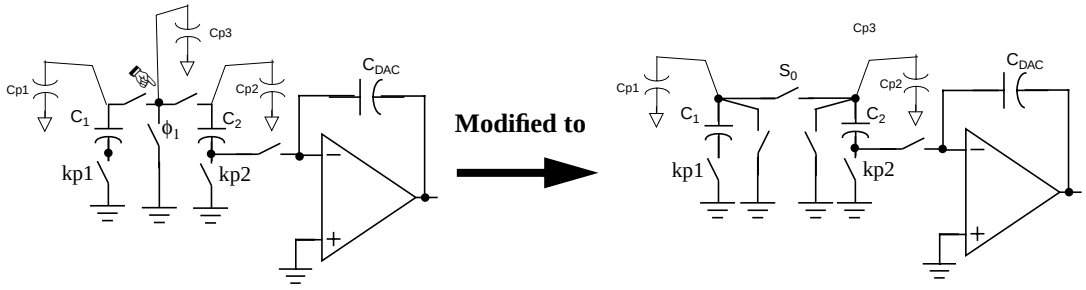


Figure 4.8: Parasitic isolation

4.6 Implementation And Simulation

A 16-bit successive-approximation A/D converter was implemented, as shown in Figure 4.9. The operation rule is outlined in Table 4.3, which is similar to Table 4.2 except for the added gain-offset compensation. Opamp gain and offset compensation utilizing predictive correlated double sampling (CDS) technique was adapted for this ADC. As illustrated in Table 4.3, the opamp is not used during $\phi_1 = 1$. A set of nominally equal capacitors is used when $\phi_1 = 1$ to predictively compensate for the opamp gain and offset before the real operation takes place during $\phi_2 = 1$. Finally, the circuit is implemented in fully differential structure to improve the circuit performance. Note that the input sample-and-hold (S/H) is incorporated into the DAC itself.

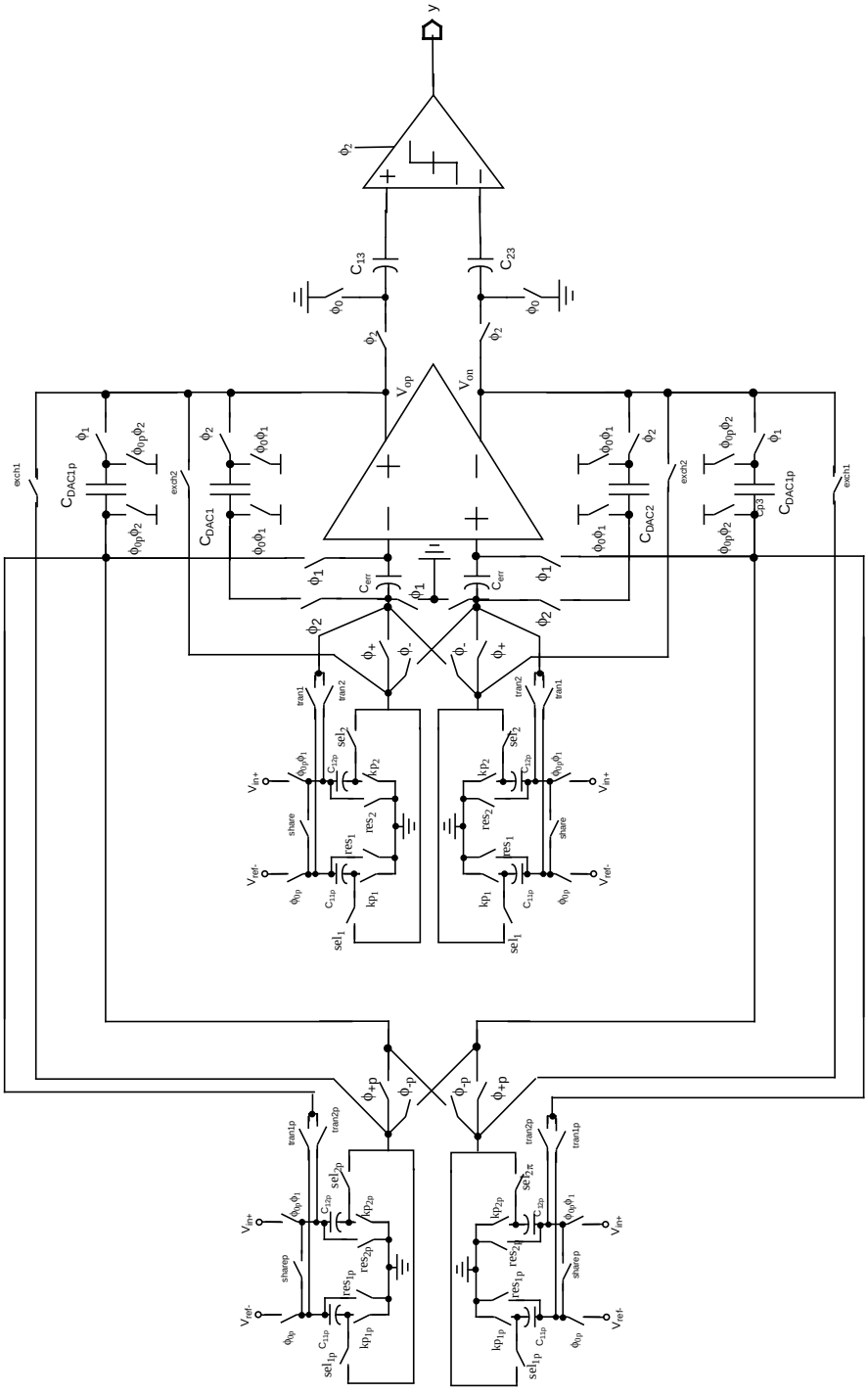
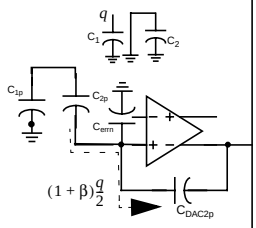
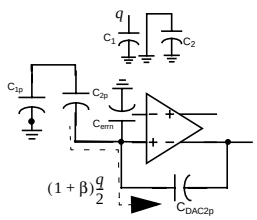
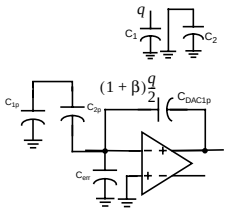
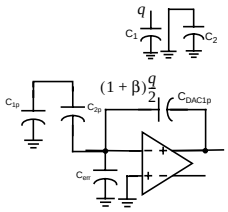
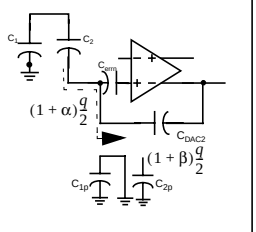
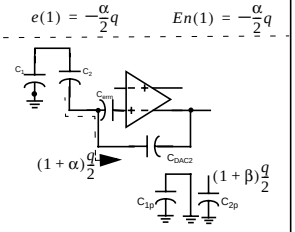
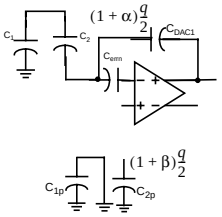
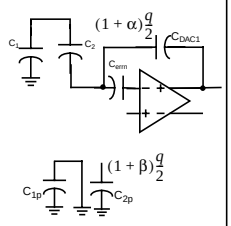
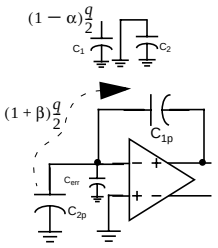
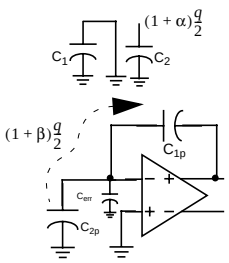
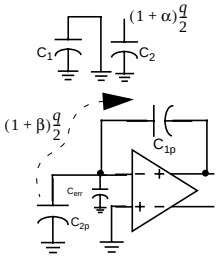
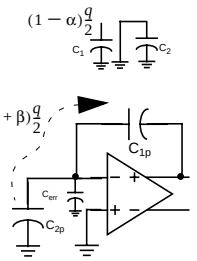
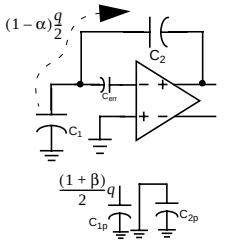
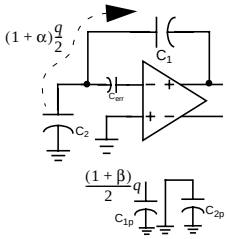
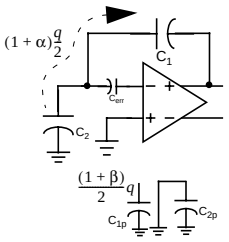
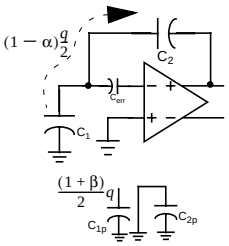
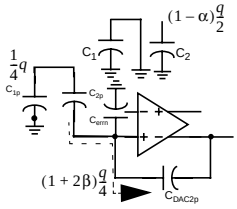
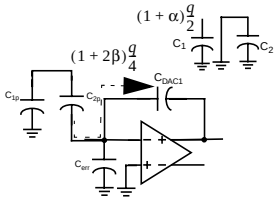
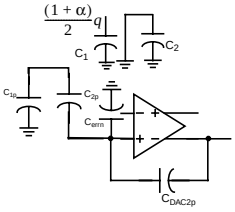
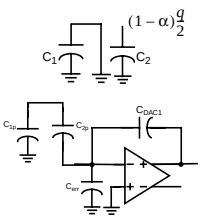
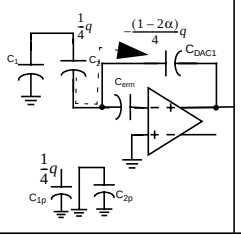
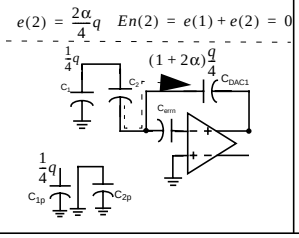
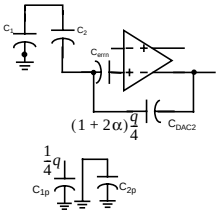
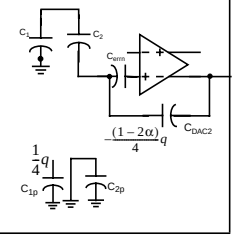


Figure 4.9: Differential gain- and offset-compensated implementation

Table 4.3: The outline of error cancelling operation

	ADD/ADD	ADD/SUB	SUB/ADD	SUB/SUB
$\phi 1$ (1)				
$\phi 2$ (2)				
$\phi 1$ (3)				
$\phi 2$ (4)				
$\phi 1$ (5)				
$\phi 2$ (6)				

The extensive SWITCAP simulation includes non-idealities of 0.5% RMS capacitor mismatch, 10% randomized parasitic capacitors, opamp gain of 66 dB, and 30 mV opamp offset. A realistic clock feed-through model associated with switches was also incorporated into the SWITCAP simulation. The simulation results for before and after the capacitor mismatch error compensation technique is applied are shown in Figure 4.10. This nonlinear uncompensated ADC with an SNDR of 57.1 dB has improved to a virtually distortion-free converter with an SNDR of 82.6 dB.

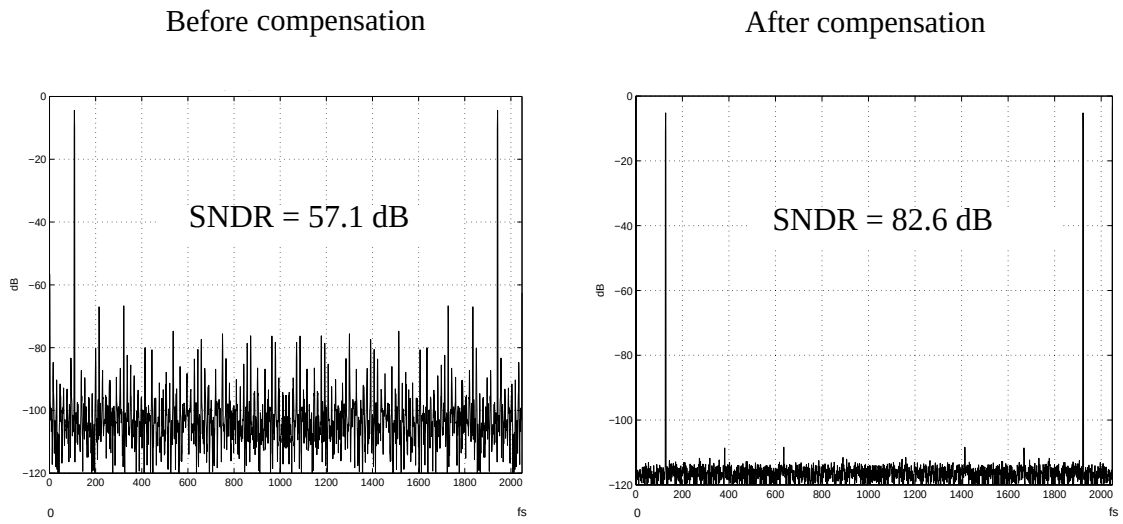


Figure 4.10:Output spectra obtained using of SWITCAP simulation

4.7 Conclusion

The proposed technique for algorithmically canceling the capacitor mismatch error has been described, and shown to be effective via SWITCAP simulation. This chapter has addressed only one specific DAC structure for illustration, but other DAC structures can also be used to achieve the same end goal. The proposed technique has been shown to suppress all capacitor mismatch error to a first-order accuracy (virtually error-free for all practical purposes), and can compensate for even small top-plate parasitic capacitances. The bottom-plate parasitic capacitance can be discharged to get rid of its error charge. The implementation utilizes a predictive correlated double sampling (CDS) technique to overcome errors resulting from finite opamp gain and opamp offset. Because the proposed data converter only contains a simple opamp, a comparator, and a few switches and capacitors, the power consumption is expected to be very low. Hence it is a good candidate for low-power low-voltage applications.

Chapter 5. Summary and Future Work

5.1 Summary

New techniques for high-resolution low-power ADC design are proposed in this thesis. Even in the presence of circuit non-idealities, using the proposed techniques, the circuit introduced can provide highly accurate A/D conversion. The following topics are included:

1. Investigation of A/D architectures that are suitable for low-power high-resolution application.

2. The principle of correlated-double-sampling technique, and the concept of predictive correlated-double-sampling in the context of A/D conversion.

3. Brief analysis of the effects of op-amp gain nonlinearity in SC circuits, and a comparison of the S/THD performance of various SC circuits.

4. A cyclic A/D converter with a new ratio-independent multiply-by-two stage using differential sampling.

5. A successive-approximation A/D with a new and efficient error cancellation scheme.

The simulations verify the effectiveness of the proposed schemes, and the robustness of the proposed A/D converters.

5.2 Future Work

Both theoretical analysis and simulation show that the proposed ADC can achieve high performance with low power consumption. We need to lay out and fabricate one or more chips to verify the performance.

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