DIGITAL CORRELATION TECHNIQUE FOR THE ESTIMATION AND CORRECTION OF DAC ERRORS IN MULTIBIT MASH $\Delta\Sigma$ ADCS

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SUMMARY

A fully digital algorithm is described for acquiring and correcting the errors of the feedback DAC used in a multibit $\Delta\Sigma$ MASH ADC. The method operates in the background and is highly accurate. It is particularly useful for wideband ADCs, where mismatch error shaping becomes ineffective. Combined with an improved digital adaptive compensation technique, which greatly reduces the raw quantization leakage in MASH architecture, it makes the design of fast and accurate ADCs using inaccurate components possible.

KEYWORDS

$\Delta\Sigma$ ADCs, multibit, correction, DAC

1. INTRODUCTION

In most state-of-the-art $\Delta\Sigma$ ADCs, multibit internal quantizers are used to obtain improved stability and resolution. The key problem then is how to deal with the inherent nonlinearity of the feedback DAC. Various techniques have been suggested to improve the effective DAC linearity. These included randomization [1], mismatch error shaping (see, e.g., [2]), direct error correction [3, 4] and digital error correction[5, 6, 7]. Randomization eliminates harmonics, but raises the noise floor; mismatch error shaping is effective for high oversampling ratios (OSR > 32), but not useful for wideband ADCs where OSR values can be as low as 4. The digital correction technique of [5] needs extra DAC unit elements and a modified noise transfer function, while the method of [7] needs an auxiliary ADC. This paper describes a fully digital correction method which acquires a digital estimate of the DAC element errors from the DAC input signal and the overall ADC output signal, after both signals were digitally preprocessed. As in the algorithm recently proposed by Galton to improve the accuracy of pipeline ADCs [8], this method uses the correlation of digital signals. It can be used even for very low OSRs, and thus applicable to wide-band signals. Since the process operates in the background, the correction process can follow any drift effects caused by environmental changes.

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2. THE PRINCIPLE OF THE DAC CORRECTION SCHEME

Fig. 1 shows a MASH $\Delta\Sigma$ ADC which uses the proposed technique. The first stage of the ADC is a second-order structure with relaxed linearity requirements on the first integrator proposed in [9]. Here, it uses a multibit quantizer. Errors of the DAC in its feedback path limit the overall conversion linearity and need to be corrected. The DAC has $M + 1$ levels and M unit elements, so the thermometer-coded output of the ADC, $d(k)$, has a wordlength of M. A scrambler (SCR) precedes the DAC which randomly reorders these M bits. $b(k)$ is the scrambled data, each bit of which determines the use of one unit element. Suppose each unit element has an ideal output value of 1. The average of their real outputs are α. The real output of the ith element deviates from α by αe_i, and

$$\sum_{i=1}^{M} e_i = 0. \tag{1}$$

Then, the output of the DAC is

$$a(k) = \alpha \sum_{i=1}^{M} b_i(k) + \alpha \sum_{i=1}^{M} b_i(k) \cdot e_i + v_{os}, \tag{2}$$

where v_{os} is the constant DAC offset. Each error e_i is modulated by a sequence $b_i(k)$.

In the output of the ADC, the modulated errors are also affected by the DAC error transfer function, as shown below:

$$\begin{aligned} y(k) &= u(k) \circledast stf(k) + q(k) \circledast ntf(k) \\ &\quad + \alpha \sum_{i=1}^{M} [b_i(k) \circledast etf(k)] \cdot e_i + v_{os} \circledast etf(k), \end{aligned} \tag{3}$$

where $u(k)$ is the input signal and $q(k)$ is the quantization noise introduced by the quantizer in the second stage, while $stf(k)$, $ntf(k)$ and $etf(k)$ are the impulse responses of signal transfer function, noise transfer function and DAC error transfer function, respectively. The symbol $\circledast$ denotes discrete time convolution.

To acquire the error values from the ADC output, we need to suppress sufficiently the interferences from the input signal, quantization noise and DAC offset. The input signal is at lower frequencies, and hence can be partially suppressed by a high-pass filter, which also suppresses the DAC offset. This filtering will not attenuate the modulated errors too much, because due to the random scrambling the $b_i(k)$ have their power distributed over a wide spectrum. For the quantization noise, which also has a wide spectrum, filtering does not work. However, quantization noise is a random signal and is uncorrelated with the modulated errors. Therefore, correlating the high-pass-filtered ADC output with the modulating sequences $b_i(k)$ should suppress the quantization noise and extract the errors. Unfortunately, the sequences $b_i(k)$ used in the correlation are correlated among themselves, so the result contains linear combinations of the errors. To separate out single errors, which is necessary for later correction, the exact relationship between the sequences should be known.

Sequences $b_i(k)$ can be separated into two parts: the mean value of all M bit streams plus the individual deviations $n_i(k)$ [10]:

$$b_i(k) = \frac{1}{M} \sum_{j=1}^{M} b_j(k) + n_i(k) \tag{4}$$

Here,

$$n_i(k) = - \sum_{j=1, j \neq i}^{M} n_j(k) \tag{5}$$

holds. The sequences $n_j(k)$ on the right side of (5) can be separated into two parts–a scaled version of $n_i(k)$ plus a sequence $m_i(k)$ which is uncorrelated with $n_i(k)$:

$$n_j(k) = -\beta \cdot n_i(k) + m_j(k), \quad j = 1 \ldots M, j \neq i \tag{6}$$

Because the scrambling is random, all $n_j(k)$ ($j = 1 \ldots M$, $j \neq i$) have equal status. It is reasonable to assume and was also verified by simulations that β is constant for all j's in (6). From (5), $\beta = (M-1)^{-1}$. Since the $n_i(k)$ $(i = 1 \ldots M)$ obey such simple relations, we can use them rather than the $b_i(k)$ as the correlating sequences. Combining (2), (1) and (4), we have

$$a(k) = \alpha \sum_{i=1}^{M} b_i(k) + \alpha \sum_{i=1}^{M} n_i(k) \cdot e_i + v_{os} \tag{7}$$

and

$$\begin{aligned} y(k) &= u(k) \circledast stf(k) + q(k) \circledast ntf(k) \\ &\quad + \alpha \sum_{i=1}^{M} n_i'(k) \cdot e_i + v_{os} \circledast etf(k), \end{aligned} \tag{8}$$

where

$$n_i'(k) = n_i(k) \circledast etf(k).$$

The errors e_i are thus modulated by $n_i(k)$ at the DAC output.

The larger the power of the quantization noise, the more clock periods are needed to suppress it. MASH ADCs often have much less quantization noise power in their final outputs than single-loop $\Delta\Sigma$ ADCs. This is the reason we propose the technique in the context of a MASH ADC here.

On the basis of the derivation given above, the error acquiring and correction process is performed as follows (see Fig. 1): as indicated in (4), $\overline{b}(k) = \frac{1}{M} \sum_{i=1}^{M} b_i(k)$ is subtracted from $b(k)$. The estimate of $n_i'(k)$ is obtained in the digital domain then by filtering $n_i(k)$ with a digital filter $\hat{ETF}$, emulating ETF, resulting in $\hat{n}_i'(k)$. The result enters the same high-pass filter (HPF) that is used to suppress the input signal and becomes $n_i''(k)$. Finally, the $n_i''(k)$ are correlated (in block CORR) with the high-pass-filtered ADC output $y'(k)$, giving

$$\hat{e}_i(k) = \left(\frac{M-1}{M} \right) \cdot \frac{\sum_{m=0}^{k} [y'(m) \cdot n_i''(m)]}{\sum_{m=0}^{k} [n_i''(m)]^2}. \tag{9}$$

The scale factor of $\frac{M-1}{M}$ is derived from (6).

The estimated results $\hat{e}_i$ are stored in the RAM and are updated in every clock period. They are read out to multiply the $\hat{n}_i'(k)$, $i = 1 \ldots M$, and the result is subtracted from $y(k)$ to give the corrected output

$$z(k) = y(k) - \sum_{i=1}^{M} [\hat{n}_i'(k) \cdot \hat{e}_i]. \tag{10}$$

3. SIMULATION RESULTS

System level simulations were done using Simulink and the Schreier Toolbox for $\Delta\Sigma$ Modulators [11]. The multibit DAC in the first stage was assumed to have 33 levels and 32 unit elements. The value of α was assumed to be 1. A random 0.1% rms error was introduced into the unit elements when modeling the real DAC. Fig. 2(a) shows the output spectra of the MASH ADC using an ideal DAC as well as using a real DAC, with no calibration or dynamic element matching used. Here the clock frequency was 100 MHz and the oversampling ratio was 4. With a 1.56 MHz, -0.92 dB sine-wave input, the output SNDR was 102.6 dB for the ideal case and 76.2 dB for the real case.

The simulation results of two dynamic element matching algorithms under the same conditions are shown. Zero-order randomization (Fig. 2(b)) only caused a 3.1 dB improvement in the SNDR, since it raised the noise floor, althought it removed the tones. Data-weighted averaging lowered the noise floor, but caused strong signal-dependent tones and only achieved an SNDR of 85.2 dB (Fig. 2(c)). Using the same real DAC, the proposed technique raised the output SNDR to 101.5 dB under the same conditions after a correction process lasting 131,072 clock periods. The output spectrum is shown in Fig. 2(d).

4. REFERENCES

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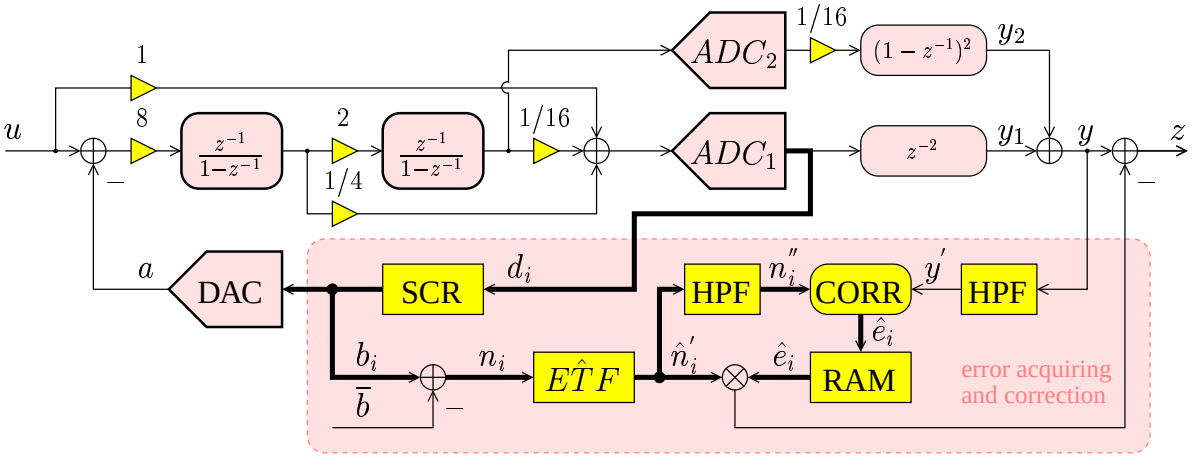

Fig. 1. MASH ADC with the proposed error correction system.

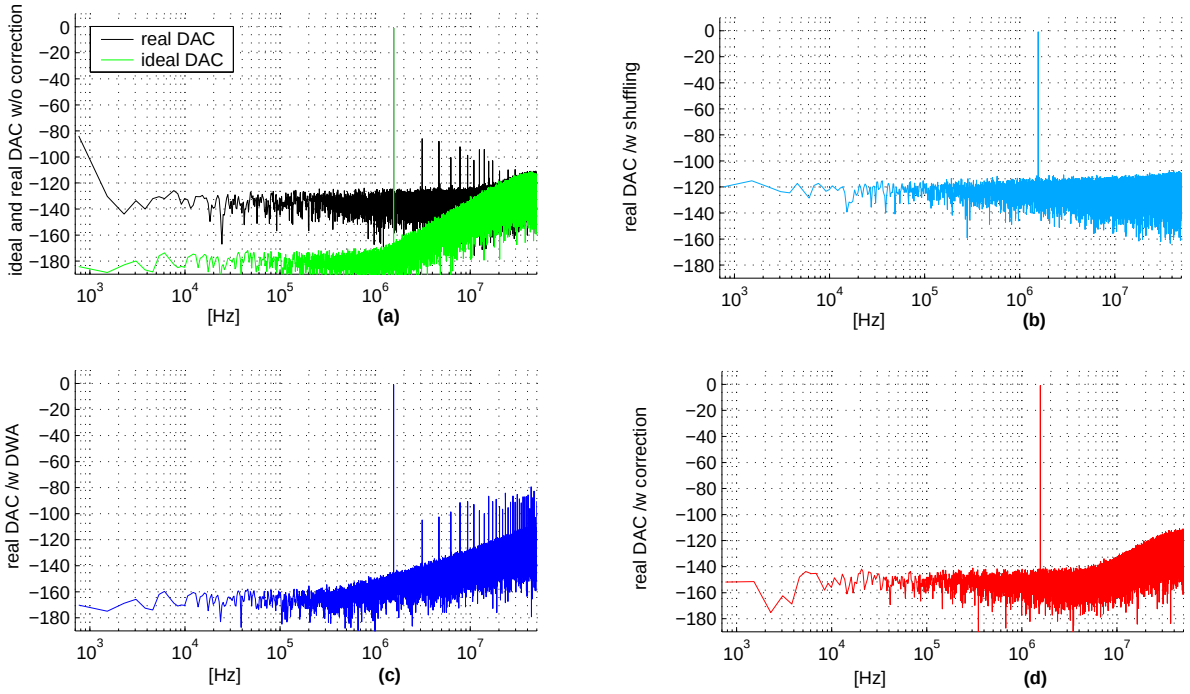

Fig. 2. Simulation results.