A Voltage-Mode Switched-Capacitor Bandpass ΔΣ Modulator

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Summary **- A novel fourth-order voltage-mode switched-capacitor bandpass ΔΣ modulator, using direct-charge-transfer pseudo-N-path resonators, is described. This modulator is insensitive to component mismatches and finite opamp bandwidth, and is also less sensitive to finite opamp gain than previous bandpass ΔΣ data converters. It is therefore suitable for high-speed communications applications.**

Keywords **- bandpass, delta-sigma, mismatches.**

I. Introduction

Many switched-capacitor (SC) bandpass ΔΣ analog-to-digital converters (ADCs) have been recently implemented since the first reported fully monolithic implementation appeared in 1993 [1]. A center frequency f_0=10.7 MHz is often used for superheterodyne receivers with a bandwidth of 200 kHz for GSM applications, and a bandwidth of 10 kHz for intermediate-frequency (IF) communications applications.

As discussed in the literature, there are several issues to consider during the design of bandpass ΔΣ modulators including center frequency accuracy, signal-to-noise ratio (SNR), and signal-to-distortion ratio (SDR). Opamp imperfections and component mismatches generally limit these performance parameters. Most implementations of SC bandpass ΔΣ modulators suffer from additive noise and spurs in the band of interest due to capacitor mismatches on the signal paths.

In this paper, a fourth-order voltage-mode bandpass ΔΣ modulator implementation with improved performance is discussed. It uses resonators based on a direct-charge-transfer pseudo-N-path (DCT-PNP) structure, proposed by us earlier [2], which showed superior performance compared to other existing architectures. The proposed modulator is suitable for communication applications requiring both high accuracy and low power consumption.

II. Pseudo-N-Path Resonator with Direct-Charge-Transfer

The direct-charge-transfer PNP resonator shown in Figure 1 was previously proposed [2]. On one of the three paths in this structure, *C1p* and *C1n* hold the differential output voltage $v_{out}(n)$ during clock phase 'c'. At the same time, *C3p* and *C3n* are connected between the output and the input of the resonator, and hence they are charged to $-v_{out}(n)+v_{in}(n)$ and $v_{out}(n)-v_{in}(n)$, respectively. Two clock periods later, the *C3* capacitors are connected as feedback capacitors during clock phase 'b', thus providing the output signal $v_{out}(n+2)$ to the next stage. The other two paths alternately operate in the same way.

The proposed DCT-PNP resonator is realized with no charge transfer through the virtual ground of the opamp, i.e. operates in a *voltage mode*. Therefore, the finite bandwidth of the opamp does not affect the accuracy of the resonant frequency, while the finite gain of the opamp introduces only a reduction of the *"Q"* of the resonator. This architecture directly samples the input signal and the previous output value with the same capacitors in order to reduce sensitivity to opamp imperfections.

III. Bandpass Modulator Implementation

The system diagram of the proposed voltage-mode bandpass ΔΣ modulator structure is shown in Figure 2. This fourth-order modulator is based on the low-distortion architecture proposed by Silva et al. [3]. In this implementation the input is sampled by the first stage capacitors. The DAC feedback signal is also applied to the inputs of the first stage, which requires one more pair of input terminals for the resonator. A modified DCT-PNP resonator architecture, as shown in Figure 3, provides these additional terminals in voltage-mode operation. The DAC signal is always processed by the same capacitors, *Cref*, even though the three paths process the input signal. Both of these signals are unaffected by relative capacitor mismatches since the same capacitor always samples and provides the output. Although this architecture is insensitive to capacitor mismatches, analysis reveals that it is sensitive to the mismatches of the *top-plate parasitic* capacitances. However, these mismatches only affect the input signal,

since three-path processing is only applied to the input signal. Hence, this effect only creates out-of band images, which can easily be removed by a digital filter.

The second stage requires signal scaling by a factor of ½ which is achieved with a modified DCT-PNP resonator as shown in Figure 4. Voltage division between equal valued capacitors C1p1 and C1p2 obtains the factor of ½. Here, voltage-mode operation is still achieved allowing for high frequency and low-power operation. The scaling in the second stage introduces mismatch effects; however, these will be negligible since they are suppressed by the first stage gain. The frequency spectrum from a SWITCAP simulation is shown in Figure 5. In this simulation, 1% mismatches were included for all capacitors and 5% mismatches were assumed for all top-plate capacitor parasitics.

IV. Conclusions

A novel voltage-mode bandpass ΔΣ modulator was proposed using DCT-PNP resonators. This modulator is insensitive to component mismatches and finite opamp bandwidth, and is also less sensitive to finite opamp gain. Additionally, the DAC feedback is processed by the same capacitors as the input in order to eliminate the folding of out-of-band noise into the passband. The proposed modulator is suitable for communication applications requiring both high accuracy and low power consumption.

Acknowledgements

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References

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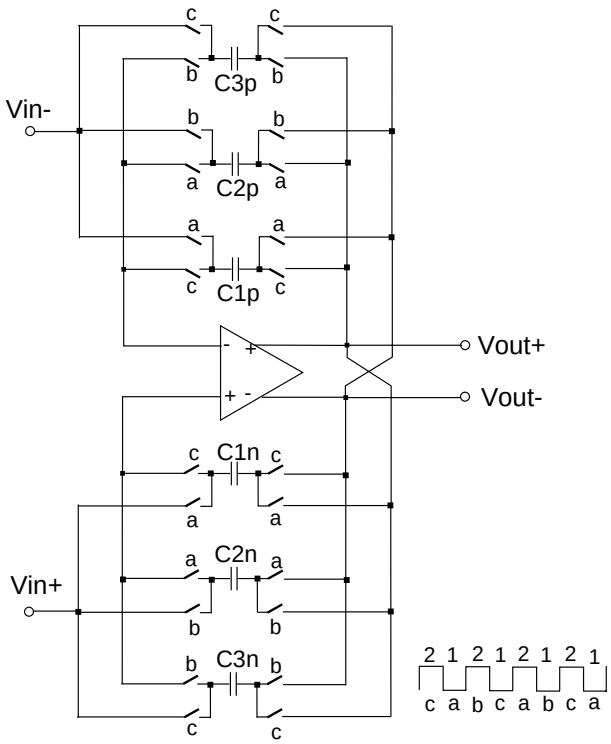

Figure 1: Direct-charge-transfer pseudo-N-path (DCT-PNP) SC resonator.

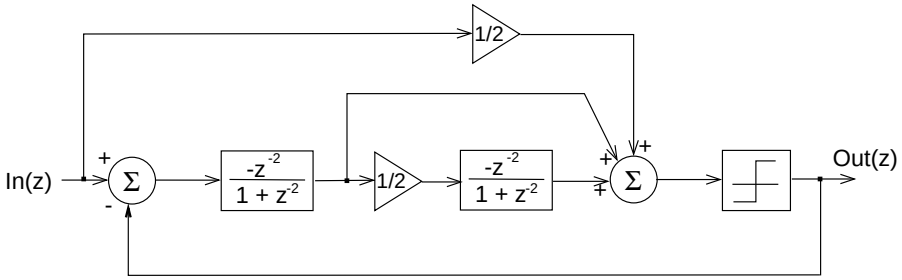

Figure 2: System diagram of the proposed fourth-order voltage-mode bandpass ΔΣ modulator.

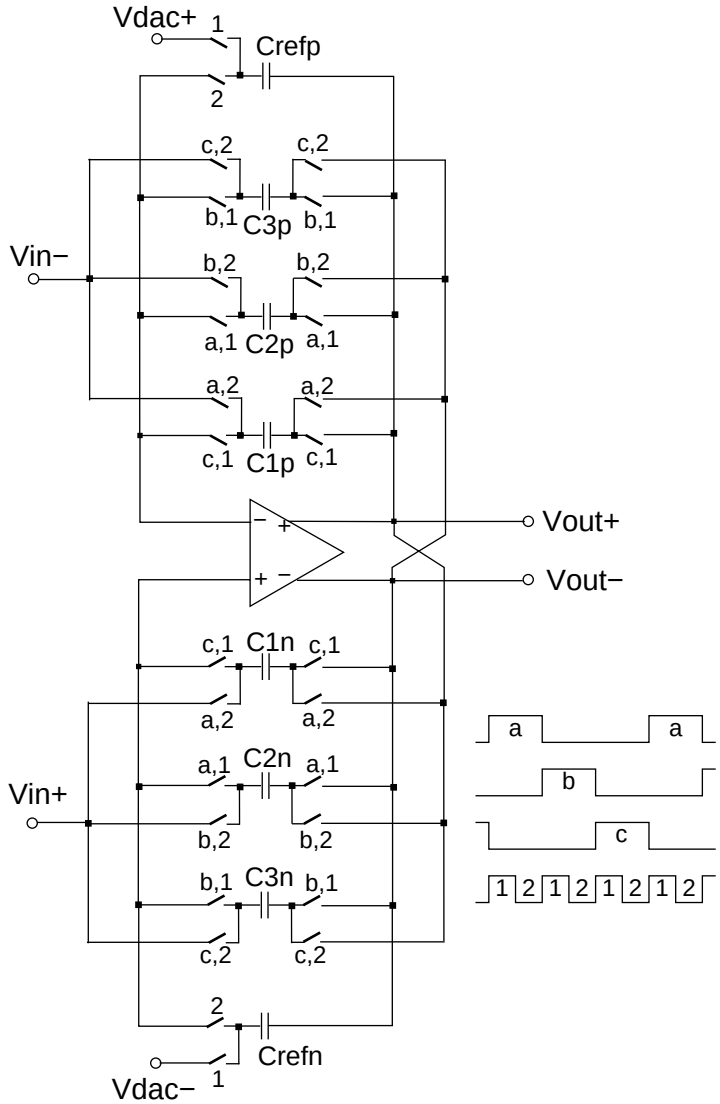

Figure 3: First stage DCT-PNP resonator with signal and DAC feedback inputs.

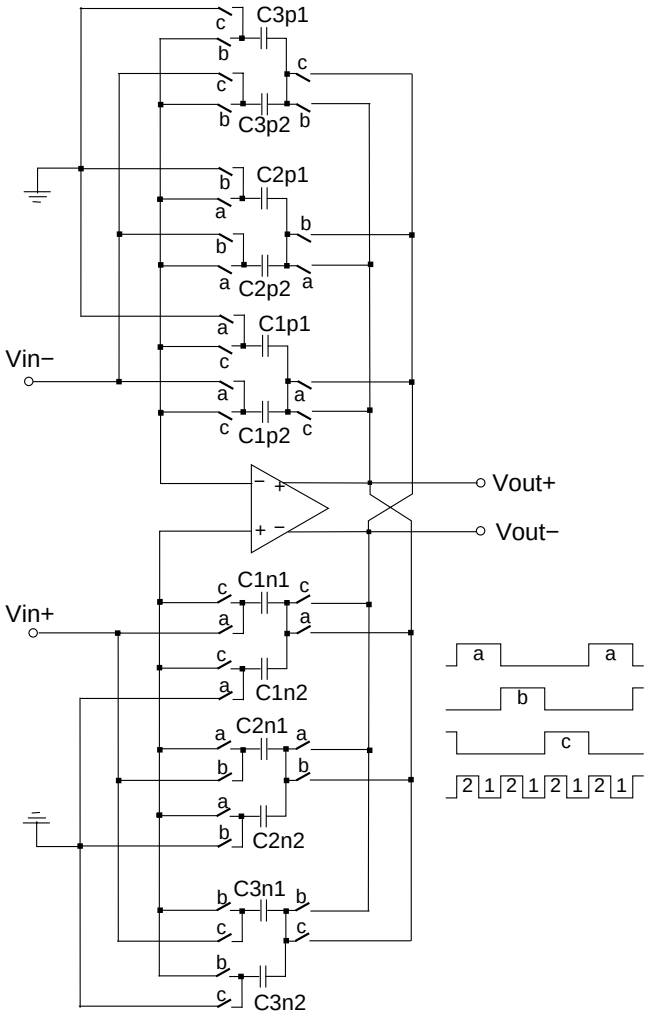

Figure 4: Scalable DCT-PNP SC resonator for the second stage.

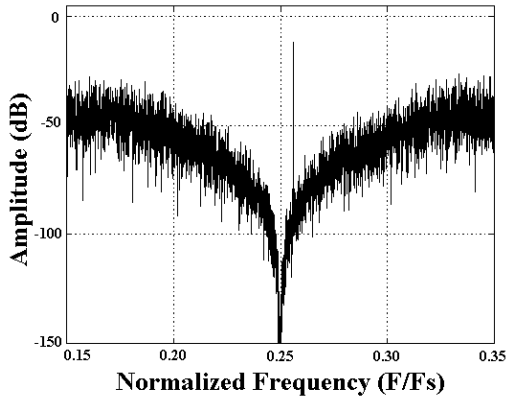

Figure 5: SWITCAP simulation results for the proposed voltage-mode bandpass ΔΣ modulator.