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A 100-dB gain-corrected delta-sigma audio DAC with headphone driver

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Abstract An oversampled digital-to-analog converter (DAC) with a 100-dB A-weighted dynamic range is presented. It uses a switched-capacitor (SC) array to transfer the sampled charges directly into the headphone driver. The overall DAC gain is precisely controlled by a novel reference stage. A new dynamic element matching algorithm, based on split-set data-weighted averaging (SDWA), is used to improve the dynamic range and to reduce the nonlinearity caused by mismatches in the multibit DAC.

Keywords Audio · Delta-sigma · Switched-capacitor · DAC · SDWA

1 Introduction

Digital-to-analog converters (DACs) with wide dynamic range and high linearity are required for high-end audio application. Several audio DACs have been reported recently using a switched-capacitor (SC) hybrid postfilter [1–3] whose output feeds a separate headphone driver. In this work, an audio DAC is realized by using an SC array to transfer the sampled charges directly into the integrated headphone driver. Thus, the DAC and the driver can all be combined, and need only one opamp. Due to the poorly controlled value of the RC time constants on a chip, the gain of the DAC is likely to be inaccurate. To obtain accurate gain, a correction circuit was implemented, which forces the DAC reference voltage to track the variation of the DAC RC time constant. This keeps the DAC gain accurately controlled even under widely varying mismatch conditions.

Data-weighted averaging (DWA) is usually applied in multibit DACs to suppress mismatch noise in the signal band. However, DWA introduces idle tones for signal levels rationally related to the full-scale output of the DAC [4], which degrade the audio performance. We proposed a new algorithm, split-set data-weighted averaging (SDWA), to overcome this problem [5].

Figure 1 shows the overall block diagram of the audio DAC.

2 DAC with correction circuitry

Figure 2(a) shows the second-order Sallen-Key filter which is commonly used as the reconstruction filter in audio delta-sigma DACs. The DAC output is applied to this filter to remove out-of-band noise. In our system, the input resistor R_1 is replaced by a SC structure as shown in Fig. 2(b). By digitally controlling the SC branch, it can be used to perform the DAC function, saving hardware.

A problem with this new configuration is that the dc gain of the DAC is poorly controlled. The transfer function of the traditional Sallen-Key filter is given by

$$H(S)=\frac{-R_2/R_1}{2\cdot R_2R_3C_1C_2\cdot S^2+(R_2+R_3+R_2R_3/R_1)\cdot C_1\cdot S+1} \quad (1)$$

The dc gain of the filter is thus given by the ratio of R_2 and R_1, which is well controlled on chip. However, in the

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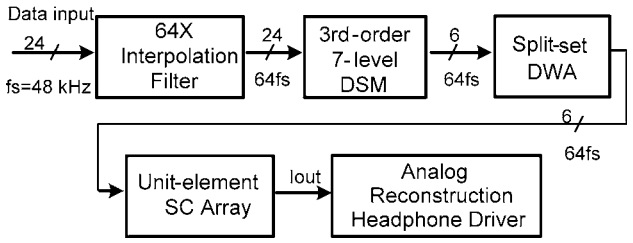

Fig. 1 Block diagram of the overall DAC and headphone driver

modified structure, the amplitude A of the filter output signal at dc is given by

$$A = 2 \cdot n \cdot V_{\text{rsc}} \cdot R_2 \cdot C_{\text{DAC}}/T_1 \tag{2}$$

Here, V_{rsc} is the reference voltage sampled by the SC array, n is the number of the unit elements in the SC array and T_1 is the clock period in the DAC. Equation (2) shows that amplitude A depends on the time constant $R_2 \cdot C_{\text{DAC}}$ which is poorly controlled on chip. To control the amplitude A accurately, a gain correction stage was introduced, as shown in Fig. 2(c). In steady state, the dc currents entering nodes A and B through the resistive and SC branches equal zero. The output voltages are then given by

$$V^+ = +V_{\text{ref}} \cdot T_2/(R_{\text{r}} \cdot C_{\text{r}}) \tag{3}$$

$$V^- = -V_{\text{ref}} \cdot T_2/(R_{\text{r}} \cdot C_{\text{r}}) \tag{4}$$

Here, T_2 is the clock period in the correction circuit. This stage generates the reference voltage for the DAC output stage. Combining (2), (3) and (4) gives

$$A = 2 \cdot n \cdot V_{\text{ref}} \cdot (T_2/T_1) \cdot (R_2/R_{\text{r}}) \cdot (C_{\text{DAC}}/C_{\text{r}}) \tag{5}$$

Equation (5) shows that amplitude A now depends on ratios of R and C values, which can be accurately controlled with careful layout. In general, T_1 and T_2 can be different, but in our design they were both set equal to the input sampling period.

3 Split-set data-weighted averaging

In audio applications, inband tones generated by the basic DWA algorithm are unacceptable. Randomization of DWA can reduce tone generation, but causes unequal usage of the DAC elements, and hence increases the noise floor. We developed a novel element selection algorithm, SDWA, which improves the spur-free dynamic range of DWA significantly while keeping the signal-to-noise ratio (SNR) high. It will be described next.

3.1 The SDWA algorithm

SDWA operates by splitting the unit element set into subsets in a special way, and randomizing each subset independently. It can improve the spur-free dynamic range (SFDR) without significantly degrading the SNR. For an N-element DAC, basic DWA is applied to the N unit elements of the DAC for M-1 clock cycles, and then in clock cycle M (where M may be predetermined, or identified by a

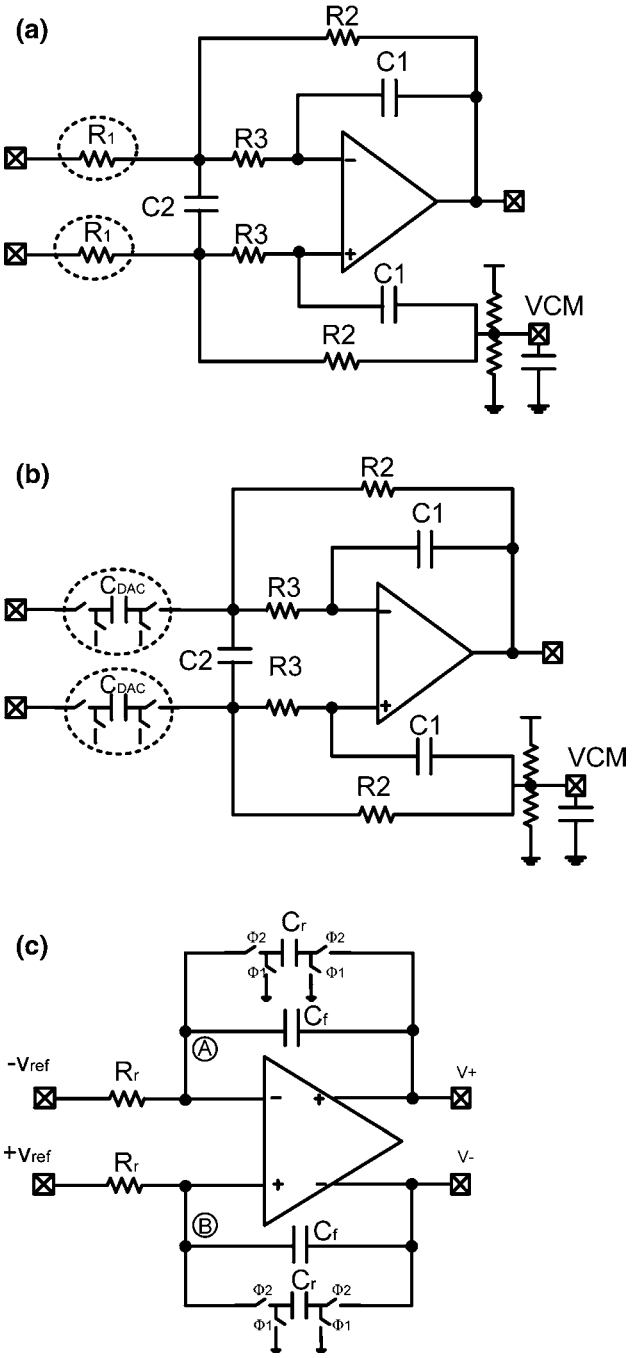

Fig. 2 DAC stages: (**a**) Conventional Sallen-Key filter; (**b**) SC realization; (**c**) Correction stage

pseudorandom digital signal reaching a predetermined value), the set of all unit elements is split into two subsets. Subset S_K contains elements 1 through k, where k is the highest unit-element index used in clock cycle M; its complement $\overline{S_K}$ contains elements with indices k + 1 through N. Next, all elements within the subset S_K are rotated (or scrambled), and a similar internal rearrangement occurs for the elements of $\overline{S_K}$. After this, DWA is restarted with the unit element now occupying position k + 1.

In Fig. 3, SDWA is illustrated for a seven-level DAC with the input sequence 4, 3, 1, 5. We assume $M = 1$, so that scrambling is performed in all clock periods. (M is in the range 104–106 in our design). The initial order of the unit elements is U1, U2, U3, U4, U5, U6. Starting with an input code 4, unit elements U1, U2, U3 and U4 are used. Then the unit elements are split into two subsets (U1, U2, U3, U4) and (U5, U6), which are rotated by one position independently, to give (U2, U3, U4, U1) and (U6, U5). The new order of all unit elements is thus (U2 U3 U4 U1 U6 U5). A second input data 3 is then going to chose unit elements (U6 U5 U2). Again the unit elements are split into (U2), (U3 U4 U1 U6 U5) and are rotated separately. The new order of unit elements now is (U2 U4 U1 U6 U5 U3). Figure 3 illustrates the rotations for subsequent inputs 1 and 5.

It is easy to see that equal usage of all unit elements is only minimally disturbed by this algorithm, because it guarantees that the usages of any two elements can differ by at most 1. Hence, the rise in the noise floor is very small.

3.2 Gate-level implementation of the SDWA algorithm

A fast and efficient gate-level implementation of the SDWA circuit for a seven-level DAC and $M = 16$ is shown in Fig. 4. Here, d1 ~ d6 are input thermometer bits and S6 ~ S1 are output SDWA data, A 3-stage logarithmic shifter is used to rotate these thermometer codes to generate basic DWA data required by SDWA algorithm. The initial order of the unit elements, (6, 5, 4, 3, 2, 1), is stored in the unit-element register and is updated by the subset shifter every 16 cycles. The output of the subset shifter is the new order of the unit elements, to be used for the next incoming data. The thermometer to binary converter, 3-bit adder, 3-bit subtractor, mux, pointer register and demux are used to realize the mod 6 adder, so that the pointer index used in logarithmic shifter and subset shifter can be generated. The baisc DWA data are the selection enable signals of the six demuxes in the output stage. For example, if the inputs of all six demuxes from top to bottom are UO6 = 5, UO5 = 6, UO4 = 1, UO3 = 4, UO2 = 3, UO1 = 2 (new unit element order generated by subset shifter), and the basic DWA data generated by the 3-stage logarithmic shifter is ''110001'' (demuxs 6, 5 and 1 are enabled and demuxs 4, 3, 2 are disabled), then the six demuxes have six group outputs: out6 = 010000, out5 = 100000, out4 = 000000, out3 = 000000, out2 = 000000, out1 = 000010. These six group demux outputs then drive six six-input OR gates to form the final SDWA data ''110010'' for controlling the switches in the SC array, which are going to chose unit elements 6, 5 and 2 (see Fig. 3 with input = 3). Only 671 transistors are needed to build this circuit. The power consumption is 0.54 mA with a 6.25 MHz input clock rate, and 1.93 mA with a 50 MHz clock rate, for Vdd = 3.3 V.

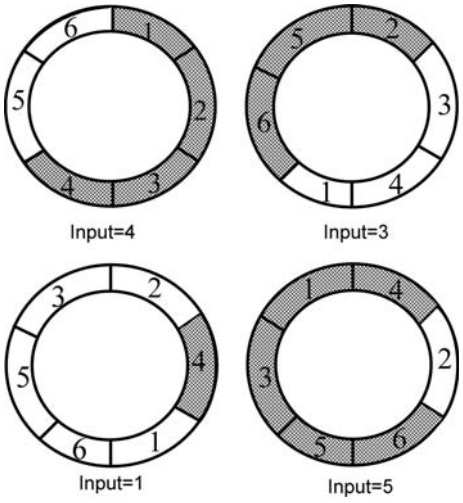

Fig. 3 The SDWA algorithm

4 Implementation of the DAC and headphone driver

As mentioned earlier, the filter opamp acts also as the headphone driver in the DAC. Figure 5 shows the proposed DAC architecture which includes the correction circuit, SC arrays providing a seven-level analog output, and the headphone driver which also acts as the analog reconstruction filter. Capacitors Cb are used to filter the output voltage of the correction circuit. The switches of the SC circuit are controlled by the output bits of the delta-sigma modulator, and scrambled using the SDWA algorithm. The SC array samples one of the correction circuit outputs V+ or V–, depending on the SDWA data. For a single-ended SC array, the load of the correction circuit would thus depend on the SDWA data, and would be unbalanced. Hence, a differential SC array is used in the design, to improve the noise immunity, and also to avoid an unbalanced load on the correction circuit.

The sampled charges generated by the DAC are fed directly into the headphone driver, which is embedded in the second-order Sallen-Key reconstruction low-pass filter.

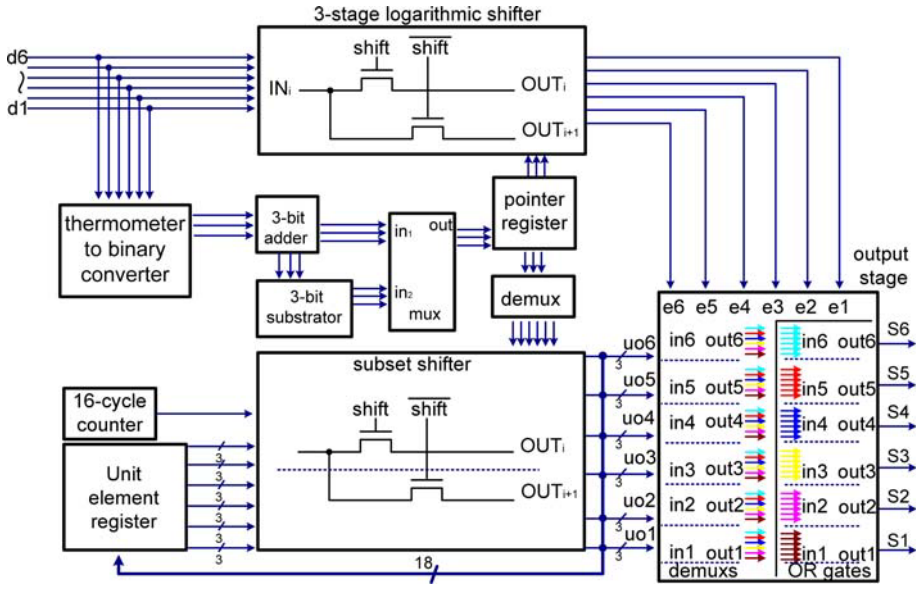

Fig. 4 SDWA implementation

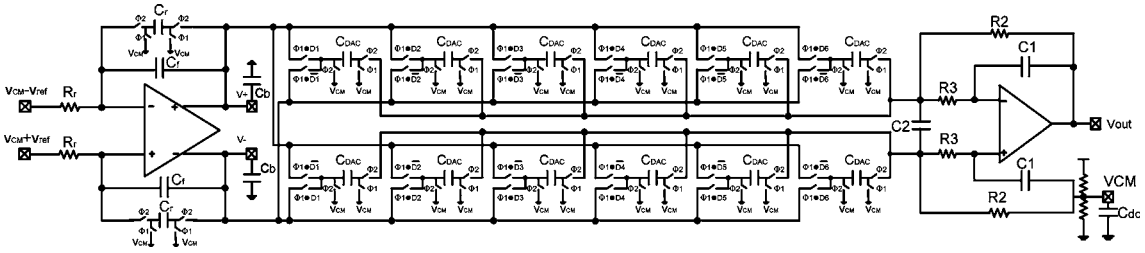

Fig. 5 Circuit diagram of the DAC with headphone driver

5 Experimental results

The SC audio DAC was fabricated in Samsung's 3.3 V, 0.35-μm CMOS process. All measurements were taken by the Audio Precision System 2.24 in the audio band (20 Hz–20 kHz), using SDWA algorithm. To drive the DAC, a third-order seven-level delta-sigma modulator was implemented in software, using the Schreier Matlab toolbox [6]. The signal bandwidth was 20 kHz and the sampling frequency was 48 kHz. The oversampling ratio was 64. The SDWA algorithm [5] was used to process the delta sigma output data, and to generate the input data for the SC array. Figure 6 shows an 1,024-point fast Fourier transform (FFT) of the output spectrum for a –60 dBFS input test signal. The noise floor was around –130 dBFS and the inband tones were below than –120 dBFS.

Figure 7 shows the A-weighted SNDR versus input level characteristics from –80 dBFS to –2 dBFS with a 1.008 kHz input signal. The load is a 32 Ohms resistor in parallel with a 220 pF capacitor. The dynamic range, calculated as the SNDR at –60 dBFS, is around 100 dB. The peak SNDR is 72 dB, and is limited by the distortion of the single-ended headphone driver. Figure 8 shows the gain correction performance, measured on five devices. The top curves show the spread of output amplitudes without correction; the bottom curves illustrate the uniform performance with correction. The die photo of the chip is shown in Fig. 9; the core area is about 1.12 mm^2.

A summary of the measured performance is given in Table 1.

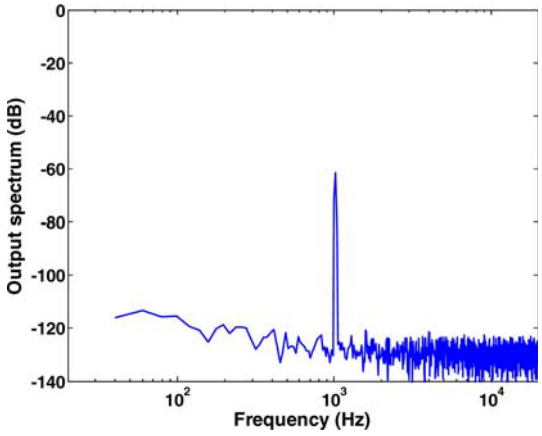

Fig. 6 Measured output spectrum with -60dBFS input sine wave

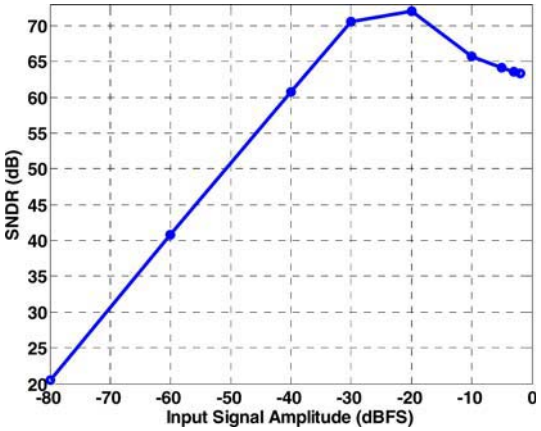

Fig. 7 SNDR versus input amplitude characteristics

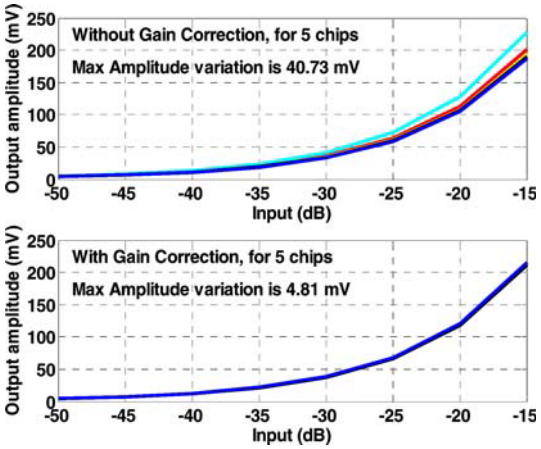

Fig. 8 Correction performance curves

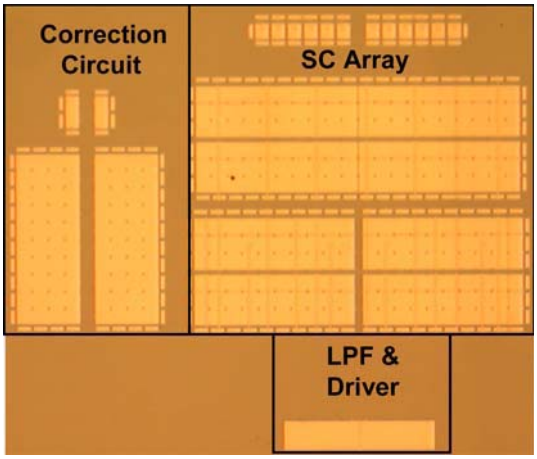

Fig. 9 Die photo

Table 1 Performance summary

Parameter	Value
Power supply	3.3 V
Power dissipation	9.57 mW
Dynamic range (SDWA, A-weighted)	100 dB
Peak SNDR	72 dB
Load	32 Ω ‖ 220 pF
Signal bandwidth	20 kHz
Die area	1.12 mm^2
Process	0.35 μm CMOS

6 Conclusion

A delta-sigma audio DAC, using a novel gain-correction technique, was described. It uses a novel algorithm for dynamic element matching.

Test results verify that it meets the requirements for a typical high-end audio system.

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