IEEE Asian Solid-State Circuits Conference
November 12-14, 2007 / Jeju, Korea

A 1.8V 36-mW 11-bit 80MS/s Pipelined ADC Using Capacitor and Opamp Sharing

Naga Sasidhar, Youn-Jae Kook, Seiji Takeuchi [1], Koichi Hamashita [1], Kaoru Takasuka [1], Pavan Kumar Hanumolu and Un-Ku Moon

School of EECS, Oregon State University, Corvallis, OR, 97331, USA
[1] Asahi Kasei EMD Corporation, Atsugi, Kanagawa 243-0021, Japan

Abstract— **A new capacitor and opamp sharing technique that enables a very efficient low power pipeline ADC design is proposed. A new method to cancel the effect of signal-dependent kick-back in the absence of sample and hold is also presented. Fabricated in a 0.18-µm CMOS process, the prototype 11-bit pipelined ADC occupies 2.2 mm^2 of active die area and achieves 66.7dB SFDR and 53.2dB SNDR when a 1MHz input signal is digitized at 80MS/s. The SFDR and SNDR are unchanged for 50MHz input signal. The prototype ADC consumes 36mW at 1.8V supply, of which analog portion consumes 24mW.**

I. Introduction

Pipelined analog-to-digital converters (ADCs) are considered most suitable for low-power/high-speed applications [1]. Because the accuracy requirements gradually decrease to the later stages of the pipeline architecture, properly scaling the capacitor size and opamp design/bias can efficiently reduce power consumption while maintaining the same ADC resolution [2]. Sharing an opamp between two consecutive stages can further reduce power and has demonstrated good performance for low power operation [3].
In a pipelined ADC it is known that amongst stages, maximum power is consumed in the first stage. To reduce power in it, a capacitor sharing technique was recently proposed [4], where the residue held on the feedback capacitor is used for the next stage MDAC operation thereby reducing the opamp load. This means that every alternate stage in the ADC can be made load-free. Our proposed technique simultaneously applies both capacitor and opamp sharing there by gaining a two fold reduction in power.

To further reduce power sample and hold (S/H) is removed. This would cause signal-dependent kick-back into the input source. In the presence of source impedance this kick-back would cause distortion. Simulations show a reduction in SNDR of about 6dB near Nyquist input. One solution to mitigate this is to reset the capacitors before sampling phase. But that would mean adding an additional phase and hence making the ADC slow. A novel reset scheme which fits in well with capacitor sharing technique has been used which would reset the capacitors without the need of an additional clock phase. The rest of this paper is organized as follows: Section II describes the capacitor and opamp sharing technique; Section III describes the capacitor reset technique; Section IV describes the circuit implementation of the prototype 11-bit pipelined ADC; and Section V presents the experimental results. Concluding remarks are given in Section VI.

II. Capacitor and Opamp Sharing Technique

One of the simplest implementations of pipelined ADCs incorporating digital redundancy is based on the 1.5-bit-per-stage architecture. This architecture is widely used to maximize conversion speed [1]. Fig. 1 shows a typical multiplying digital-to-analog converter (MDAC) used in this type of pipelined ADC architecture.

Fig. 2 shows first two 1.5-bit stages using opamp sharing technique. During ϕ_1, input signal (V_{in}) is sampled by two capacitors, C_{1f} and C_{1D}. During this phase, the opamp generates the residue value (V_{res2}), which is transferred to the third stage (to the third stage sampling capacitors C_{3f} and C_{3D}). During ϕ_2, capacitor C_{1f} is connected in the feedback path and C_{1D} is connected to one of three possible DAC voltages, $\pm V_{ref}$ or 0 depending on the sub-ADC output. The generated residue value V_{res1} is sampled by the second stage capacitors, C_{2f} and C_{2D}. It is apparent that this technique needs only one opamp to generate residues V_{res1} and V_{res2} of the two consecutive stages. In this configuration, it is worthy to note here that when V_{res1} is transferred to C_{2f} and C_{2D}, the same information is also already stored on C_{1f}.

Fig. 3 shows the proposed capacitor and opamp sharing technique. Here, C_{1f} is composed of two parts, C_{2f} and C_{2D}. During ϕ_1, input value is initially sampled on to the capacitors, C_{1f} and C_{1D}. During ϕ_2, the opamp generates the residue value but this is not transferred to sampling capacitors of the second stage. It should be noted here that the residue value is held on the feedback capacitor C_{1f}. During the next phase, ϕ_1, using the stored value on C_{1f} which is composed of C_{2f} and C_{2D}, second residue value is generated and transferred to sampling capacitors of the following/third stage, C_{3f} and C_{3D}. Since the next input value has to be sampled while generating the second stage residue, two sets of feedback capacitors, C_{1fE} and C_{1fO}, an *even* set (E) and *odd* (O) set, are used alternately.

Given the consideration that the most power hungry operation in a pipeline ADC is the very first stage, this

1-4244-1360-5/07/$25.00

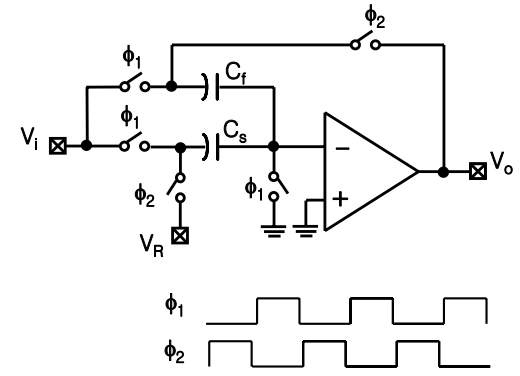

Figure 1: Typical switched capacitor MDAC

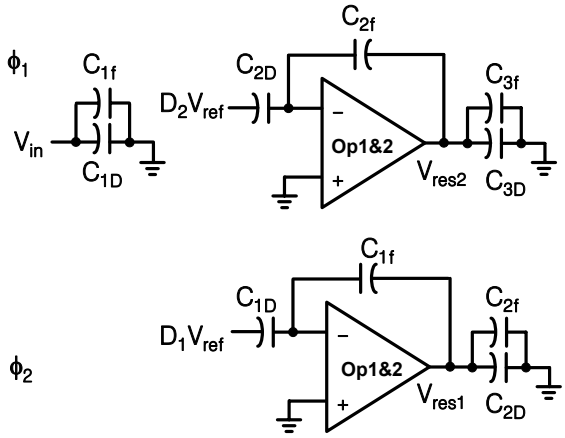

Figure 2: Residue generation using opamp sharing technique

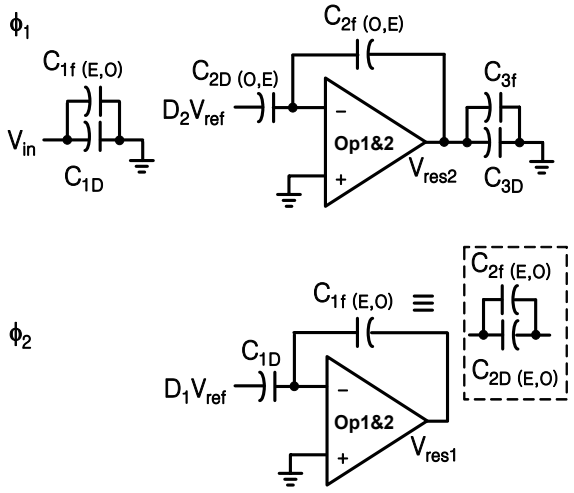

Figure 3: Residue generation using capacitor and opamp sharing technique

capacitor and opamp sharing technique efficiently reduces the overall power consumption because the effective capacitive load of the opamp is significantly reduced. In the conventional pipeline operation, the effective loading capacitance is C_{2f} + C_{2D} + (1-β)C_{1f}, as seen in Fig. 2, where β is the feedback factor due to capacitor voltage divider feedback. In the proposed capacitor sharing technique, the effective loading capacitance reduces to just (1-β)C_{1f}, as seen in Fig. 3.

A. Scaling and kT/C noise

The kT/C noise plays an important role in choosing the proper sampling capacitor value, and it strongly defines the fundamental limit (along with opamp noise) of the overall ADC. In a standard 1.5-bit-per-stage pipelined ADC, if a 75% scaling is applied from one stage to the next, which is considered a conservative scaling ratio, the input referred kT/C noise is about 1.5 kT/C. With the capacitor sharing technique, as proposed, the scaling factor is inherently 50% since the feedback capacitor is used to sample the residue value. When applying 50% scaling, the input referred kT/C value increases to about 1.9 kT/C. Compared with the 75% scaling case, the capacitor sharing technique increases the input referred kT/C noise by about 27%. Because this result is normalized to input sampling capacitor, simply increasing the size of the sampling capacitor by the same amount (27%) would make the noise same. Increasing the capacitor size may initially seem disadvantageous. However, in the capacitor sharing technique, because the capacitor values scale so quickly (by 50% from one stage to the next), the capacitance loading at each MDAC stage decreases significantly. In the conventional case, for example, applying 75% scaling, the effective loading capacitance is $2C_1$ (=2x0.75C_1+0.5x1C_1), as shown in Fig. 2, assuming low opamp input capacitance (simplified discussion here). On the contrary, the corresponding value with capacitor sharing technique, even after 30% increase (over estimating 27%), is 0.65C_1 (=0.5x1.3C_1), as shown in Fig. 3. The implied best case improvement is a three fold power saving.

III. RESET WITHOUT EXTRA PHASE

In the absence of a sample and hold, the capacitors have to be reset so as to avoid signal-dependent charge kick-back which would cause distortion. Fig. 4 shows the differential picture on how the capacitor C_{1D} is reset. On both positive and negative sides, C_{1D} is split into two halves C_{1dn}, C_{1dnv} & C_{1dp}, C_{1dpv}. Consider the left half of the figure. At the end of amplification phase(ϕ_2), C_{1dn}, C_{1dnv} & C_{1dp}, C_{1dpv} would have been charged either to the same common mode voltage or to equal and opposite polarity voltages (±Vref) basing on D1. In the following sampling phase C_{1dnv} & C_{1dpv} swap positions as shown. This would cause charge sharing between C_{1dn} & C_{1dpv} and C_{1dp} & C_{1dnv}, hence *resetting* them. On the other hand, as has been described before, there are two sets of C_{1f} capacitors C_{1fE} and C_{1fO}, an *even* set (E) and *odd set* (O) that are used alternately. As seen in Fig. 3, in phase ϕ_2 when one set is used for amplification, the other set is idle. The idle set goes to sampling in the next phase. So the idle time is used to reset them. This way the reset is implemented without requiring an extra clock phase.

IV. CIRCUIT DESIGN

Capacitor and opamp sharing technique is used only for first 4 stages, as the sampling capacitor becomes small after that. Opamp sharing is still used for the rest of the stages. The first stage opamp is implemented using a telescopic cascode

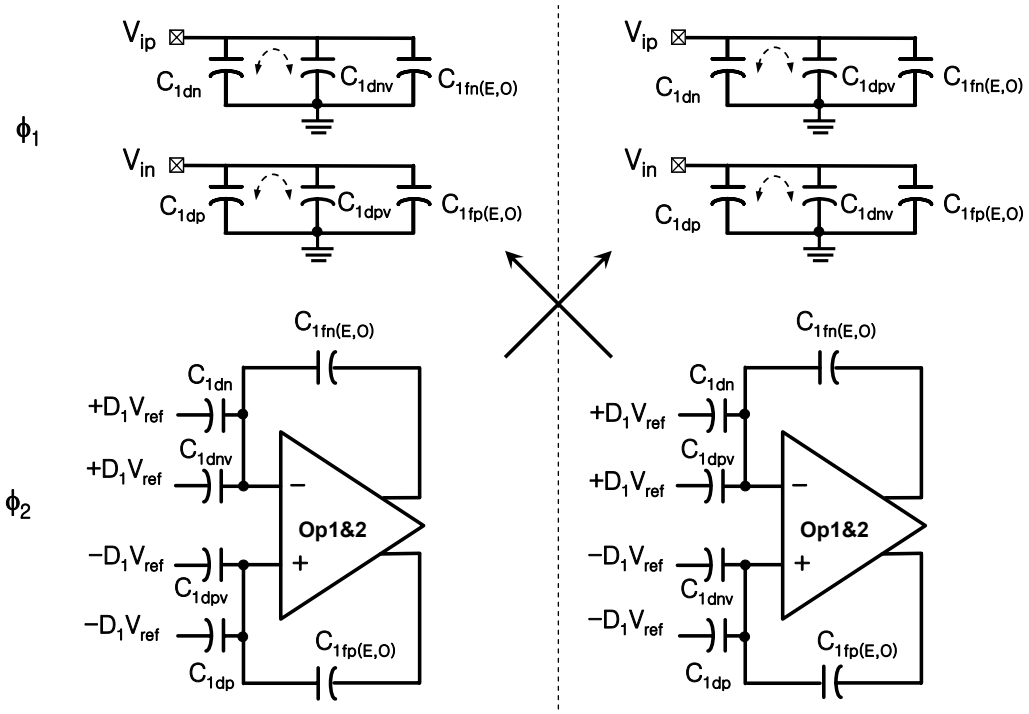

Figure 4: Resetting without extra clock phase

structure with gain boosting. The size of sampling capacitors and opamp current of each stage are shown in Fig. 5. Because our initial intent was for a higher resolution ADC, the capacitor values were over designed for the performance achieved. A proper redesign with reduced capacitor values would significantly reduce our present power consumption. Distributed clock generators are used to better optimize the load on the clock drivers.

V. Experimental Results

The prototype ADC was fabricated in a 0.18-µm CMOS process. The die photograph is shown in Fig. 7. The active die area is 1.2 mm x 1.8 mm. The total power consumption is 36mW at 1.8-V supply and 80-MHz sampling frequency. The analog portion consumes 24mW. The measured DNL and INL are -0.92/1.3 LSB and -3.11/3.06 LSB, as shown in Fig. 6. With 1MHz input at 80MS/s, the measured SFDR, SNR, and SNDR are 66.7dB, 57.6dB, and 53.2dB, respectively (see Fig. 8). The digital output of the ADC is decimated

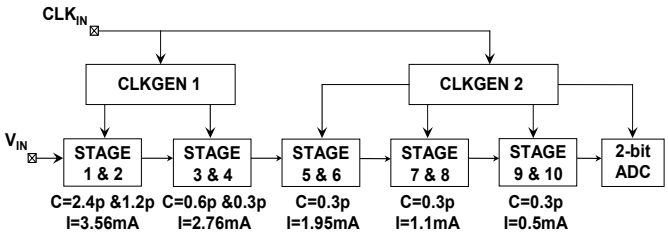

Figure 5: Block diagram of the ADC

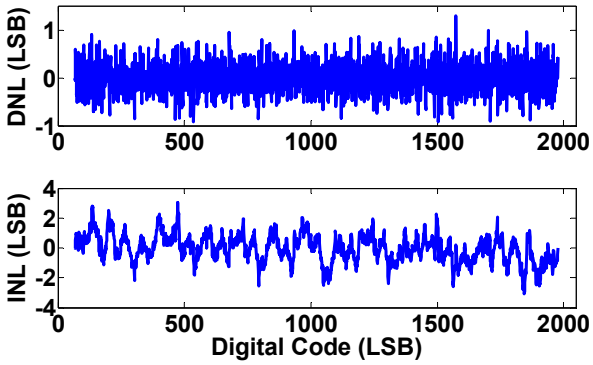

Figure 6: DNL and INL plots

(downsampled) by 4 on chip for testing purposes. Fig. 9 shows the dynamic performance versus input frequency at 80MS/s. The measured SFDR, SNR, and SNDR are 66dB, 58dB, and 53dB, respectively over the whole input range (1MHz to 50MHz). Fig. 10 shows the dynamic performance versus conversion/clock rate with 1MHz input signal. Fig. 11 shows the dynamic performance versus power supply with 1-MHz input signal. The ADC works well down to 1.6V.

VI. Conclusions

Capacitor sharing technique significantly reduces the effective load capacitance, thereby reducing the power consumption of an opamp. Capacitor sharing is found to be a suitable partner for opamp sharing. A new method to cancel the effect of signal-dependent charge kick-back in the absence of sample and hold was also presented.

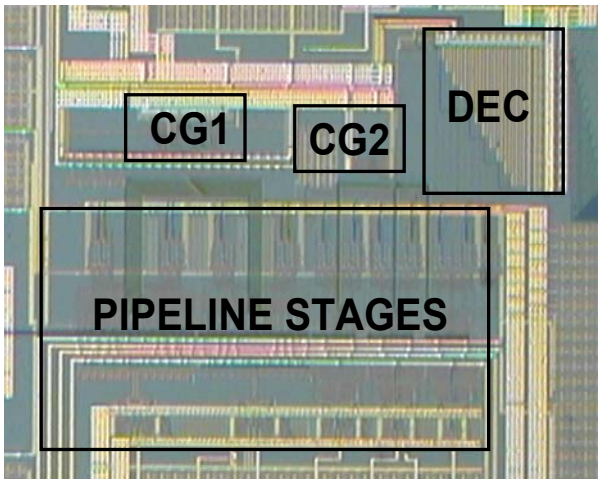

Figure 7: Die photograph

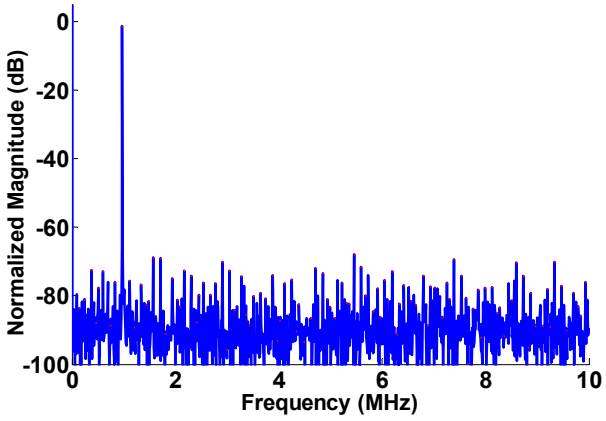

Figure 8: Measured signal spectrum at 80MS/s

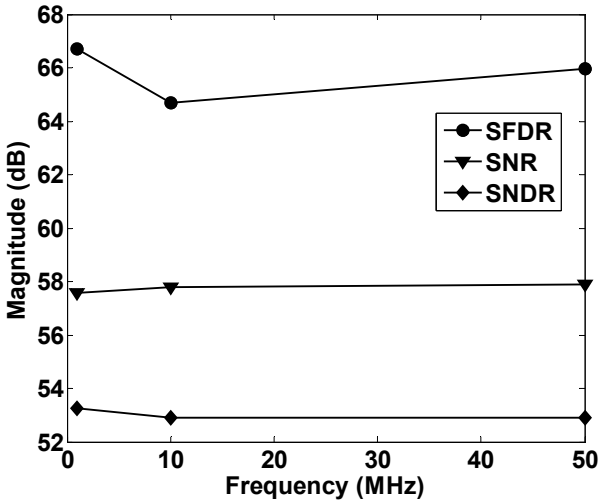

Figure 9: Measured dynamic performance versus input signal frequency

This was achieved via capacitor swapping to neutralize/reset the charge in the input capacitors between samples. The proposed techniques are suitable for low power and high speed pipelined ADC applications.

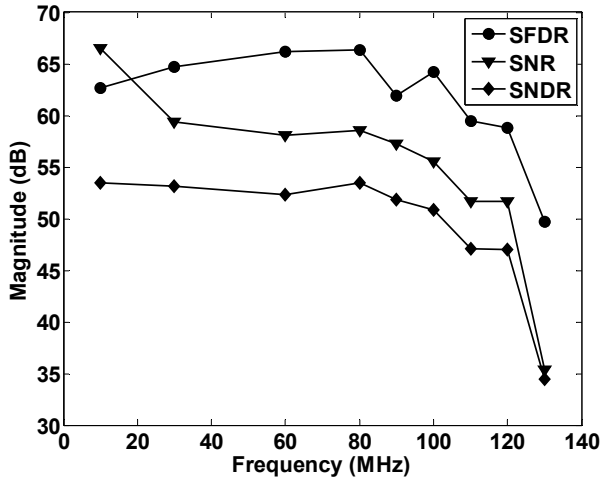

Figure 10: Measured dynamic performance versus conversion rate

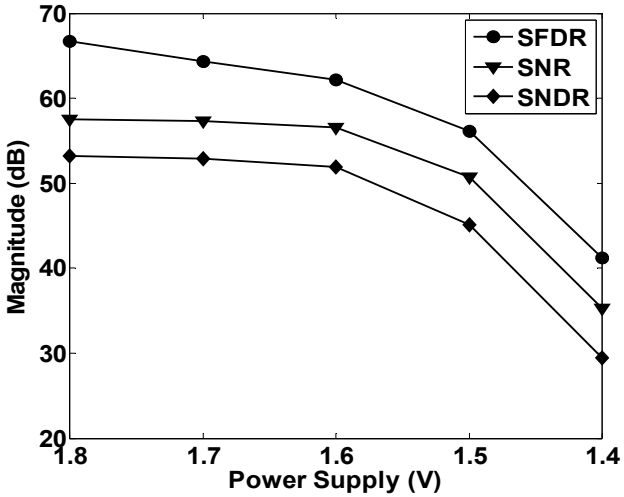

Figure 11: Measured dynamic performance versus power supply

ACKNOWLEDGEMENT

This work was supported by Asahi Kasei EMD Corporation, and partly by NSF CAREER CCR-0133530.

REFERENCES

[1] S. Lewis, H. Fetterman, G. Gross, R. Ramachandran, and T. Viswanathan, "A 10bit 20MS/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351-358, 1992

[2] D. Cline, and P. Gray, "A power optimized 13b 5MS/s pipelined analog-to-digital converter in 1.2µm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 294-303, 1996

[3] B. Min, P. Kim, F. Bowman, D. Boisvert, and A. Aude, "A 69mW 10bit 80MS/s pipleined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031-2039, 2003

[4] S. Malik, and R. Geiger, "Simultaneous capacitor sharing and scaling for reduced power in pipeline ADCs," *IEEE Midwest Symp. Circuits Syst.*, pp. 1015-1018, Aug. 2005

[5] J. Li, and U. Moon, "A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1468-1476, 2004