High-Speed Switched-Capacitor Filters Based on Unity Gain Buffers

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***Abstract*- In this work a new voltage buffer, the drain-follower, achieves 300MHz bandwidth with 2pF load, a dc gain of 0.993V/V, 1mV offset voltage, -60 dB total harmonic distortion at 1.4Vpp output voltage and 6.5mW power dissipation from 5V supply. A unity-gain buffer switched-capacitor biquad filter has been implemented in 0.5μm CMOS technology. The circuit has been sent for fabrication. Simulation results of the biquad filter indicate operation at 100MHz with 20mW power consumption from a 5V supply can be achieved.**

High-frequency operation of conventional switched-capacitor (SC) filters is limited by the need for high-gain, large-bandwidth opamps [1]-[3]. While it is possible to realize opamps with the required gain and bandwidth, power consumption becomes an issue [4],[5]. Realizing SC filters with unity-gain buffers rather than opamps may be a solution. A simple unity-gain buffer (UGB) can operate at very high-frequency with competitive power consumption.

Several buffers have been characterized to determine their applicability to unity-gain buffer SC filters. The primary metrics are gain, bandwidth and offset voltage. An ideal buffer will have a gain of unity, extremely large bandwidth and no offset voltage. Hspice simulations were performed using realistic CMOS models and load capacitance. It was found that the PMOS SF has the most desirable characteristics. While the PMOS SF suffers from large offset voltage (|Vgs|) and relatively low bandwidth (due to the lower mobility of holes) the other buffers tested exhibit poor gain and linearity primarily due to the body effect.

The body effect can be eliminated in the PMOS SF by tying the source to the n-well. Unfortunately the capacitive load introduced by the n-well reduces bandwidth. Bandwidth can be improved by inserting a buffer between the source and n-well which drives the additional load but maintains a constant n-well to source voltage, as shown in Fig. 1(a).

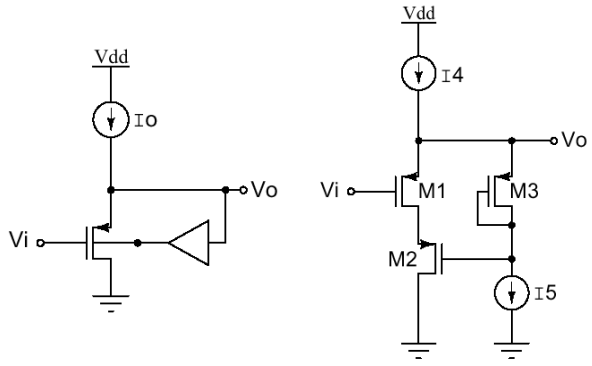

Fig. 1: PMOS Source Followers: (a) PMOS SF with n-well buffer; (b) cascoded PMOS SF.

Even with the elimination of the body effect in the PMOS SF the gain is still sufficiently below unity to degrade the accuracy of a filter. Neglecting the body effect the low frequency gain of a PMOS SF with active load can be derived as

$$\frac{V_o}{V_i} \cong \frac{gm_1\left(R_{o1} \parallel R_{o4}\right)}{gm_1\left(R_{o1} \parallel R_{o4}\right)+1}$$

A PMOS SF with a simple feedback network is shown in Fig. 1(b). The low frequency gain of this

circuit is

$$\frac{V_o}{V_i} \cong \frac{(1+gm_2R_{o2})gm_1R_{o1}}{(1+gm_2R_{o2})gm_1R_{o1}+1+gm_2R_{o1}R_{o2}\left(\frac{1}{R_{o4}}+\frac{1}{R_{o5}}\right)}$$

Again, the body effect has been neglected in the analysis. In Fig. 1(b) we see that transistor M1 is cascoded by M2 and the small signal analysis shows that this produces a $(g_mR_o)^2$ term in both the numerator and denominator, which brings the buffer gain very close to unity.

The SC integrator is a basic building block of many SC circuits. A unity-gain buffer SC integrator is shown in Fig. 2(b). Operation is as follows. During clock phase ϕ_1 the input voltage is sampled by C_1. During clock phase ϕ_2 C_1 is switched across the unity-gain buffer. If the offset voltage of the buffer is zero C_1 is fully discharged and C_2 acquires a charge of V_iC_1.

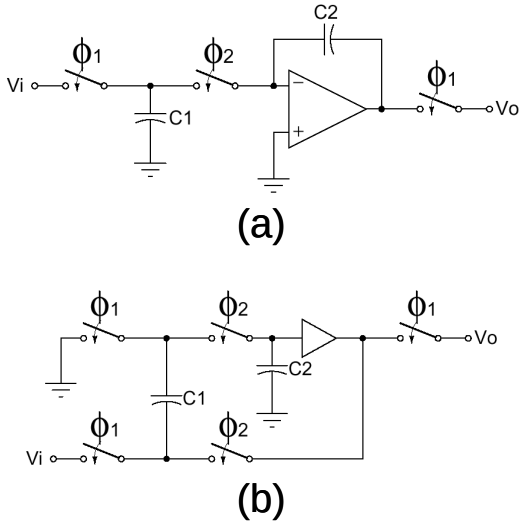

Fig.2: SC Integrators: (a) Conventional; (b) Unity-gain buffer.

Z-domain equations for the charge transfer during each clock phase can be solved to find the discrete time transfer function for each SC integrator shown in Fig.2, which is

$$H(z) \equiv \frac{V_o(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}.$$

One major drawback of UGB SC circuits is their sensitivity to stray capacitances between various circuit nodes and ground. These stray capacitances stem from transistor gates (buffer input), interconnect and source-drain diffusions of MOS switches. The effective buffer input capacitance for a typical buffer used in UGB SC circuits is $C_{gs}(1-A)$, where A is the gain of the buffer. For buffer gains close to unity this capacitance is negligible. The rest of this chapter deals with minimizing the effects of interconnect and source-drain diffusion capacitance.

Since damped integrators are used in both UGB SC ladder filters and UGB biquads, the analysis of a damped integrator with parasitic strays will give good insight as to how these strays effect filter accuracy and how to minimize the effect. Fig. 3 shows a damped UGB SC integrator with parasitic capacitors.

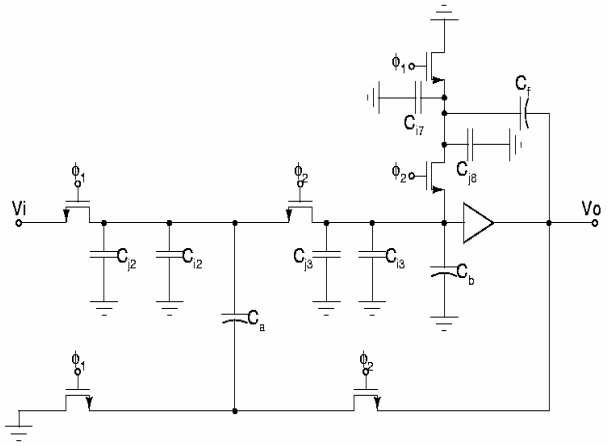

Fig.3: Damped unity-gain buffer SC integrator with stray capacitance.

C_{i2} is the interconnect capacitance between the top plate of C_a and ground, C_{j2} is the total diffusion capacitance between the top plate of C_a and ground, C_{i3} is the interconnect capacitance between the top plate of C_b and ground, C_{j3} is the total diffusion capacitance between the top plate of C_b and ground, C_{i7} is the interconnect capacitance

between the top plate of C_f and ground and C_{j8} is the total diffusion capacitance between the top plate of C_f and ground. The discrete-time transfer function of the circuit assuming a buffer gain of A is

$$H(z) = \frac{(C_a + C_{i2} + C_{j2})A}{(C_b + C_x + (C_a + C_f)(1-A))z - C_b + C_f A - C_{i3} - C_{j3}}$$

where

$$C_x = C_{i2} + C_{j2} + C_{i3} + C_{j3} + C_{i7} + C_{j8} .$$

The damped integrator magnitude response for all interconnect capacitors equal to 1fF, C_{j2} = 3fF, and $C_{j3} = C_{j8}$ = 10fF is shown in Fig. 4 where the effects of these stray capacitors are clear.

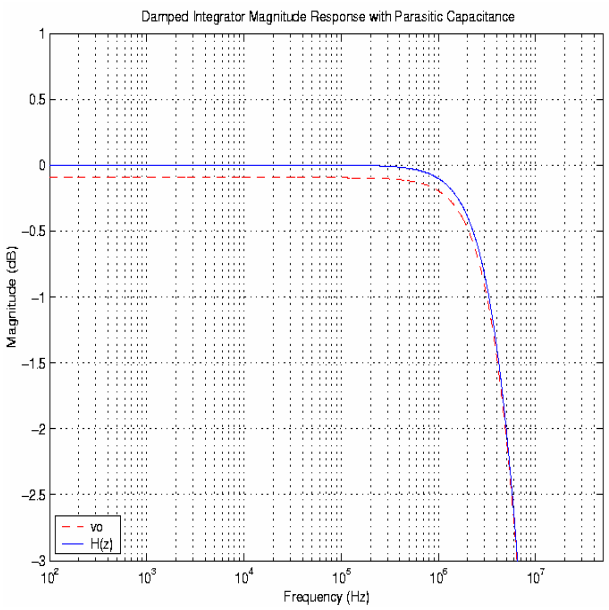

Fig. 4: Magnitude response of damped unity-gain buffer SC integrator with parasitic capacitance.

From the transfer function of the damped integrator we find the dc gain and pole location of the circuit to be

$$H(z)\big|_{z=1,A=1} = \frac{C_a + C_{i2} + C_{j2}}{C_f + C_{i2} + C_{j2} + C_{i7} + C_{j8}}$$

$$p_1 = \frac{C_b - C_f A + C_{i3} + C_{j3}}{C_b + (C_a + C_f)(1-A) + C_x} .$$

We can set the dc gain equation equal to the desired dc gain and solve for C_f in terms of C_a and the stray capacitance. Using this value for C_f will eliminate the error in the filter response due to the strays. The pole location can be adjusted in the same manner. Fig.5 shows the filter magnitude response after tuning where we see that the error due to the stays has been corrected. It should be noted that the diffusion capacitance associated with MOS switches is non-linear and can produce harmonic distortion, which is not corrected by the method of tuning presented here.

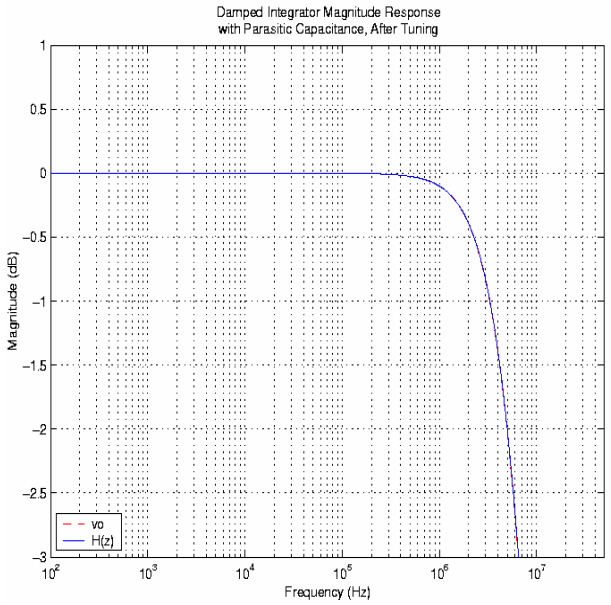

Fig. 5: Magnitude response of damped unity-gain buffer SC integrator with parasitic capacitance after tuning.

This method for reducing the effects of stray capacitance on the filter response depends heavily on how well we can estimate the value of the strays. Good process information is critical. Another method for reducing the stray interconnect capacitance is to run a poly or metal layer as a shield between the interconnect layer and the substrate [6]. The shield layer should be tied to the output of the buffer. The interconnect strays can be can be significantly reduced at the expense of additional load on the buffer. In most cases the

additional load on the buffer is negligible.

A second order low-pass filter with f_c/f_s=10 and constructed using unity-gain buffer SC integrators is shown in Fig. 6. Switcap was used to generate the magnitude response of the filter, which is shown in Fig. 7.

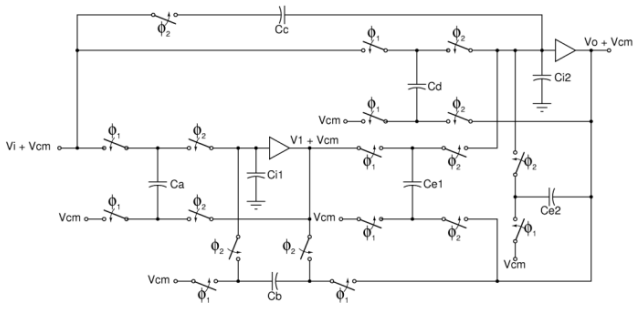

Fig. 6: Low-Q Unity-gain buffer biquad.

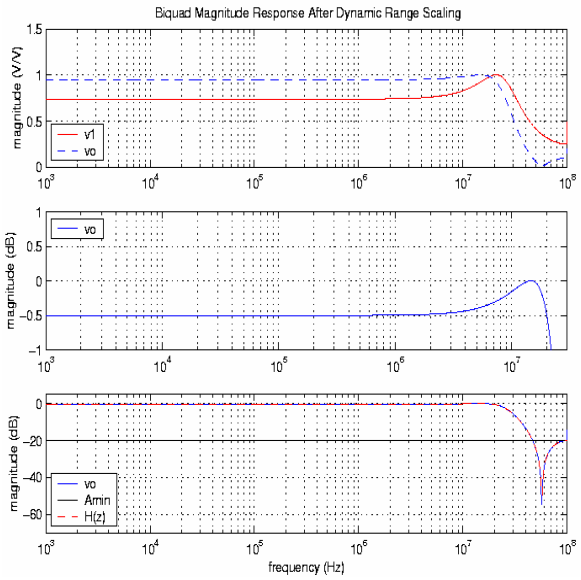

Fig. 7: Unity-gain buffer biquad magnitude response.

The unity-gain buffer Fig. 1(b) with the output taken at the drain of M_1 will be used in the filter since the very small offset voltage of this circuit eliminates the need for additional offset voltage compensation circuitry. Adrian Early with Cypress Microsystems recommended this change. The recommended changes are detailed in Fig. 8.

It uses NMOS devices to take advantage of their high mobility. Taking the output at the drain of M_1 does not significantly reduce the bandwidth because all nodes are low impedance. Additionally, body effect compensation is inherent in the circuit structure.

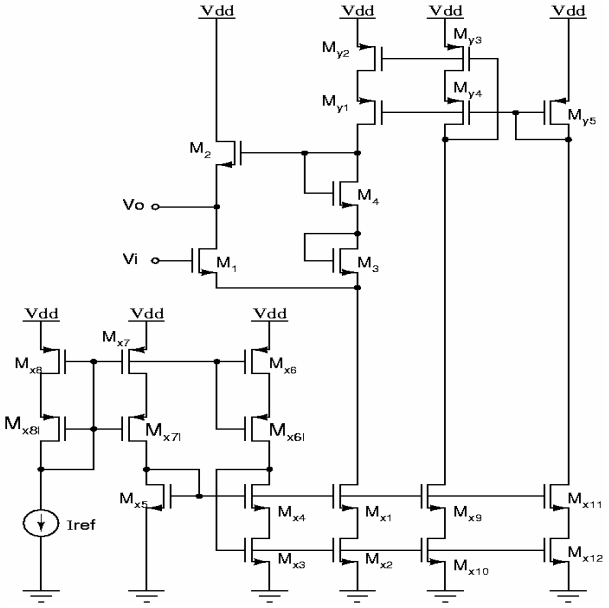

Fig. 8: NMOS Drain Follower.

Simulation results with a 2pF load show a 3-dB bandwidth of 300MHz, 0.992 DC gain and 1mV offset voltage. Power dissipation is 6.5mW from a 5V supply. A unity-gain buffer switched-capacitor biquad filter has been implemented in 0.5µm CMOS technology. The circuit has been sent for fabrication. Simulation results of the biquad filter indicate operation at 100MHz with 20mW power consumption from a 5V supply can be achieved.

Implementation	[6]	[7]	[8]	[9]	This work
Technology	3µm	2.5µm	3.5µm	0.5µm	0.5µm
Cut-off frequency (MHz)	0.22	0.185	1	20	10
Sampling frequency (MHz)	12	10	21	200	100
Power supply (V)	10	5	10	3	5
Power Consumption (mW)	5.7	18	165	10	20

Table 1. Comparison of unity-gain buffer filters.

The work presented in this thesis is compared to previous implementations in Table 1. An opamp based implementation [9] is included in the comparison to show how UGB SC filter designs perform versus conventional SC filter architectures. The conventional architecture seems to offer the best performance. It achieves a clock frequency of

200MHz and 10mW power consumption from a 3V supply using double-sampling techniques. The UGB SC biquad implemented here would benefit from more optimization, which would increase the performance of the circuit, making it a more viable option for discrete-time analog signal processing. If a double-sampling scheme is devised for UGB SC filters we will see an immediate doubling of the clock frequency with no increase in power consumption. Other areas for optimization are reducing or eliminating the effects of stray capacitors, eliminating the need for track-and-hold circuits and reducing power consumption.

References

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