Sub-1-V Design Techniques for High-Linearity Multistage/Pipelined Analog-to-Digital Converters

Dong-Young Chang, *Member, IEEE*, Gil-Cho Ahn, *Student Member, IEEE*, and Un-Ku Moon, *Senior Member, IEEE*

***Abstract*—The design of an ultra-low-voltage multistage (two-stage algorithmic) analog-to-digital converter (ADC) employing the opamp-reset switching technique is described. A highly linear input sampling circuit accommodates truly low-voltage sampling from external input signal source. A radix-based digital calibration technique is used to compensate for component mismatches and reduced opamp gain under low supply voltage. The radix-based scheme is based on a half-reference multiplying digital-to-analog converter structure, where the error sources seen by both the reference and input signal paths are made identical for a given stage. The prototype ADC was fabricated in a 0.18-μm CMOS process. The prototype integrated circuit dissipates 9 mW at 0.9-V supply with an input signal range of 0.9 V_{p-p} differential. The calibration of the ADC improves the signal-to-noise-plus-distortion ratio from 40 to 55 dB and the spurious-free dynamic range from 47 to 75 dB.**

***Index Terms*—Analog-to-digital converter (ADC), digital calibration, input sampling circuit, opamp-reset switching, pseudodifferential, ultra-low voltage.**

I. Introduction

CMOS technology has received much attention in the integrated circuits (ICs) arena due to a number of advantages for digital circuit implementation. These obvious advantages for digital circuit design naturally extends to all mixed-signal systems where both analog and digital circuits are compelled to co-exist on the same silicon die. Perhaps the most notable advantage of the CMOS process is its scalability. As the device feature size dramatically shrinks into deep submicrometer, the increasing integration density also leads to operating frequency improvement that results from transconductance enhancement and decreased stray capacitance. However, the shrinking device dimensions also implies proportional scaling of maximum supply voltage. Today's state-of-the-art CMOS process is already about to make transition below 1-V supply. This decreasing voltage headroom poses a significant challenge in the analog circuit design. Since analog circuits are routinely integrated with digital, most commonly as the interface between the real world, which is inherently analog, and the digital signal processor, it is highly desirable that all analog circuits adapt to the scaled lower supply voltages and operate reliably.

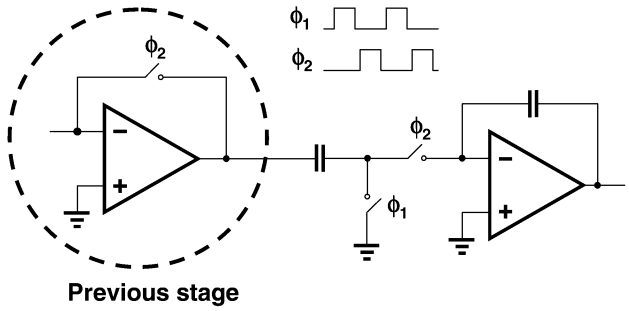

Fig. 1. ORST.

One class of circuits critically affected by this trend is the switched-capacitor (SC) circuits. SC circuits are used in many analog signal-processing building blocks for its naturally superior S/H function and good linearity. However, floating switches face a fundamental limitation in turning switches on/off under low supply condition. When V_{DD} is much larger than the sum of NMOS and PMOS absolute threshold voltages (in the complementary floating switch), it is easy to achieve large on-conductance for rail-to-rail signal swing. As V_{DD} starts to shrink, switch resistance and signal-dependent nonlinearity increase dramatically. In the case where V_{DD} finally gets smaller than the sum of the threshold voltages, there will be a signal range where the switch will no longer conduct.

There are several well-known methods to overcome this problem. The approaches include: 1) clock voltage boosting (e.g., $2V_{DD}$ clock) [1], [2], which cannot be used in submicrometer low-voltage CMOS processes as the gate oxide can only tolerate the technology's maximum voltage (V_{DD}); 2) using multithreshold MOSFETs [3], which are not always scalable to very low voltage supplies, as it could suffer from an unacceptable amount of leakage current (i.e., the switch may not fully turn off); 3) bootstrapped clocking [4]–[6], which has added loading and possible reliability issues; and 4) switched-opamp (SO) technique [7]–[10], which is fully compatible with low-voltage submicrometer CMOS processes, but the operating speed is limited due to slow transients from the opamp being switched off and on.[1]

The opamp-reset switching technique (ORST) has been proposed and applied to analog-to-digital converter (ADC) designs [12]–[14] providing reliable and fast low-voltage operation. The concept of the ORST is depicted in Fig. 1. After the previousstage output is sampled onto the sampling capacitor, the

Manuscript received January 3, 2004; revised June 3, 2004. This work was supported in part by the Center for Design of Analog-Digital Integrated Circuits under National Science Foundation CAREER Grant CCR-0133530 and by Analog Devices.

D.-Y. Chang is with Texas Instruments Incorporated, Tucson, AZ 85706 USA (e-mail: dychang@ti.com).

G.-C. Ahn and U. Moon are with the Department of Electrical and Computer Engineering, Oregon State University, Corvallis, OR 97331-3211 USA (e-mail: gcahn@ece.orst.edu; moon@ece.orst.edu).

Digital Object Identifier 10.1109/TCSI.2004.839532

[1]The SO technique have recently demonstrated high clocking speed at reduced accuracy [11].

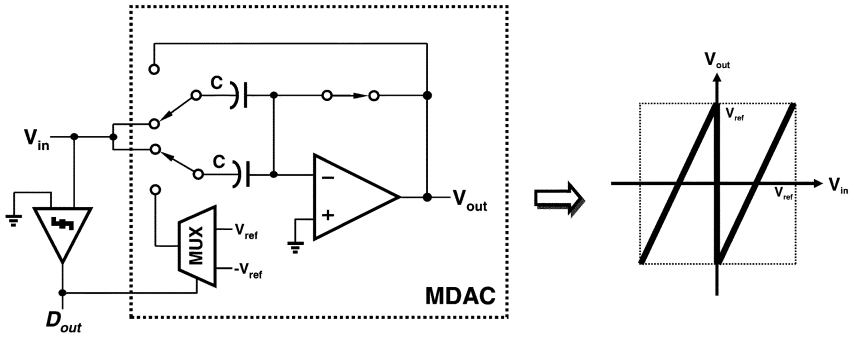

Fig. 2. Implementation of 1-bit-per-stage architecture.

sourcing opamp is placed into the unity-gain feedback configuration to provide a reset level. Since the opamp does not have to be switched off at any phase, a high-speed operation can be achieved.

In the ADC design, the overall linearity is often limited by the nonideal characteristics of analog building blocks. Under reduced/low supply voltage with limited signal headroom, the nonlinear effects are especially severe, resulting in degraded system performance. The digital calibration techniques have been recognized as one of the effective means to correct for these unavoidable limitations. In this paper, a radix-based digital calibration technique effective for multistage ADC is proposed. This technique is based on a multiplying digital-to-analog converter (MDAC) structure that uses a half-reference injection [15]. By merging the signal paths of both input and reference in a given MDAC, all nonideal factors within the MDAC stage are merged into a single equivalent error term that represents the radix number of the given stage. The ADC output is then digitally calibrated by applying the modified radix. It will be shown that the equivalent radix value/number can be extracted by forcing two different MSBs at the front-end stage while keeping the analog input fixed. The extracted radix numbers are further refined via a mathematical iteration/update algorithm. The proposed calibration technique is able to compensate for capacitor mismatches and finite opamp gain error. One of the key advantage of this technique is that the calibration accuracy is not bounded by the accuracy limitation of the converter itself.

In the following, we describe the design details of a two-stage algorithmic ADC. A two-stage algorithmic ADC is chosen because it represents a general form of multistage/pipelined ADCs, and the hardware is minimal compared to a nonrecycling pipelined ADC. A two-stage algorithmic ADC has two distinct nonlinear error values (one for each stage), and it cannot be reduced down to a single radix system, as in single-stage (effectively) algorithmic ADC [22]. The low-voltage design technique (incorporating enhanced ORST), as well as the radix-based digital calibration technique are applied to the prototype ADC. This prototype IC design also employs a highly linear input sampling circuit at the front-end. The prototype IC verification from this two-stage algorithmic ADC makes the proposed study generally applicable to all multistage pipelined ADCs. In Section II, the design limitations of a single-bit-per-stage ADC architecture are reviewed. Section III summarizes the radix calibration technique based on a half-reference MDAC. Section IV covers low-voltage circuit implementation details of key ADC building blocks. The prototype IC measurement results are summarized in Section V, followed by concluding remarks in Section VI.

II. Single-Bit-Per-Stage ADC Architecture

Fig. 2 illustrates the conceptual block diagram of a single-bit-per-stage ADC architecture in its simplest form. The block diagram is based on an SC MDAC where the "capacitor-flip-over" structure is commonly used. After the analog input is sampled onto the bottom plates of both sampling capacitors, one of the capacitors flips over to the output, while the other one is connected to either $+$ or $-V_{\rm ref}$ depending on the 1-bit digital output of the comparator (single-bit flash ADC). This results in the following input-to-output relationship:

$$V_{\rm out} = 2 \cdot \left(V_{\rm in} + D \cdot \frac{V_{\rm ref}}{2} \right) \tag{1}$$

where $D = -1$ for $V_{\rm in} > 0$ and $D = +1$ for $V_{\rm in} < 0$. As briefly discussed in Section I, the circuit would face a serious floating switch problem under low-voltage conditions if the MDAC in Fig. 2 is implemented as is. The ORST provides an elegant solution on this problem. In a previous low-voltage MDAC design, the ORST was employed by using a separate reference sampling capacitors instead of reusing one of the two sampling capacitors for reference sampling [12]. Since all switches are to be connected to either very high (V_{DD}) or very low GND voltage potential to avoid the floating switch problem, the appropriate reference level could only be provided by controlling the capacitor ratio between the sampling capacitor and the dedicated reference capacitor. This implies a wide spread of capacitance values, which hampers matching accuracy in the MDAC.

This paper presents a "half-reference" MDAC incorporating ORST, as shown in Fig. 3. During the sampling phase (ϕ_1), both $\pm V_{\rm ref}/2$ (depending on sub-ADC decision level) and the analog input are sampled onto the top and bottom plates of the sampling capacitor, respectively. During the amplification phase (ϕ_2), the top plate of the capacitor is connected to the virtual ground of the opamp, while the bottom plate is reset (ORST operation) by the sourcing amplifier of the previous stage. Assuming ideal conditions, the residue voltage of (1) is obtained. In reality, there exists important static error terms in the MDAC. They are capacitor mismatch (denoted by α) and finite opamp

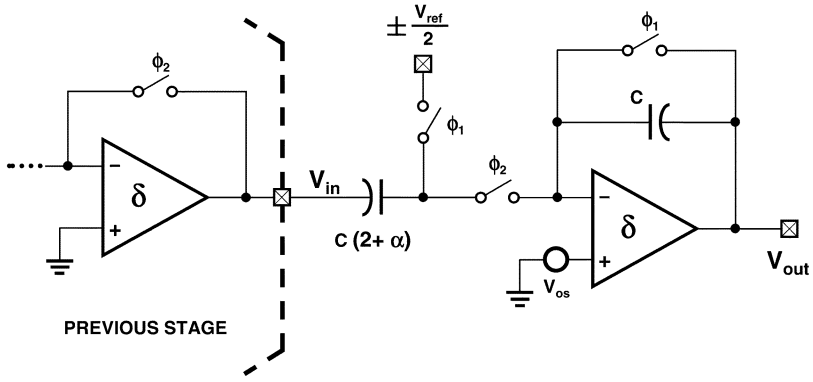

Fig. 3. Low-voltage half-reference MDAC.

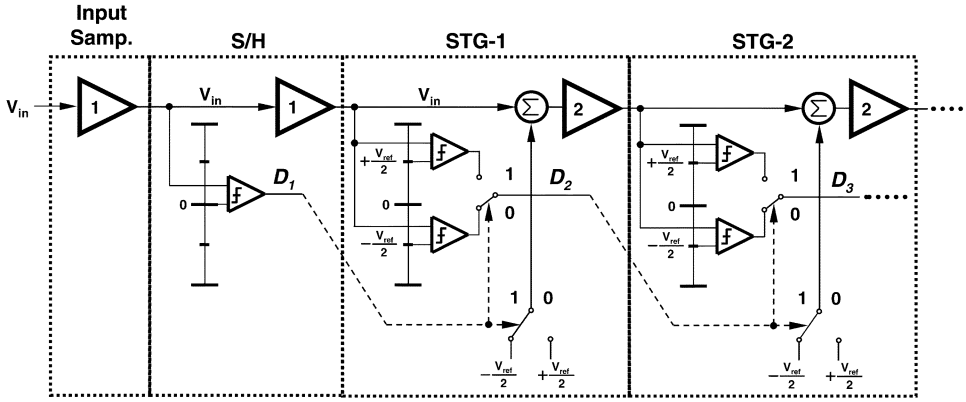

Fig. 4. Conceptual block diagram of a bit-lookahead scheme.

dc gain error (denoted by δ), which directly contribute to critical ADC linearity error. The details of the correction/calibration of these error terms are discussed in Section III. The offset (denoted by $V_{\rm os}$) can also degrade the dynamic range or lead to ADC linearity error if it is not fully absorbed by the digital redundancy/correction. When these error terms are included, the residue voltage expression changes to

$$V_{\rm out} = (2+\alpha)(1+\delta)\cdot\left(V_{\rm in} + D\cdot\frac{V_{\rm ref}}{2}\right) + \underbrace{(3+\alpha)(1+\delta)\cdot V_{\rm os}}_{O}. \quad (2)$$

The finite dc gain error term (δ) resulting from the combination of capacitor mismatch (α) and opamp dc again A is

$$\delta = -\frac{3+\alpha}{3+\alpha+A}. \quad (3)$$

Constant offset term (O) in (2) does not affect the overall linearity of the ADC unless the offset is big enough to push the transfer curve in Fig. 2 out of the reference range (bounded by the dotted $V_{\rm ref}$ line) where the analog information would be lost. The lost information, namely, missing decision levels, is not reconstructible. To ensure no missing decision levels occur, the interstage gain is to be made less than two. This is commonly referred to as the sub-radix conversion system. In this way, a limited amount of shift in the transfer function could be allowed while all information is preserved, transferred, and reconstructed by the remaining stages. In other words, the sub-radix conversion system is just one form of realization for digital redundancy/correction, implementations of which have many variations.

Another important point to be considered in this MDAC structure is the operation timing. In a conventional pipelined ADC, the sub-ADC's bit decision is made after (at the end) the input signal sampling phase. This implies that the input and $\pm V_{\rm ref}/2$ cannot be sampled during the same clock phase. Therefore, the low-voltage structure of Fig. 3 requires a bit-lookahead configuration to move the comparator decisions a half clock cycle (one phase) ahead. This is shown in Fig. 4. Instead of comparators deciding polarity of the present stage input, the ADC looks ahead to the next stage signal polarity by shifting the reference points of the comparator by $+$ and $-V_{\rm ref}/2$ [16]. This will result in two digital outputs in each stage. The valid data between the two is selected by the previous stage's digital output. In order to allow for this reference shifting, the ADC requires another sample-and-hold (S/H) function to follow the front-end input sampling. To align the operation, the additional S/H generates a half clock cycle delay in the sampled $V_{\rm in}$ after the signal polarity has been decided.

III. Radix-Based Digital Calibration Technique for Multistage ADC

A. Radix-Based Calibration

The block diagram of the half-reference MDAC (from Fig. 3) is shown in Fig. 5. Assuming all capacitors are matched perfectly and all opamps have infinite open-loop gain, the recon-

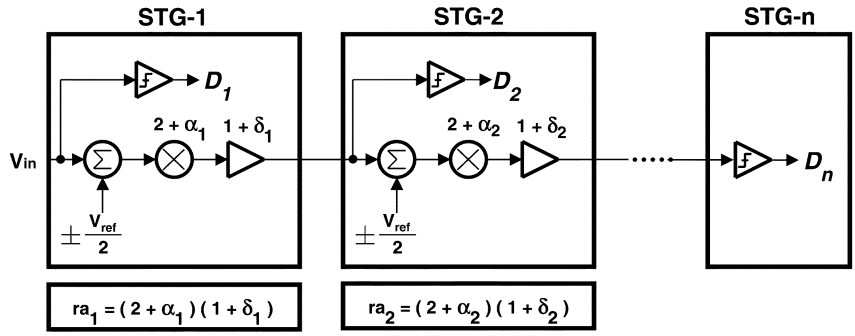

Fig. 5. Block diagram of a proposed multistage ADC using the half-reference MDAC.

structed digital output D_{out} (quantized analog output) can be calculated as follows:

$$D_{\text{out}} = \sum_{k=0}^{n-1} D_{n-k} \cdot (2)^k. \tag{4}$$

However, in the presence of the two error terms (α_i and δ_i), (4) no longer provides a linear relationship.

One of the effective ways to improve linearity of the ADC is to apply self-calibration in the digital domain. The key concept of most digital calibration techniques usually relies on measuring error terms by the converter itself. The measured values are either directly subtracted from the digital output and curve fitted to the ideal transfer curve [17]–[20] or the ADC is self-linearized using the extracted errors [21], [22]. A technique similar to our radix-based calibration reported in [22] is applicable to single-stage ADCs only. The calibration technique based on the half-reference MDAC described below can be generalized to any number of stages in a multistage/pipelined ADC design.

One of the most important characteristics in the half-reference structure is that the $V_{\text{ref}}/2$ is directly subtracted from the input on the same capacitor before it is amplified. The net result is that both input and reference $(V_{\text{ref}}/2)$ see the same multiplying factor (which has error). In this way, the two different nonideal factors are merged into an interstage gain mismatch term, which represents the equivalent radix of the stage. As a result, the digital output can now be calibrated with a simple modified radix calculation [15]. The reconstructed/calibrated digital output D_{out} can be calculated as follows:

$$D_{\text{out}} = D_n + D_{n-1} \cdot (\text{ra}_{n-1}) + D_{n-2} \cdot (\text{ra}_{n-1})(\text{ra}_{n-2}) + \cdots + D_1 \prod_{k=1}^{n-1} \text{ra}_k \tag{5}$$

where $\text{ra}_i = (2+\alpha_i)(1+\delta_i)$. One of the key advantages of this technique is that it accounts for nonlinear factors of all conversion stages such that the calibrated output will not be affected by component inaccuracies.

B. Calibration of a Two-Stage Algorithmic ADC

In the prototype IC realization of this study, a two-stage algorithmic ADC is chosen, representing the simplest form of a multistage ADC, to illustrate the ADC calibration. A simplified schematic/block diagram is shown in Fig. 6. It consists

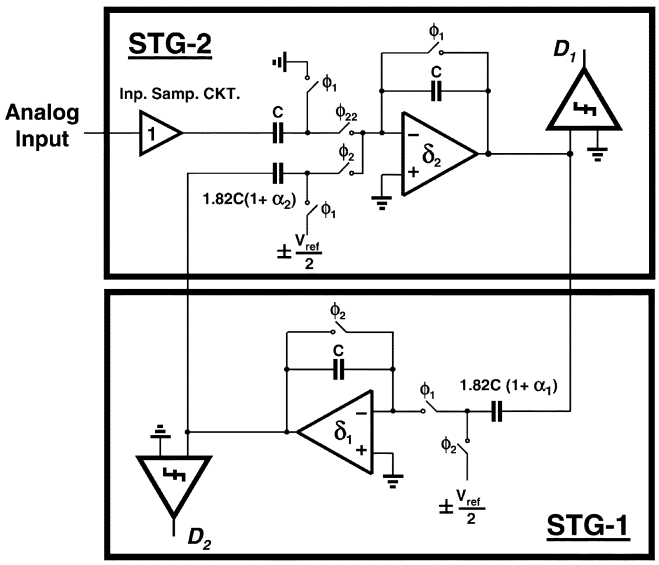

Fig. 6. Two-stage algorithmic ADC.

of a front-end input sampling circuit, which tracks and transfers the external signal to the ADC, and the two conversion stages STG-1 and STG-2. During the first conversion cycle, the tracking signal from the input sampling circuit is transferred to STG-1 by S/H operation of STG-2 (during ϕ_{22}). This generates a half clock period delay for the bit-lookahead operation, which, for simplicity, is omitted in Fig. 6. In addition, the held signal provides fully settled signal from the tracking signal to STG-1. Each conversion stage includes a half-reference MDAC using ORST for low-voltage operation and a comparator providing a single-bit digital output. The 12-bit word output is generated after seven clock cycles (14 phases) operation. Thus, the sampling rate is seven times slower than the clock frequency. The ADC's 12-bit output word is then reconstructed by

$$\begin{aligned} D_{\text{out}} = \underbrace{D_{12}}_{\text{LSB}} &+ D_{11} \cdot (\text{ra}_1) + D_{10} \cdot (\text{ra}_1)(\text{ra}_2) \\ &+ D_9 \cdot (\text{ra}_1)^2(\text{ra}_2) + D_8 \cdot (\text{ra}_1)^2(\text{ra}_2)^2 \\ &+ \cdots + \underbrace{D_1}_{\text{MSB}} \cdot (\text{ra}_1)^6(\text{ra}_2)^5 \end{aligned} \tag{6}$$

where ra_1 and ra_2 are equivalent radices for STG-1 and STG-2, respectively. To allow for enough digital redundancy, the interstage gain is set to 1.82 in this ultra-low-voltage implementation.

C. Radix Measurement and Calibration

In this calibration, all error terms should first be measured accurately. The accuracy of the measurement determines the overall ADC resolution. The primary difficulty is that the exact radix for each stage cannot be known in advance. With the calibration sequence described below, initial estimated values iterate to the final correct values mathematically using an incremental calculation loop.

The biggest discontinuities of the ADC transfer curve occur at the points where the MSB changes from zero to one. In a radix-2 system (standard binary system), this discontinuity can be extracted by injecting "1" and "0" digital bits to the MSB stage with zero analog input. For example, in the ideal situation, if "1" is forced with zero analog input then the residue results in $-V_{\rm ref}$ and the resulting ADC output would be $1000\cdots00$ (MSB "1" is the forced bit). When "0" is forced under the same condition, the residue would be $V_{\rm ref}$, which leads to the ADC output of $0111\cdots11$ (MSB "0" is the forced bit). Although the ADC is converting the same mid-level analog input of 0 V, the difference in quantized value between the two output results in 1-LSB. Since there is no digital redundancy between stages, no output bit (digital) correction takes place. Given the residue voltage of full $\pm V_{\rm ref}$ (due to "bit forcing"), when the error terms resulting from the nonidealities are considered in ADC design, digital redundancy should be employed to prevent missing decision levels, as discussed above. In this case, forcing the MSB of "1" and "0" will only change the residue signal path. Since the digital outputs are inherently corrected by the digital redundancy, the nominal/statistical difference between the two quantized values will be 0-LSB. With this known/desired value of 0-LSB, the estimated radix numbers $({\rm ra}_i)$ can now be corrected by an incremental update algorithm

$$ {\rm ra}_i[n+1] = {\rm ra}_i[n] - \Delta \cdot \epsilon_i[n] \tag{7}$$

where ϵ is the difference between the two quantized output after the MSBs are forced, n is the iteration index, and Δ is update step size. Each word is calibrated using the current estimate of ${\rm ra}_1$ and ${\rm ra}_2$. The two radices are updated alternately until the mathematical iteration comes to an end. The measurement/calibration details are described below.

The first step is to measure ${\rm ra}_1$. MSB of "1" is forced to STG-1 and the analog input is set to zero. The resulting residue is

$$ V_A = -({\rm ra}_1) \cdot \frac{V_{\rm ref}}{2}. \tag{8}$$

The ADC itself then digitizes V_A during the remaining conversion cycles to produce a 12-bit digital word D_A.[2] This digital word D_A includes "1" forced MSB. Next, MSB of "0" is forced to STG-1 to obtain the residue

$$ V_B = ({\rm ra}_1) \cdot \frac{V_{\rm ref}}{2} \tag{9}$$

which is also digitized to a 12-bit digital word D_B (forced MSB "0" included). Note that V_A and V_B define the upper and lower reference level of STG-2. The ϵ_1 can now be calculated as follows:

$$ \epsilon_1 = D_{\rm out}(D_A) - D_{\rm out}(D_B) \tag{10}$$

where $D_{\rm out}$ is calculated (reconstructed) using (6).

The ϵ_2 measurement for ${\rm ra}_2$ is done in a similar manner by effectively exchanging the roles of STG-1 and STG-2. The two resulting residues from STG-2 during the bit-forcing sequence also redefine the full-scale input range of STG-1. Once the measurements are completed for ϵ_1 (for ${\rm ra}_1$) and ϵ_2 (for ${\rm ra}_2$), (7) is used to mathematically update the radix values ${\rm ra}_1$ and ${\rm ra}_2$. Since the overall ADC range is composed of the combination of the two radices, they are updated alternately based on one another's latest values until the overall transfer function is fully linear (i.e., ϵ_i approaches zero). The update/iteration loop is purely mathematical once the four digital words are taken/measured from the ADC/hardware.

[2]Even though we are keeping with 12-bit conversion for consistency in the explanation, a higher number of bits can be used to increase the accuracy of calibration measurement.

IV. Circuit Design

A. Low-Voltage Input Sampling Circuit

One of the most challenging tasks in the low-voltage ADC design is to sample/transfer the front-end input signal fast and accurately from sources external to the IC. One such circuit exists in the context of the SO technique [23]. A modified structure incorporating our ORST operation is shown in Fig. 7. To emphasize the voltage *potential*, the reference voltages are expressed as V_{DD} and GND. During the reset phase (ϕ_2), V_{xp} is pulled up to V_{DD}, while C_1 is precharged to V_{DD} and C_2 discharged. During the amplification phase (ϕ_1), V_{xp} becomes $V_{DD}/2$ (i.e., a fixed/battery reference $V_{\rm batt}$) due to charge sharing between C_1 and C_2. V_{xp} acts as an intermediate virtual ground. Assuming that the input common-mode voltage is $V_{DD}/2$, the output common-mode voltage also becomes $V_{DD}/2$. During ϕ_2 (ignoring the body effect for simplicity), the resistance of the PMOS switch MPP is

$$ R_{\rm MPP} = \frac{1}{\beta[(V_{SG} - |V_{TH}|) - V_{SD}]} \tag{11}$$

where $\beta = \mu_p C_{OX}(W/L)$. The voltage division between R_1 and $R_{\rm MPP}$ introduces nonlinear voltage fluctuation at V_{xp}

$$ V_{xp} = \left(\frac{R_2' R_{\rm MPP}}{R_1 R_2' + R_1 R_{\rm MPP} + R_2' R_{\rm MPP}}\right) V_{\rm INP} + \left(\frac{R_1 R_2'}{R_1 R_2' + R_1 R_{\rm MPP} + R_2' R_{\rm MPP}}\right) V_{DD} \tag{12}$$

where $R_2' = R_2 + 1/g_{m\_{\rm opamp}}$. Due to this nonlinear resistance $R_{\rm MPP}$, signal distortion results. The level-shifting voltage $V_{\rm batt}$ becomes a function of V_{xp}, and $V_{\rm OUTN}$ becomes a function of $V_{\rm batt}$. Assuming that the opamps have finite, but linear open-loop gain A, those voltages are given by

$$ V_{\rm batt} = \frac{V_{xp}(C_1 + C_2) - (C_1 V_{DD} + C_2 {\rm GND})}{C_1 + C_2} \tag{13}$$

$$ V_{\rm OUTN} = \left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)\right)^{-1} \cdot \left(\left(1 + \frac{R_2}{R_1}\right) V_{\rm batt} - \left(\frac{R_2}{R_1}\right) V_{\rm INP}\right). \tag{14}$$

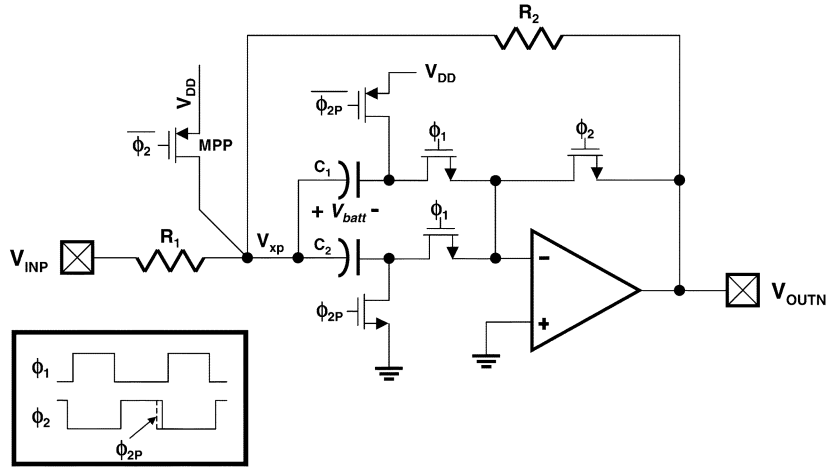

Fig. 7. Conventional input sampling circuit.

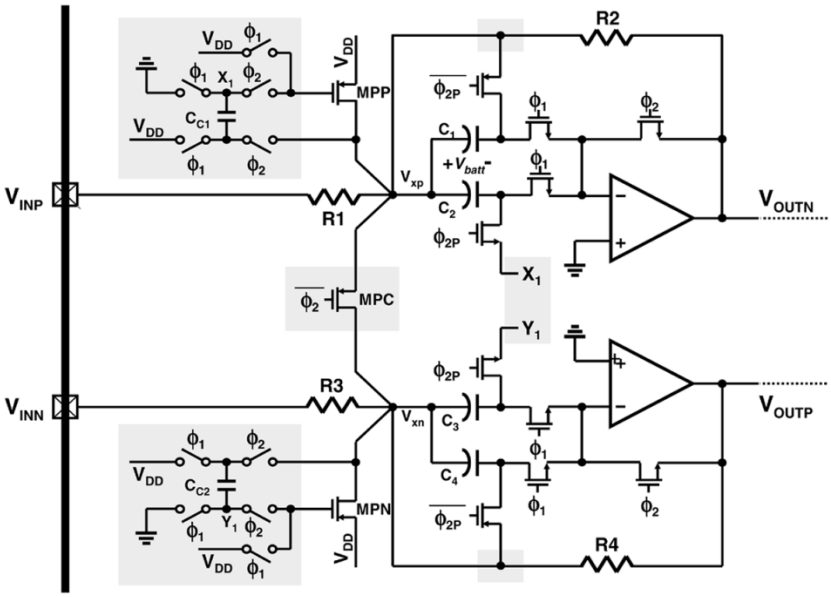

Fig. 8. Proposed input sampling circuit.

It can be observed that the output harmonic-distortion results from the signal-dependent distortion at V_{xp} caused by $R_{\rm MPP}$ nonlinearity.

Three design techniques are proposed to minimize this nonlinearity problem. They are depicted in the shaded areas of Fig. 8. As required for the ultra-low-voltage operation of ORST, the design incorporates the pseudodifferential architecture. During ϕ_2, the capacitor C_{C1}, which was precharged to V_{DD} during the previous clock phase, is connected between the PMOS gate and V_{xp} so that the gate voltage of the MPP would track the variation of V_{xp}. This makes $R_{\rm MPP}$ constant

$$R_{\rm MPP} = \frac{1}{\beta(V_{DD} - |V_{TH}|)}. \tag{15}$$

Note that V_{xp} is slightly lower than V_{DD} during ϕ_2, and X_1 may go below GND, which can cause a latch-up condition. Careful design requires proper sizing of C_{C1} with respect to C_1 and C_2. We have used $C_{C1} = 4$ pF and $C_1 = C_2 = 2$ pF in this design. To cancel the remaining distortion at the output, V_{xp} and X_1 are sampled to C_1 and C_2, respectively, instead of sampling V_{DD} and GND. In doing so, the nonlinear fluctuation at V_{xp} is further cancelled during the tracking phase

$$\begin{aligned} V_{\rm batt} &= \frac{V_{xp}(C_1 + C_2) - (C_1 V_{xp} + C_2(V_{xp} - V_{DD}))}{C_1 + C_2} \\ &= \frac{C_2 V_{DD}}{C_1 + C_2}. \end{aligned} \tag{16}$$

The output voltage is no longer a function of V_{xp} or $R_{\rm MPP}$, but a linear function of $V_{\rm INP}$ only

$$\begin{aligned} V_{\rm OUT\,N} = &\left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)\right)^{-1} \\ &\cdot \left(\left(1 + \frac{R_2}{R_1}\right)\left(\frac{C_2 V_{DD}}{C_1 + C_2}\right) - \left(\frac{R_2}{R_1}\right) V_{\rm INP}\right). \end{aligned} \tag{17}$$

Since the devices/elements will never match perfectly in circuit implementation, incorporating both techniques will minimize distortion. Another straightforward way to improve the linearity of $R_{\rm MPP}$ is to increase the device size so that the fluctuation at

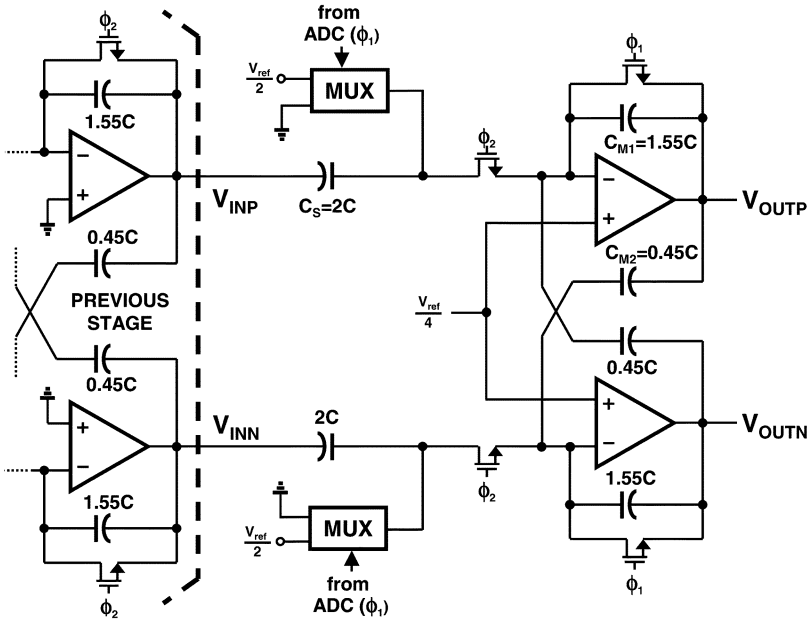

Fig. 9. Schematic of the MDAC.

$V_{xp}(V_{xn})$ can be as small as possible. However, this proportionally increases the device area. As in a previous design, we have incorporated a differential resetting switch MPC [12]. The differential resetting switch can be made half the size of MPP and MPN, and will achieve the same result as doubling the sizes of MPP and MPN. More importantly, using MPC also helps to suppress even harmonics that are due to device mismatches in the two pseudodifferential signal paths. This is because MPC provides a differentially stable V_{DD} reference level to both V_{xp} and V_{xn} during the reset phase.

Simulation results of the conventional (Fig. 7) and proposed (Fig. 8) circuits in SPECTRE indicate that the THD levels in the range of a -40-dB level (conventional) improves to a -100-dB level performance in the proposed design. The measurement results of the prototype ADC presented in Section V confirm the effectiveness of this input sampling circuit.

B. MDAC

The schematic of the low-voltage half-reference MDAC is depicted in Fig. 9. It employs the ORST in a pseudodifferential configuration. If the pseudodifferential architecture is applied without an effective common-mode feedback (CMFB) circuit, any common-mode voltage errors entering the cascaded stages would accumulate with multiplication of the MDAC gain. This is because the pseudodifferential configuration inherently performs a single-ended operation, resulting in the common-mode gain that is the same as the differential gain. Building a traditional CMFB circuit under such low voltage while using no floating switches is a challenging task. In this study, we get around the problem of adding a traditional CMFB circuit by incorporating a mild positive feedback with C_{M2} [12]. This configuration provides the differential gain of

$$A_{\mathrm{DIFF}} = \frac{C_S}{(C_{M1} - C_{M2})} = 1.82 \tag{18}$$

while the common-mode gain is kept to

$$A_{\mathrm{CM}} = \frac{C_S}{(C_{M1} + C_{M2})} = 1. \tag{19}$$

Thus, once the common-mode voltage at the front-end is set to $V_{DD}/2$, it is retained throughout the conversion cycles without the addition of a complex CMFB circuitry.

For an ADC reference range of 0.9-V peak-to-peak differential under the supply voltage of 0.9 V, $\pm V_{\mathrm{ref}}/2$ reference implies ± 0.1125-V single-ended swing from the mid-level $V_{DD}/2$ ($= 0.45$ V). This makes reference sampling impossible due to the switch overdrive problem. In this design, the center voltage of the reference swing is shifted down to 0.1125 V. Therefore, $\pm V_{\mathrm{ref}}/2$ can be realized by differential sampling of 0.225 V and GND. With the virtual ground of the opamp also set to 0.1125 V, there is no net shift in the reference common-mode level.

There are two factors that cause missing decision levels. They are: 1) opamp offset voltage in the MDAC and 2) the comparator offset in the sub-ADC. The interstage gain made less than two (sub-radix system) is expected to provide enough digital redundancy between stages. To avoid extreme reduction of the interstage gain, the opamp offset is suppressed sufficiently at the circuit level. This is shown in Fig. 10. The offset level is sampled onto the storing capacitor (C_{off}) during the sampling phase. During the amplification phase, actual offset voltage and the precharged value are cancelled out by setting the V_X node to ground potential. Although only differential offset $(V_{\mathrm{os1}} - V_{\mathrm{os2}})$ matters in the MDAC, this technique suppresses absolute offsets for both positive and negative signal paths at the same time. To reject the offset efficiently, C_{off} should be made much larger than the parasitic capacitance at the virtual ground node. On the other hand, the offset should fully charged C_{off} during a half clock cycle. In this MDAC, this tradeoff led to a C_{off} value of 10 pF. This technique is made possible because one node of the virtual ground pair is always available in the pseudodifferential

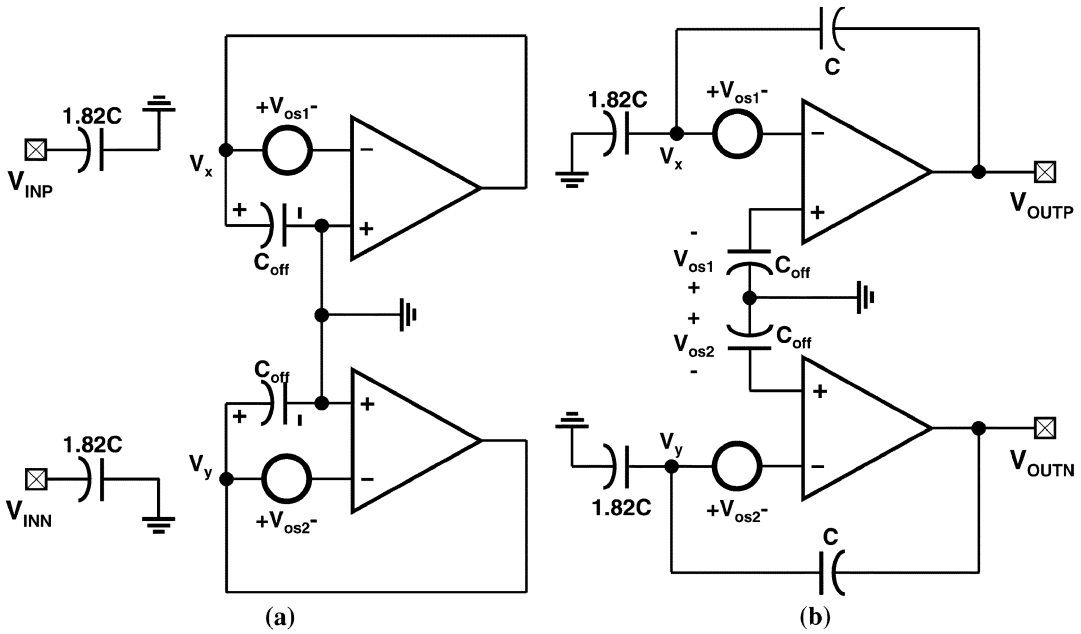

Fig. 10. Pseudodifferential offset cancellation. (a) Offset sampling. (b) Offset cancellation.

configuration. Section IV-C will describe the details of comparator offset compensation.

Finally, we also propose a solution to a small drawback in the MDAC incorporating ORST. In the ORST operation, the opamp loop dynamics experience a feedback factor difference between the sampling/reset and amplification modes. This is because the opamp has to be placed in the unity-gain feedback configuration during the sampling/reset phase. If the difference is drastic, the opamp would have to be overcompensated to cover a wide range of loop bandwidths. This would end up being an unnecessary burden on the circuit design. As shown in Fig. 11, an additional switch is used where it provides a controlled resistance between the opamp virtual ground and the signal ground during the sampling phase. It can be made twice the size of the feedback/reset switch so that the reset mode feedback factor is the same or similar to that of the amplification mode (feedback factor of $\approx$1/3).[3] This assures good and consistent phase margin and settling dynamics during all phases. In addition, the signal ground is set to the same potential as the virtual ground such that there would be a negligible (≈ 0) amount of dc current flowing through the switches. One small drawback here is that any offset voltage appearing at the virtual ground node will be amplified and transferred to the next stage during the reset phase. However, the pseudodifferential offset cancellation (Fig. 10) suppresses the offset voltage, and any remaining amount of offset amplified are small/negligible and signal independent.

C. Comparator

The comparator in the sub-ADC is composed of a preamplifier followed by a latch, as shown in Fig. 12, with all floating switches having been eliminated. The analog input signal is

[3]This generic description in reality is oversimplified because the resistive network/load to ground will effectively reduce the open-loop gain of the opamp. One needs to consider the effectively reduced open-loop dc gain in conjunction with the feedback factor that establish loop stability/dynamics.

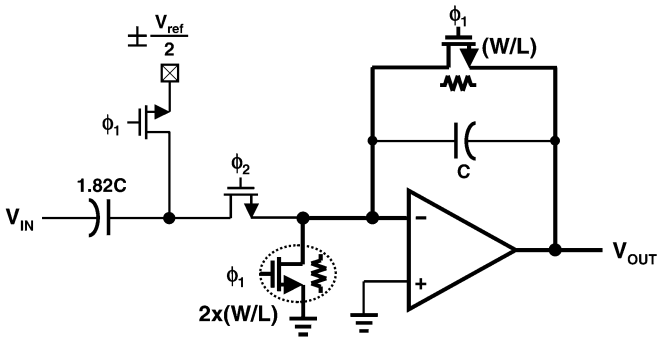

Fig. 11. Feedback factor control in the ORST.

compared to $V_{\rm ref}/2$. One of the most critical aspects of comparator design is the minimization of the input-referred offset. Among numerous offset cancellation methods, the two most common approaches are based on the input offset storage (IOS) and the output offset storage (OOS) [24]. The IOS is also referred to as the auto-zeroing technique. The main idea involves the comparator storing the offset voltage at the input sampling capacitor by placing the preamplifier in the unity-gain feedback configuration and cancelling it out during the comparison/amplification phase. However, the ISO would not be a good choice in the ultra-low-voltage design because of the need for the feedback switches, which need to transfer differential offset centered at $V_{DD}/2$. In this design, the OOS is employed to bypass this floating switch problem.

The detailed operation is shown in Fig. 13. During the sampling phase (ϕ_2), the offset of the sourcing amplifier from the previous stage MDAC ($V_{\rm osa}$), which is the excess error term after the pseudodifferential offset cancellation, is removed initially by cross-coupled sampling. Therefore, effectively zero voltage is charged to C_1. At the same time, the offset of the preamplifier ($V_{\rm os}$) is amplified by the preamplifier gain of A and sampled onto C_2. To produce proper input common-mode

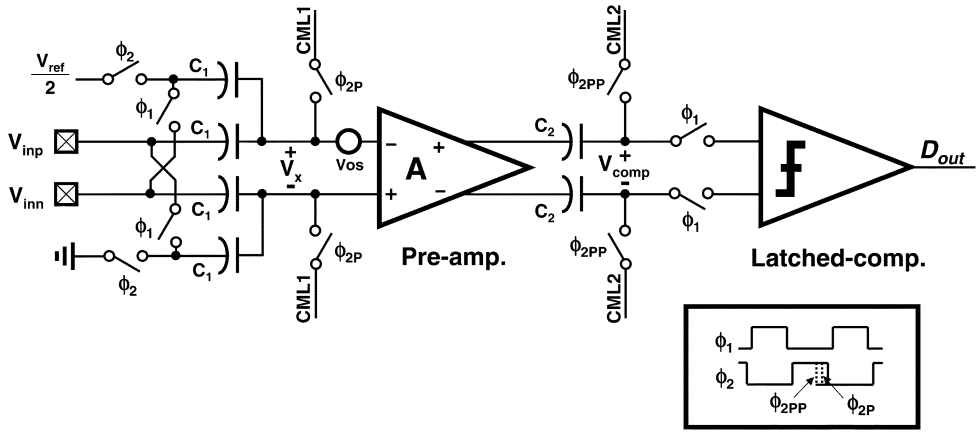

Fig. 12. Schematic of the comparator.

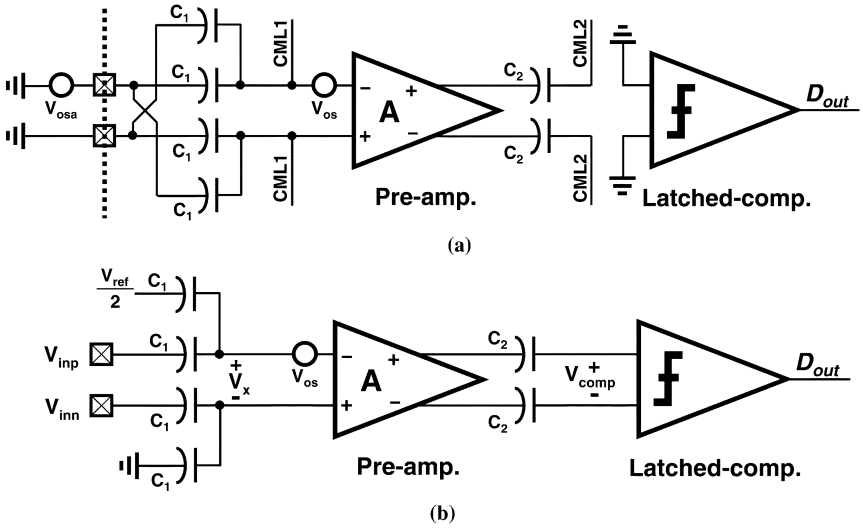

Fig. 13. OOS of the comparator. (a) Sampling phase. (b) Comparison phase.

levels for the preamplifier and the latch (both with NMOS input pairs), CML1 and CML2 are set to 0.2 V. Although CML1 and CML2 have the same potential, they should be biased separately. While C_2 samples the offset at the falling edge of ϕ_{2PP}, C_1 can still sample the reset voltage at ϕ_{2P} without interruption.

During the comparison/amplification phase (ϕ_1),

$$V_x = V_i - \frac{V_{\rm ref}}{2} - V_{\rm os} \tag{20}$$

where $V_i = V_{\rm INP} - V_{\rm inn}$. When V_x is amplified and sampled onto C_2,

$$V_{\rm comp} = A \cdot \left(V_i - \frac{V_{\rm ref}}{2} - V_{\rm os} \right) + A \cdot V_{\rm os} = A \cdot \left(V_i - \frac{V_{\rm ref}}{2} \right). \tag{21}$$

In the end, $V_{\rm comp}$ is a function of V_i and $V_{\rm ref}/2$ only. One important thing should be considered in deciding the preamplifier gain A. If A is too big, $AV_{\rm os}$ will go out of the preamplifier output swing range and offset information will be lost. If A is too small, then a large amount of offset voltage from the latch will be referred to the preamplifier input. Considering this tradeoff, the gain A is set to eight in this design. C_1 and C_2 are sized 200 fF.

V. Measurement Results

The die photograph of the prototype IC is shown in Fig. 14. The active die area is 1.2 mm $\times$ 1.2 mm. The input sampling circuit is at the lower left-hand-side corner followed by the two converting stages located side by side to minimize signal crossing. The chip is implemented in a 0.18-μm CMOS process with a threshold voltage of $\approx$0.45 V for both NMOS and PMOS. The prototype ADC is characterized for signal-to-noise-plus-distortion ratio (SNDR) and spurious-free dynamic-range (SFDR) based on a fast Fourier transform (FFT) of measured data. The differential nonlinearity (DNL) and the integral nonlinearity (INL) errors are measured based on code-density test. ICs are characterized at the power supply voltage of 0.9 V and the input range of 0.9 V_{p-p} differential. When different supply voltages are used, the reference range is also adjusted to have the same peak-to-peak differential input range as the supply. Due to reduced radix and digital truncation error, the prototype is rescaled to 10-bit (binary/radix-2) level,

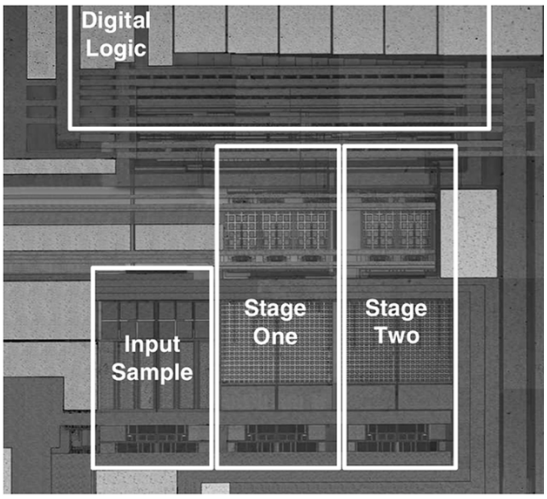

Fig. 14. Die photograph of the prototype ADC.

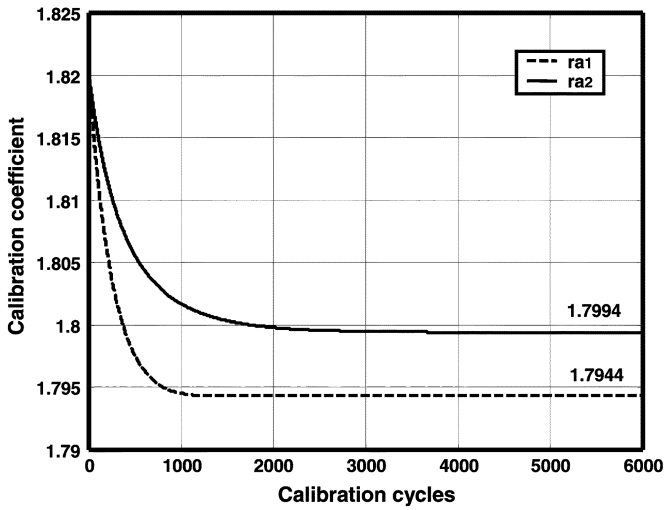

Fig. 15. Measured iteration steps of radices.

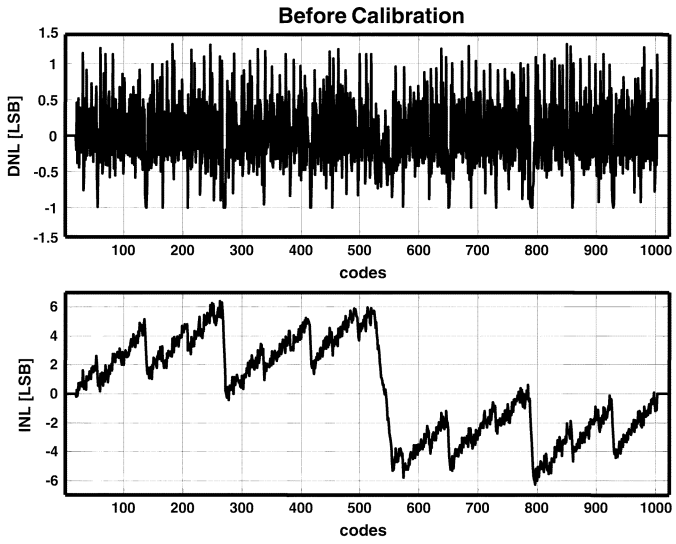

Fig. 16. DNL and INL before calibration.

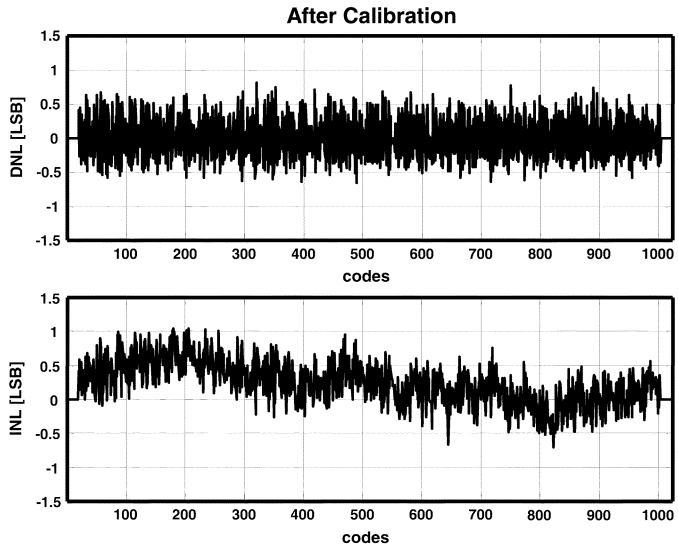

Fig. 17. DNL and INL after calibration.

although the ADC output is a 12-bit sub-radix 1.82 word (effectively 10.4-bit binary).[4] The digital calibration/recalculation is done externally (software).

Before any static and dynamic measurements of the ADC are made, the precise radix of each stage was first measured and calculated. After the digital words were extracted/measured for calibration (as described in Section III), mathematical iteration steps refined the radix number from the initial value of 1.82, as shown in Fig. 15. The update step size of 2^{-14} was used for the iteration. The final values/radices change under different supply, conversion speed, and bias condition due to varying settling behavior and dc gain variation of the opamp. All measured results in the following were obtained after the radix measurements/iterations based on each test condition.

The code density measurements are done at the 10-bit level. A total of 2^{16} samples was collected with a sampling rate of 1 MSPS and an input signal of 15 Hz at 0.9-V supply. Typical DNL and INL plots are shown in Figs. 16 and 17 for before and after calibration, respectively. The results before calibration shows peak DNL and INL errors of $1.4/-1.0$ LSB and $6.3/-6.2$ LSB, respectively. The DNL value of -1 LSB implies missing codes, which result in large INL jumps at major transition codes. After calibration, DNL and INL improved to $0.8/-0.65$ LSB and $1.05/-0.7$ LSB, respectively. There are no missing codes and most of the major carry jumps are removed in the INL plot.

Fig. 18 shows the output spectrum at 0.9-V supply. A full-scale input sine wave of 50 kHz with sampling rate of 1 MSPS were used. Before calibration, SFDR of 47 dB and SNDR of 40 dB were obtained. After calibration, all tones are reduced below a -75-dB level (SFDR) and SNDR improved to 55 dB. It can be concluded that SNDR is dominated by noise level rather than harmonic distortion after calibration. Fig. 19 shows the dynamic measurement results under different supply voltages, but with the same bias condition. This demonstrates that the SFDR is better than 80 dB at 1.2-V supply. This implies that more headroom in signal swing results in improved signal distortion. In this measurement setup, the peak-to-peak differential input

[4]This results from $(1.82)^{12} = 2^N$ leading to $N = 12 \cdot \log(1.82)/\log(2) = 10.367$ effective binary bits.

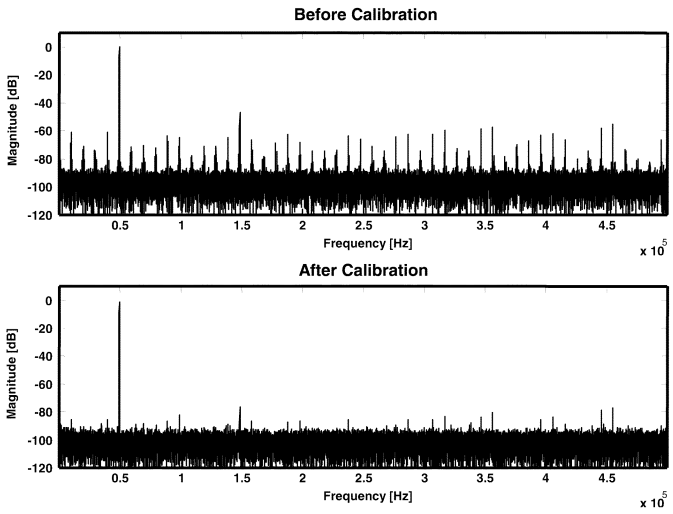

Fig. 18. ADC output spectra at $V_{DD} = 0.9$ V.

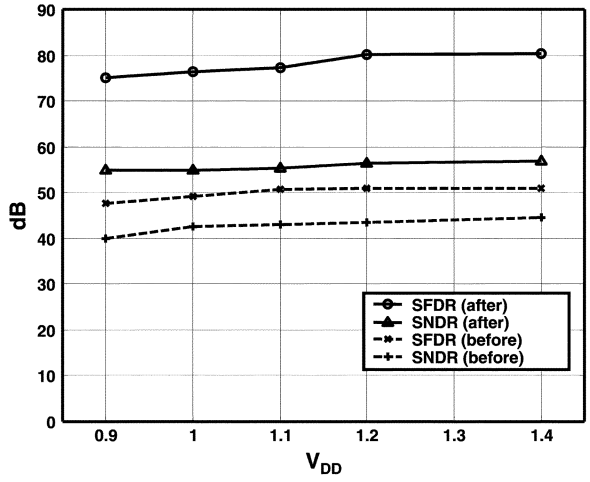

Fig. 19. Measured dynamic performance versus V_{DD}.

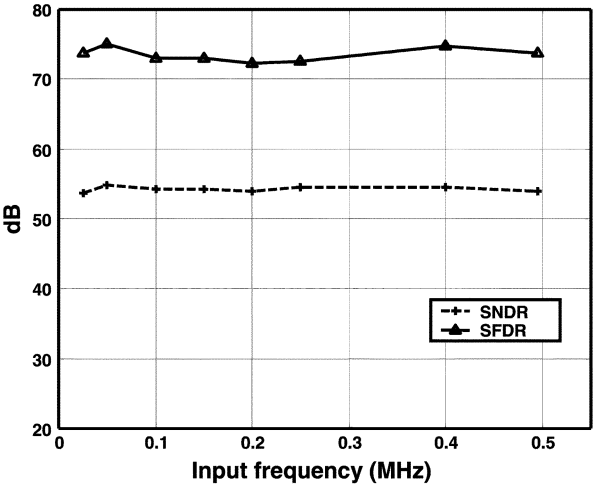

Fig. 20. Dynamic performance versus f_{in} at $V_{DD} = 0.9$ V.

range was set equal to the supply voltage. Fig. 20 shows that the ADC performs consistently up to the Nyquist rate. These measurement results also imply that the input sampling circuit

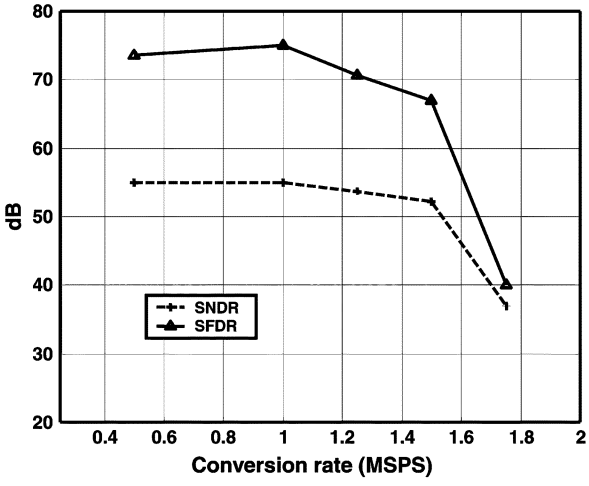

Fig. 21. Dynamic performance versus f_s at $V_{DD} = 0.9$ V.

TABLE I
MEASUREMENT SUMMARY

Technology	0.18μm CMOS
Resolution	10.4 binary bits (12 bits of radix-1.82)
Chip size	1.2mm×1.2mm
Supply voltage	0.9 V
Conversion rate	1 MSPS (clock=7 MHz)
Power consumption	9 mW (at 0.9V)
DNL	1.4 LSB / 0.8 LSB (cal.)
INL	6.3 LSB / 1.05 LSB (cal.)
SNDR	40 dB / 55 dB (cal.)
SFDR	47 dB / 75 dB (cal.)

is sufficiently linear (i.e., performs at least better than 80-dB linearity level at 1.2 V independent of input signal frequency). Dynamic performance versus clock rate is also summarized in Fig. 21. The ADC performs up to 1.5 MSPS with consistent performance. The total power dissipation of the ADC is 9 mW at 0.9-V supply. The overall performance of the ADC is summarized in Table I.

VI. CONCLUSION

The design of an ultra-low-voltage (0.9 V) two-stage algorithmic ADC has been presented. For effective low-voltage operation, the ORST has been used. In addition to very low-voltage operation, the prototype IC realization requirements have been fulfilled by a number effective design techniques. These include: 1) a highly linear input sampling circuit; 2) a radix-based MDAC structure incorporating bit-lookahead scheme; 3) an iterative scheme for refining of measured radix error; 4) pseudodifferential offset cancellation schemes for MDAC and a comparator; and 5) robust feedback control for improved stability. Fabricated in a 0.18-μm CMOS process, the prototype IC dissipates 9 mW at 0.9-V supply, demonstrating 10-bit 1-MSPS performance. It has a differential peak-to-peak input range of 0.9 V and occupies a 1.2 mm × 1.2 mm die area. While the challenges of true low-voltage analog design in future submicrometer CMOS continue to be difficult obstacles ahead, our design example provides a new milestone for a sub-1-V operation in Nyquist pipelined ADCs.

ACKNOWLEDGMENT

The authors would like to thank the personal support of S. Ju and B. Chatterjee, and National Semiconductor, for providing fabrication of the prototype IC.

REFERENCES

[1] T. Cho and P. Gray, "A 10 b 20 Msamples/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[2] J. Wu, Y. Chang, and K. Chang, "1.2 V CMOS switched-capacitor circuits," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 1996, pp. 388–389.

[3] T. Atachi, A. Ishinawa, A. Barlow, and K. Taksuka, "A 1.4 V switched capacitor filter," in *IEEE Proc. Custom Integrated Circuits Conf.*, May 1990, pp. 821–824.

[4] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14 MS/s CMOS pipeline analog-to-digital converter," in *IEEE VLSI Circuits Symp.*, Jun. 1998, pp. 166–169.

[5] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Delta\Sigma$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.

[6] J. Steensgaard, "Bootstrapped low-voltage analog switches," *Proc. IEEE Int. Circuits Syst. Symp.*, vol. II, pp. 29–32, May 1999.

[7] J. Crols and M. Steyaert, "Switched opamp: An approach to realize full CMOS SC circuits at very low supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936–942, Aug. 1994.

[8] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900-mV low-power A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.

[9] A. Baschirotto and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1979–1986, Dec. 1997.

[10] M. Waltari and K. Halonen, "1-V 9-bit pipelined switched-opamp," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 129–134, Jan. 2001.

[11] V. Cheung, H. Luong, and W. Ki, "A 1-V 10.7-MHz switched-opamp bandpass $\Delta\Sigma$ modulator using double-sampling finite-gain-compensation technique," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1215–1225, Oct. 2002.

[12] D. Chang and U. Moon, "A 1.4-V 10-bit 25 MSPS pipelined ADC using opamp-reset switching technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1401–1404, Aug. 2003.

[13] D. Chang, G. Ahn, and U. Moon, "A 0.9 V 9 mW 1 MSPS digitally calibrated ADC with 75 dB SFDR," *IEEE VLSI Circuits Symp.*, pp. 67–70, Jun. 2003.

[14] M. Keskin, U. Moon, and G. Temes, "A 1-V 10-MHz clock-rate 13-bit CMOS $\Delta\Sigma$ modulator using unity-gain-reset opamps," *IEEE J. Solid-State Circuits*, vol. 37, pp. 817–823, Jul. 2002.

[15] D. Chang and U. Moon, "Radix-based digital calibration technique for multi-stage ADC," *IEEE Int. Circuits Syst. Symp.*, vol. II, pp. 796–799, May 2002.

[16] T. Matsuura *et al.*, "A 240-Mbps, 1-W CMOS EPRML read-channel LSI chip using an interleaved subranging pipelined A/D converter," *IEEE J. Solid-State Circuits*, vol. 33, no. 11, pp. 1840–1850, Nov. 1998.

[17] S. Lee and B. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, Dec. 1992.

[18] H. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE J. Solid-State Circuits*, vol. 29, pp. 509–515, Apr. 1994.

[19] U. Moon and B. Song, "Background digital calibration techniques for pipelined ADC's," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 44, pp. 102–109, Feb. 1997.

[20] S. Kwak, B. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1866–1875, Dec. 1997.

[21] A. Karanicolas and H. Lee, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, Dec. 1993.

[22] O. Erdogan, P. Hurst, and S. Lewis, "A 12-b digital-background-calibrated algorithmic ADC with -90-dB THD," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1812–1820, Dec. 1999.

[23] A. Baschirotto, R. Castello, and G. Montagna, "Active series switch for switched-opamp circuits," *Electron. Lett.*, vol. 34, no. 14, pp. 1365–1366, Jul. 1998.

[24] B. Razavi and B. Wooley, "Design techniques for high-speed high-resolution comparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, Dec. 1992.

Dong-Young Chang (S'00–M'04) received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1995 and 1997, respectively, and the Ph.D. degree in electrical and computer engineering from Oregon State University, Corvallis, in 2002.

In 1997, he joined Samsung Electronics, Kiheung, Korea, where he was engaged in the design of analog front-end systems for charge-coupled device (CCD)/CMOS image sensors and LCD displays. During Summer 2000, he was with Bell Laboratories, Lucent Technologies, Allentown, PA, where he investigated various low-voltage data converters. Since January 2003, he has been with Texas Instruments Incorporated, Tucson, AZ, where he is involved with low-power high-speed ADC products. His research has focused on low-voltage and low-power analog and mixed-mode ICs. He holds three U.S. patents.

Dr. Chang was the recipient of the 1998 Outstanding Student Paper Award presented by the IEEE Solid-State Circuits Seoul Chapter and the 2000 Outstanding Student Designer Award presented by Analog Devices.

Gil-Cho Ahn (S'94) received the B.S. and M.S. degrees in electrical and electronics engineering from Sogang University, Seoul, Korea, in 1994 and 1996, respectively, and is currently working toward the Ph.D. degree in electrical engineering at the Oregon State University, Corvallis.

From 1996 to 2001, he was a Design Engineer with Samsung Electronics, Kiheung, Korea, where he was involved with mixed analog-digital ICs. His current research interests include high-speed high-resolution data converters and low-voltage low-power mixed-signal circuit design.

Mr. Ahn was the recipient of the Analog Devices Outstanding Student Designer Award in 2004.

Un-Ku Moon (S'92–M'94–SM'99) received the B.S. degree from University of Washington, Seattle, in 1987, the M.Eng. degree from Cornell University, Ithaca, NY, in 1989, and the Ph.D. degree from the University of Illinois at Urbana-Champaign, in 1994, all in electrical engineering.

From February 1988 to August 1989, he was a Member of Technical Staff at AT&T Bell Laboratories, Reading, PA. From August 1992 to December 1993, while with the University of Illinois at Urbana-Champaign, he taught a microelectronics course. From February 1994 to January 1998, he was a Member of Technical Staff at Lucent Technologies Bell Laboratories, Allentown, PA. Since January 1998, he has been with Oregon State University, Corvallis. His interest has been in the area of analog and mixed analog–digital ICs. His past work has included highly linear and tunable continuous-time filters, telecommunication circuits including timing recovery and ADCs, and SC circuits.

Prof. Moon has served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING. He currently serves as an Associate Editor of the IEEE TRANSACTIONS ON SOLID-STATE CIRCUITS since January 2005. He also serves as a member of the IEEE Custom Integrated Circuits Conference Technical Program Committee and Analog Signal Processing Program Committee and Analog Signal Processing Program Committee of the IEEE International Symposium on Circuits and Systems. He was a recipient of the National Science Foundation CAREER Award in 2002, and the Engelbrecht Young Faculty Award from Oregon State University College of Engineering in 2002.