Radix-Based Digital Calibration Techniques for Multi-Stage Recycling Pipelined ADCs

Dong-Young Chang, *Member, IEEE*, Jipeng Li, *Member, IEEE*, and Un-Ku Moon, *Senior Member, IEEE*

***Abstract*—This paper describes a digital-domain self-calibration technique for multistage pipelined analog-to-digital converters (ADCs). By making the signal paths of both the input and the reference voltage the same, all error factors within a stage are merged into a single term which represents the equivalent radix number. The initially estimated radix for each stage mathematically iterates to the final correct value via an incremental update algorithm, after foreground calibration measurements are obtained during ADCs recycling mode of operation. In this way, an accurate calibration is achieved using a modified radix-based calculation. Two different single-bit-per-stage ADC adaptation/calibration methods are presented as examples. The proposed technique compensates for linear errors such as capacitor mismatches as well as finite opamp gain.**

***Index Terms*—Analog-to-digital converter (ADC), multistage ADC, pipelined recycling, radix-based digital calibration.**

I. Introduction

THE increasing demand for high-resolution analog-to-digital converters (ADCs) has stimulated many innovative design solutions. These solutions seek to overcome the finite accuracy set by the analog building blocks. Because of the inevitable limitations of analog components in integrated circuits (ICs), data converter resolution is bound to 10–12 effective number of bits (ENOB). It is primarily due to a variety of calibration techniques that recent development of data converters are able to fulfill the high-resolution requirements of modern data conversion systems. The calibration techniques of these ADCs may be placed into three categories: analog-domain calibration (including circuit level linearity enhancement techniques) [1]–[10]; digital-domain calibration [11]–[16]; and calibration by trimming (typically internal capacitors or laser-trimmed thin-film resistors) [17]–[19]. The analog-domain techniques usually require additional circuitry such as opamps and extra digital-to-analog converters (DACs) for calibration. Sometimes they need extra clock phases to do the job. These methods imply slower conversion speed and increased power consumption. These are the reasons why the focus is shifting from analog to digital techniques for calibration.

The digital calibration techniques have received more attention in the recent years because they do not require manual modification or extra analog circuitry. The key concepts of these techniques rely on measuring component mismatches by the converter itself. The measured error values are either directly subtracted from the digital output [11]–[14] and curve fitted to the ideal transfer curve, or the ADC is self-linearized using the extracted errors [15], [16]. The digital calibration reported in [11] and [14] suffer from large differential nonlinearity (DNL) errors coming from truncation errors and interstage gain mismatches when the ADC is calibrated for more than one stage [20]. The approach in [12] does not account for the finite gain error, and the technique in [16] is applies only to a *single-stage* algorithmic ADC. The calibration techniques in [13] and [15] calibrate only the front-end conversion stages, and thus the calibration accuracy is limited by the remaining stages which equally suffer from analog inaccuracies.

In this paper, a radix-based digital calibration technique for multistage ADCs is described. Two ADC structures based on multiplying DAC (MDAC) are used to describe the basic calibration theory [21]. By making both the input and the reference voltage go through the same signal path, all nonideal factors within each converting stage are merged into a single equivalent term. This equivalent term represents the radix for the stage, and the ADC output can be digitally calibrated using a simple radix calculation. It will be shown that the equivalent radix value/number can be extracted by forcing most significant bits (MSBs) in the front-end stage while analog input is fixed. In this manuscript, a two-stage algorithmic ADC is used as a design example to describe the calibration procedure in a simplified manner. The proposed calibration method in general is applicable to multistage pipelined ADCs with modifications that will allow recycling operation during calibration mode.[1] The proposed technique compensates for capacitor mismatches and finite opamp gain error.[2] It will be shown that the key advantage here is that the calibration accuracy is not limited by the accuracy limitation of the converter itself as in most prior digital calibration techniques.

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[1]Naturally, there will be some drawback to normal operation by allowing the reconfigurability for recycling mode calibration operation. This will typically result in a reduced speed of conversion.

[2]As in most calibrations schemes available to date, our work does not compensate for nonlinear errors such as opamp nonlinearity. This is an important subject that is starting to receive increasing attention [22].

In Section II, the proposed radix calibration technique based on two different ADC architectures is covered in detail. A mathematical radix iteration procedure is described in Section III. Simulation results of a calibrated ADC are summarized in Section IV, followed by concluding remarks in Section V.

II. Radix-Based Digital Calibration Technique

In a single-bit-per-stage architecture, a two-level DAC and a multiply-by-two residue gain stage are often merged into a block called MDAC where a "capacitor-flip-over topology" has been widely used [23]. According to Fig. 1, after the input is first sampled onto the bottom plates of both sampling capacitors during ϕ_1, one of the capacitor flips over to the output and the other one is connected to $\pm V_{\rm ref}$ during ϕ_2 depending on the sub-ADC's decision level (single comparator for single-bit-per-stage architecture). There exists three important static errors. They are capacitor mismatch, finite opamp gain, and offset. They are denoted by α_i, δ_i, and o_i, respectively, in the following figures. Unlike the capacitor mismatches and the finite opamp gain errors, constant offset does not affect the linearity of the ADC in most applications. However, if the offset is big enough to push the transfer curve of a conversion stage out of the reference range, the signal/input information is partly lost. The lost information, namely missing decision level, is not reconstructible even after a post/digital calibration/correction process. To ensure no missing decision levels occur in the single-bit-stage architecture, the interstage gain is sometimes made less than two. This is referred to as the sub-radix conversion system. In this way, although a shift may occur in the transfer function, all the information will be preserved, transferred, and reconstructed by the remaining stages. This technique is referred to as the digital redundancy/correction, implementations of which have many variations. The digital redundancy relaxes the offset requirements of comparators and opamps.

Assuming that all capacitors are matched perfectly and the opamp has an infinite open-loop gain, the ideal operation can be depicted as shown in Fig. 2. The reconstructed ADC output $D_{\rm out}$ (where the MSB is D_1) can be calculated as follows:

$$D_{\rm out} = \sum_{k=0}^{n-1} D_{n-k} \cdot (2)^k \tag{1}$$

where n is the resolution of the ADC. This provides perfectly linear transfer function. However, in the presence of all error terms, (1) is no longer a linear function. Assuming for simplicity that the opamp has finite but linear open-loop gain A, the ith stage's residue output is (MDAC structure of Fig. 1 assumed)

$$V_{\rm out} = (2+\alpha_i)(1+\delta_i) \cdot \left(V_{\rm in} + D \cdot \frac{(1+\alpha_i)}{(2+\alpha_i)} V_{\rm ref} \right) \tag{2}$$

where $\delta_i = -(2+\alpha_i)/(1+\alpha_i+A)$ and $D = \pm 1$. Fig. 3 shows the corresponding block diagram (including offset).

For a special case, as in the *single-stage* algorithmic ADC, where $\alpha_i = \alpha$ and $\delta_i = \delta$, the residue voltage can be rewritten as

$$V_{\rm out} = (2+\alpha)(1+\delta) \cdot (V_{\rm in} + D \cdot V_r) \tag{3}$$

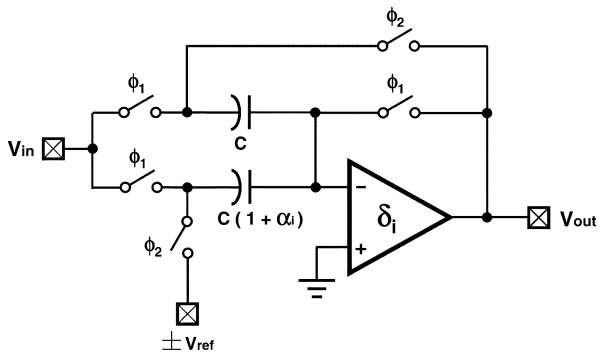

Fig. 1. Conventional MDAC with "capacitor flip-over" topology.

where $V_r = (1+\alpha)/(2+\alpha)V_{\rm ref}$. The effective reference voltage V_r is a newly defined reference level and does not contribute to linearity error. As a result, only one interstage gain term $ra = (2+\alpha)(1+\delta)$ exists. This represents an equivalent radix for the stage. The output of the ADC can now be calibrated with a simple radix calculation [16]

$$D_{\rm out} = \sum_{k=0}^{n-1} D_{n-k} \cdot (ra)^k. \tag{4}$$

In multistage architecture, each stage includes two sets of error terms as shown in (2), which are interstage gain with error $(2+\alpha_i)(1+\delta_i)$ and reference level with error $(1+\alpha_i)/(2+\alpha_i)$. Since the input and the reference are amplified with different coefficients (due to error terms), we can no longer assume the equivalent radix for the stage. For the ADC to be calibrated in the form of (4), both the input and the reference should have the same multiplying factor. Two alternative methods are discussed in the following.

A. Calibration of Half-Reference MDAC

The first method is based on the MDAC structure illustrated in Fig. 4. To allow only a single equivalent error term per stage, both input and reference should see the identical set of error terms. Instead of one of the sampling capacitors being flipped over to the output, dedicated feedback and sampling capacitors are used. After the input is sampled onto the sampling capacitor while the opamp is being reset during ϕ_1, $+$ or $-V_{\rm ref}/2$ is sampled onto the very same capacitor during ϕ_2. Therefore, the reference voltage is directly subtracted from the input before it is multiplied. The net result is that both the input and the reference see the same signal path. The residue voltage can now be described as

$$V_{\rm out} = ra_i \cdot \left(V_{\rm in} + D \cdot \frac{V_{\rm ref}}{2} \right) \tag{5}$$

where $ra_i = (2+\alpha_i) \cdot (1+\delta_i)$. With this modified MDAC, the digital output can be calibrated as follows:

$$D_{\rm out} = D_n + D_{n-1} \cdot (ra_{n-1}) + D_{n-2} \cdot (ra_{n-1})(ra_{n-2}) + \cdots + D_1 \prod_{k=1}^{n-1} ra_k. \tag{6}$$

The equivalent radix block diagram of this operation is illustrated in Fig. 5. Note that this type of calibration changes the

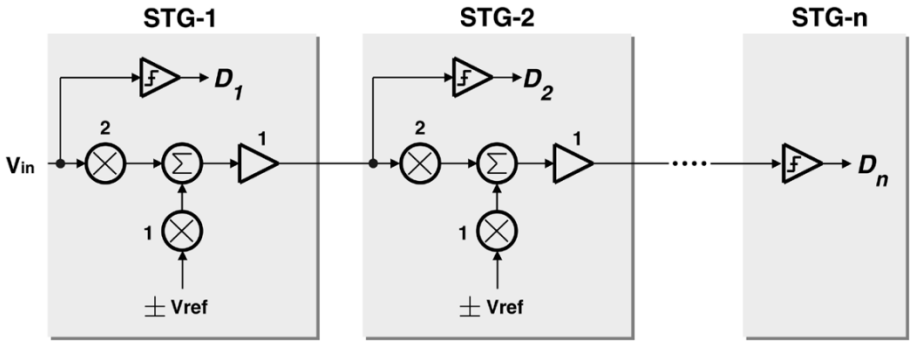

Fig. 2. Ideal block diagram of a multistage ADC.

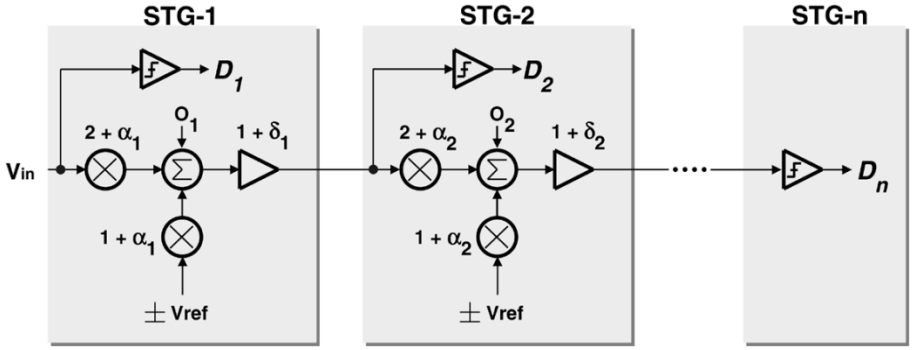

Fig. 3. Block diagram of a multistage ADC with error sources.

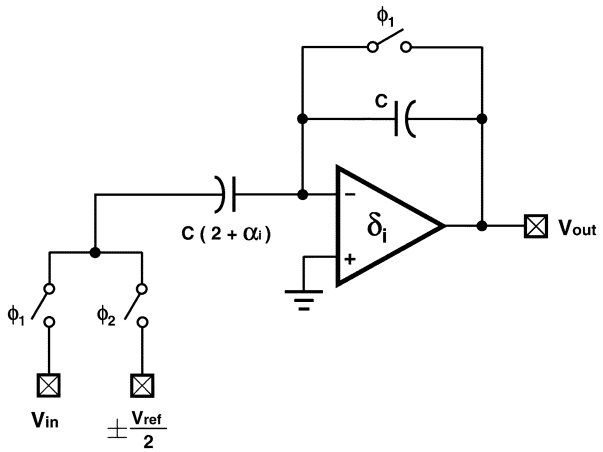

Fig. 4. Half-reference based MDAC architecture.

slope of overall ADC transfer curve. This linear gain error does not affect the overall ADC linearity. If desired, this can be compensated by a variety of methods including using a variable gain amplifier at the input of the ADC, digitally trimming the input capacitor, analog reference voltage scaling, and digital domain scaling.

B. Calibration of Capacitor Flip-Over MDAC

The second method is based on Fig. 3. Some equivalent transformations should be made in Fig. 3. The procedure of reconfiguration is illustrated in Fig. 6. If we change $V_{\rm ref}$ to $V_{\rm ref}/2$ and adjust the gain factor of the reference voltage accordingly, we arrive at the diagram of Fig. 6(b). Then, we merge the gain factor of the reference voltage to the input and output portions to result in the form shown in Fig. 6(c). Finally, the input and output of each stage is redefined as shown in Fig. 6(d). In this way, the residue voltage at the ith stage can be rewritten as

$$V_{\rm out} = 2(1+\alpha_i)\cdot(1+\delta_i)\cdot\frac{(2+\alpha_{i+1})}{2(1+\alpha_{i+1})} \cdot\left(V_{\rm in}{}' + D\cdot\frac{V_{\rm ref}}{2}\right) \quad (7)$$

where $V_{\rm in}{}' = ((2+\alpha_i)/2(1+\alpha_i))\cdot V_{\rm in}$, which is a newly defined input. The resulting equivalent radix is

$$ra_i = 2(1+\alpha_i)(1+\delta_i)\cdot\frac{(2+\alpha_{i+1})}{2(1+\alpha_{i+1})}. \quad (8)$$

Since both the input (newly defined) and the reference see the same multiplying factor, the calibrated ADC output can also be obtained by (6). One issue in this reconfiguration is that the comparator (sub-ADC) still sees the original input $V_{\rm in}$ (before reconfiguration). This means a signal-dependent offset is added to the input of the comparator (sub-ADC). However, this is not a problem because the amount of added offset is small since it comes from internal capacitor mismatch and is compensated by the digital redundancy architecture. In addition, this structure has an added advantage over the half-reference MDAC because of the increased feedback factor.

C. 1.5-Bit-Per-Stage Architecture

Since the two-level DAC is inherently linear, the slope of the ADC is naturally merged into the interstage gain term. Another architecture that has an inherently linear DAC is the 1.5-bit-per-stage ADC. It uses three levels: $+V_{\rm ref}$, 0, and $-V_{\rm ref}$,

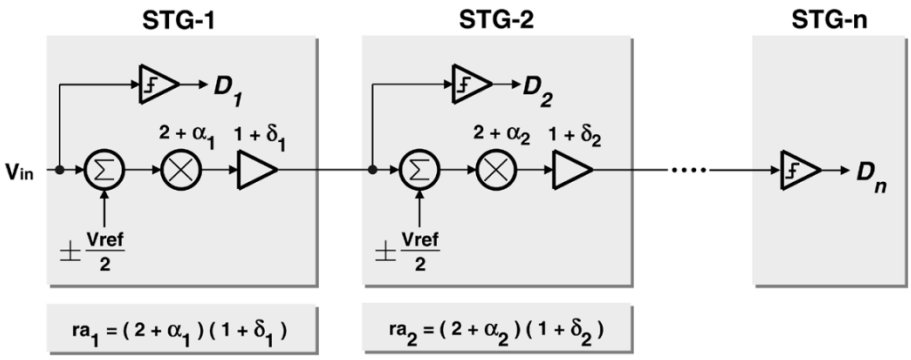

Fig. 5. Block diagram of the half-reference based ADC.

which are subtracted from the input during the residue amplification. Therefore, either "capacitor flip-over" or "half-reference" architectures can be employed and calibrated in the same way. The difference from the single-bit-per-stage architecture is that it generates two raw bits per stage and digital correction is done by overlapping these bits with shift registers and adders. In order to apply our proposed radix-based calibration to this 1.5-bit-per-stage architecture properly, the raw codes from all stages need to be preserved and applied in the calibration before the digital correction happens. We omit the details of the 1.5-bit-per-stage architecture in order to maintain the focus on the fundamentals of the new calibration scheme.

III. Radix Measurement and Calibration

In the proposed calibration scheme, all error terms should first be measured accurately. The accuracy of the measurement determines the overall ADC resolution. The primary difficulty is that the exact radix for each stage cannot be known in advance. With the calibration sequence described in the following, the initially estimated values iterate to the final/correct values mathematically using an iterative calculation loop. Between the two configurations described in Section II, the latter architecture (Fig. 5) is used in this section to illustrate the detailed calibration steps. The former architecture (Fig. 6) can be calibrated in exactly the same way. A 14-bit *two-stage* algorithmic ADC architecture is chosen, representing a simplest form of multistage ADC, as shown in Fig. 7. The ADC generates a 14-bit (sub-radix bits) digital output after 7 clock cycles (14 phases). The ADC output can be reconstructed by

$$D_{\text{out}} = \underbrace{D_{14}}_{\text{LSB}} + D_{13}\cdot(ra_1) + D_{12}\cdot(ra_1)(ra_2) + D_{11}\cdot(ra_1)^2(ra_2) + D_{10}\cdot(ra_1)^2(ra_2)^2 + \cdots + \underbrace{D_1}_{\text{MSB}}\cdot(ra_1)^7(ra_2)^6 \quad (9)$$

where ra_1 and ra_2 are equivalent radices for STG-1 and STG-2, respectively.

Accounting for all the error terms, the biggest discontinuity of the ADC occurs at the points where the MSB changes from zero to one. In a standard radix-2 (binary) system, assuming an ideal condition, this discontinuity can be extracted by forcing digital bits to the MSB-stage with zero analog input. For example, if "1" is forced with zero analog input, the residue results in $-V_{\text{ref}}$, and the resulting ADC output would be $1000\cdots00$ (MSB "1" is the forced bit). When "0" is forced under the same condition, the residue would be V_{ref}, which leads to the ADC output of $0111\cdots11$ (MSB "0" is the forced bit). Although the ADC is converting the same analog input of 0 V, the difference of the two quantized values is 1 least significant bit (LSB). In practical implementations, considering the error terms (e.g., capacitor mismatch and offset) for both stages, digital redundancy is normally employed to prevent the missing decision levels as mentioned in the previous section. In this example, the digital redundancy simply means using a sub-radix number less than two. In this case, forcing the MSB of "1" and "0" will only change the residue signal path. Since digital outputs are inherently corrected by the digital redundancy, the nominal difference between the two quantized values will be zero (not 1 LSB). Therefore, with this desired value of zero, the estimated radix numbers can now be corrected by an incremental update algorithm:

$$ra_i[n+1] = ra_i[n] - \Delta\cdot\varepsilon_i[n]. \quad (10)$$

Here, ε_i is the mismatch between the two quantized output after MSBs are forced, n is the iteration index, and Δ is update step size. Each word is calibrated using the current estimate of ra_1 and ra_2. The two radices are updated alternately until the iteration comes to an end. The measurement/calibration details specific to sub-2-radix are summarized in the following.

The first step is to measure ra_1. As shown in Fig. 7, MSB of "1" is forced to STG-1 and the analog input is set to zero. The resulting residue of STG-1 is

$$V_A = -(ra_1)\cdot\frac{V_{\text{ref}}}{2}. \quad (11)$$

The ADC itself then digitizes V_A during the remaining conversion cycles to have a 14-bit digital word DA which includes "1" forced MSB. Next, MSB of "0" is forced to STG-1 to obtain the residue

$$V_B = (ra_1)\cdot\frac{V_{\text{ref}}}{2} \quad (12)$$

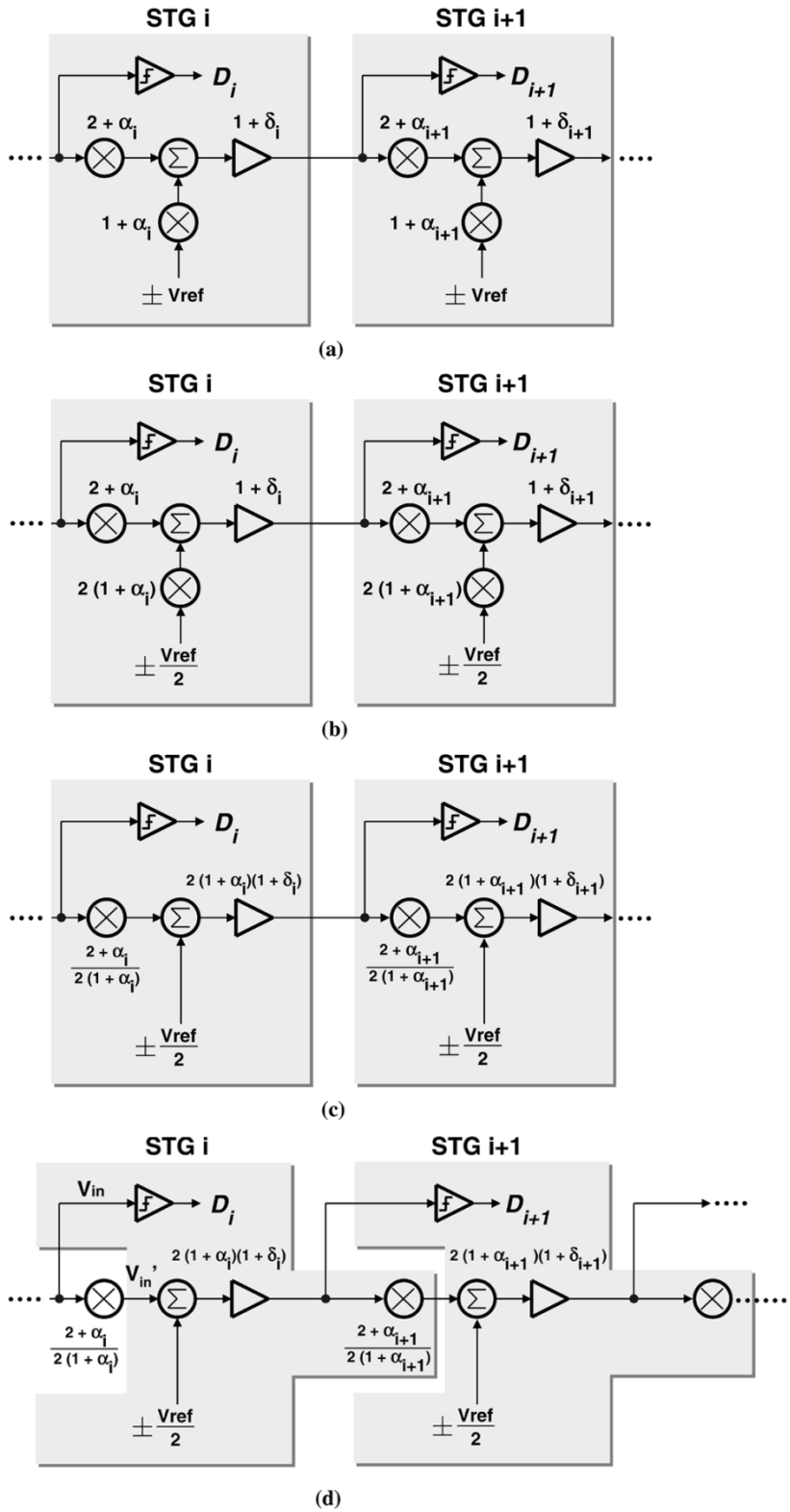

Fig. 6. Equivalent transformation of ADC.

which is also digitized to DB (forced MSB "0" included). Note that V_A and V_B define the upper and lower reference level of STG-2. The ε_1 can now be calculated as follows:

$$\varepsilon_1 = D_{\text{out}}(DA) - D_{\text{out}}(DB) \tag{13}$$

where D_{out} is calculated using (9).

The ε_2 measurement for ra_2 is done in a similar manner by effectively moving the MSB-stage from STG-1 to STG-2. The two resulting residues from STG-2 during the bit-forcing sequence also redefine the full-scale input range of STG-1. The only difference is that during the bit-forcing of STG-2 (with zero analog input to STG-2), the STG-1 output is ignored. This implies that

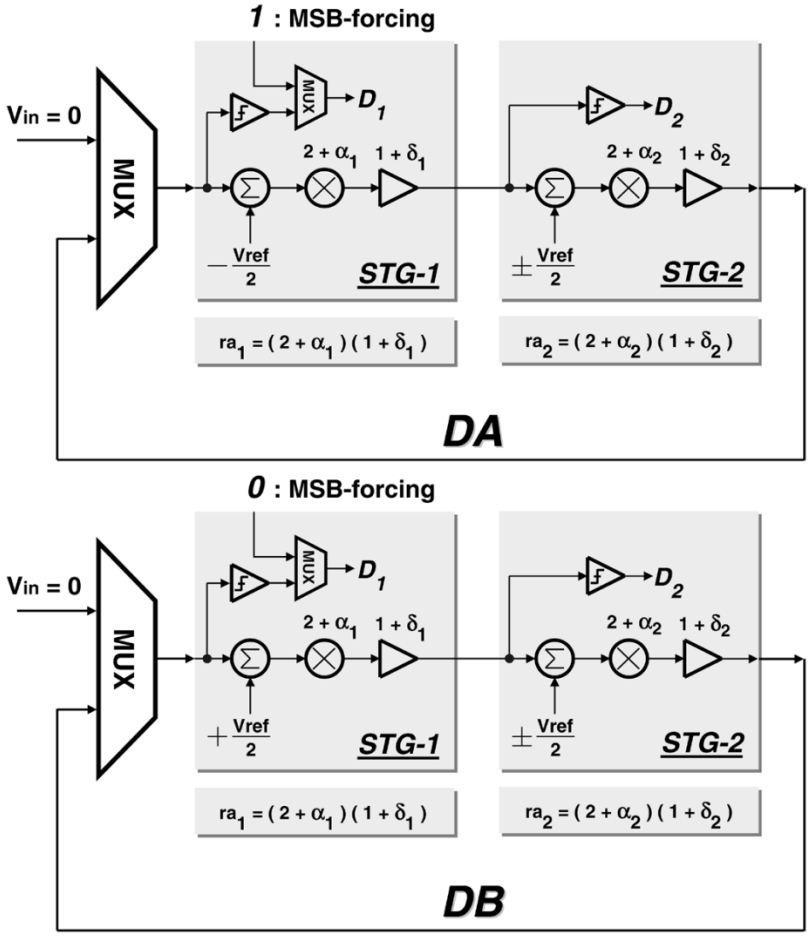

Fig. 7. Conceptual block diagram of ra_1 iteration.

ra_2 measurement is done at the 13-bit level (instead of 14-bit). Note that the resolution (number of bits) used in the calibration mode can be different from the normal conversion mode. For example, 18-bit and 17-bit accuracy may be used to minimize calibration mode quantization error instead of the 14-bit and 13-bit setting.[3]

Once the measurements are completed for $\varepsilon_1(ra_1)$ and $\varepsilon_2(ra_2)$, (10) is used to update the initially updated radix values ra_1 and ra_2. Since the overall ADC range is composed of a combination of the two radices, they are updated alternately based on one another's latest values until the overall transfer function is fully linear (i.e., ε_i approaches zero). The update/iteration loop is purely mathematical after four digital words are generated (measured). This two-stage algorithmic ADC calibration example extends to ADC's with any number of stages.

[3]This fact makes the calibration operation of a multistage pipelined (not algorithmic) ADC equivalent to this two-stage algorithmic ADC example. However, in the pipeline ADC, it would need to operate in a recycling mode for calibration, which implies modifying the MSB stage to accommodate the recycling mode. This would typically imply some degradation in the ADC conversion speed during normal operation.

IV. Simulation Results

Based on Fig. 7 (using half-reference MDAC), the Fig. 8 illustrates the iteration of ra_1 and ra_2 at the behavioral level simulation. Actual values of ra_1 and ra_2 used in the simulation (randomly chosen) are 1.9531 and 1.9442, and the final iteratively reached values are $ra_1 = 1.9533$ and $ra_2 = 1.9438$. The update step size Δ should be much smaller than 1-LSB step size of the ADC. In this simulation, 2^{-19} is used. Fig. 9 shows a typical fast Fourier transform (FFT) plot with $\sigma = 0.4\%$ capacitor mismatches and opamp dc gain of 1000. The resulting signal-to-noise + distortion ratio (SNDR) shows 80.1 dB after calibration. Under the similar statistical nonideal conditions, the ADC based on the capacitor flip-over structure (Fig. 1) is also simulated. The output spectrum before/after calibration is shown in Fig. 10. The SNDR after calibration is 80.5 dB.

The calibrated ADCs simulated signal-to-noise distortion ratio (SNDR) is a few decibels lower than the ideal 14-bit ADC (with radix-1.95). There is a couple of reasons for this. One reason is that ra_2 is measured/iterated using 13-bit digital words (not 14-bit). Second, digital truncation errors occur during the calculation of ε_i. In theory, one simple way to recover the decreased dynamic range is to increase the resolution of the ADC for the calibration mode and to reduce radix update step size (Δ) even more during iteration. It has been verified that this results in achieving almost the ideal accuracy (less

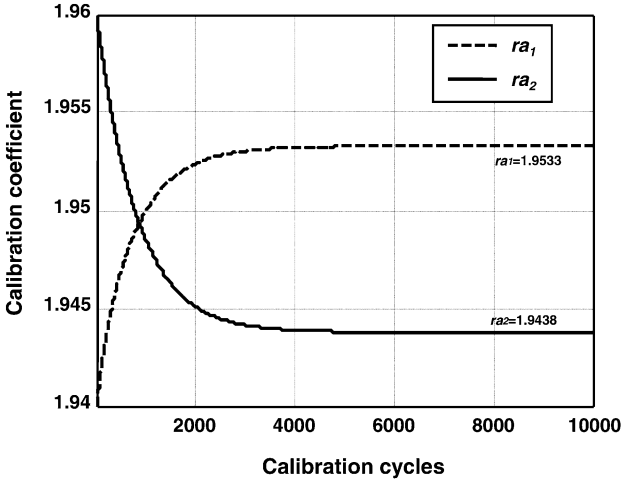

Fig. 8. Iteration/convergence of radices for the two-stage algorithmic ADC using the half-reference architecture.

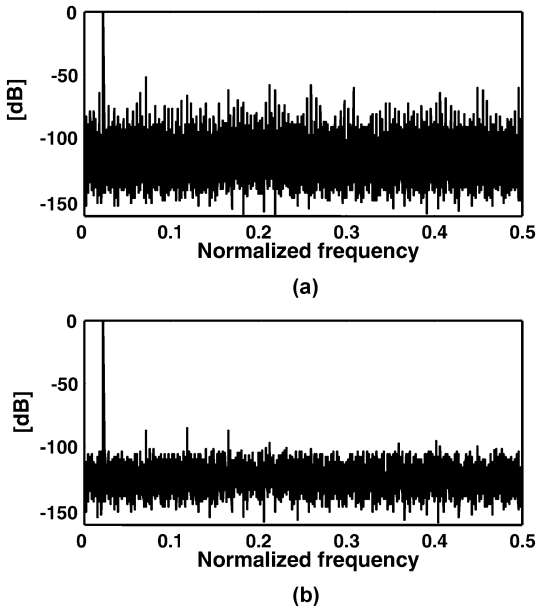

Fig. 9. FFT plots of (a) before and (b) after calibration of the half-reference architecture.

than a fraction of a decibel difference) of the overall ADC (added cost is the added computational complexity). It has also been verified in simulation that straight pipelined ADC can be calibrated to the same degree of accuracy when the ADC calibration is performed in a recycling mode of operation (i.e., the last stage sends the residue back to the MSB stage to resolve an increased number of bits).

It is important to realize, however, that in practical IC realizations, component/environmental nonlinearities and various noise sources would significantly limit the overall resolution, and very high SNDR numbers are difficult to achieve. Some of the most effective digital calibration methods in the past have demonstrated up to 93-dB level of SFDR and 85-dB level of SNDR (e.g., [14]), where SNDR was limited by the kT/C noise and opamp nonlinearity.

When we applied our proposed radix-based calibration to an ultra low-voltage IC implementation [24], we were able to

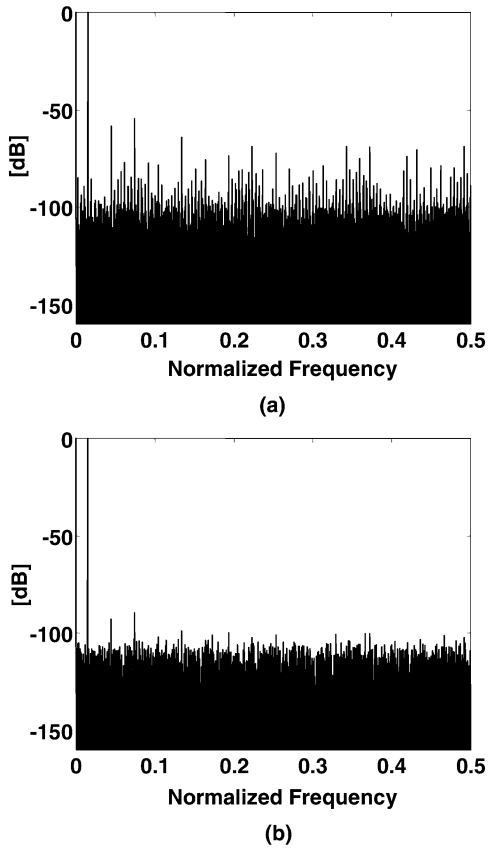

Fig. 10. FFT plots of (a) before and (b) after calibration of the capacitor flip-over topology.

achieve SFDR improvement from 47 to 75 dB, and SNDR improved from 40 to 55 dB. The performance limitation of this IC implementation was due to issues associated with ultra low-voltage operation, where opamp nonlinearity, kT/C limitation, and other nonidealities start to dominate at aggressively reduced voltage headroom.

V. Conclusion

A radix-based digital self-calibration technique for multistage ADCs is described. The calibration scheme is enabled by use of equivalent radix architecture, MSB-forcing for error extraction, and mathematical update/iteration loop to correct the error. Two alternative ways to implement and calibrate the ADC are presented. The proposed calibration technique accounts for nonidealities of all conversion stages during calibration such that the calibrated output during the conversion cycle will not be limited by component inaccuracies. The proposed radix-based calibration technique is generally applicable to multistage pipelined ADCs (e.g., N-stage N-bit pipelined ADC). A multibit-per-stage architecture can also be accommodated with proper modifications to the MDAC.

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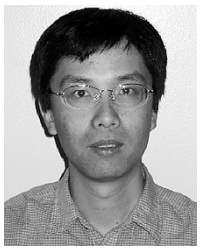

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