Analysis of Charge-Pump Phase-Locked Loops

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***Abstract*—In this paper, we present an exact analysis for third-order charge-pump phase-locked loops using state equations. Both the large-signal lock acquisition process and the small-signal linear tracking behavior are described using this analysis. The nonlinear state equations are linearized for the small-signal condition and the z-domain noise transfer functions are derived. A comparison to some of the existing analysis methods such as the impulse-invariant transformation and s-domain analysis is provided. The effect of the loop parameters and the reference frequency on the loop phase margin and stability is analyzed. The analysis is verified using behavioral simulations in MATLAB and SPECTRE.**

***Index Terms*—Impulse invariance, jitter, loop delay., phase-locked loop (PLL), phase noise, state space, z-domain.**

I. Introduction

CHARGE-PUMP based phase-locked loops (CPLL) are widely used as clock generators in a variety of applications including microprocessors, wireless receivers, serial link transceivers, and disk drive electronics [1]–[8]. One of the main reasons for the widely adopted use of the CPLL in most PLL systems is because it provides the theoretical zero static phase offset, and arguably one of the simplest and most effective design platforms. The CPLL also provides flexible design tradeoffs by decoupling various design parameters such as the loop bandwidth, damping factor, and lock range. While there are numerous CPLL design examples in the literature, precise analysis and a mathematical clarity of the loop dynamics of the CPLL is lacking. The two most popular references in this arena by Hein and Scott [9] and Gardner [10] provide useful insight and analysis for second-order PLLs. Several other references [11], [12], provide simplified yet useful approximations of third-order CPLLs. However, they do not provide a complete and extensive analysis for practical integrated circuit (IC) PLLs, i.e., third-order CPLLs. The intent of this paper is to clarify and provide mathematically exact and insightful understanding of the PLL dynamics and accurate transfer functions of a practical CPLL system. The focus of the detailed derivations and analysis is on the CPLL example because IC designers predominantly choose CPLLs over other PLL architectures. Although the presentation is for a CPLL, the analysis can be readily extended for other PLL systems.

A typical implementation of the CPLL consists of a phase frequency detector (PFD), a CP, a passive loop filter (LF), and a voltage controlled oscillator (VCO). The CPLL system is shown in Fig. 1. A divider is used in feedback, in applications requiring clock multiplication but is omitted here for simplicity. The PFD commonly generates a pair of digital pulses corresponding to the phase/frequency error between the reference clock and the VCO output by comparing the positive (or negative) edges of the two inputs. The CP then converts the digital pulses into an analog current that is converted to a voltage via the passive loop filter network. The resulting control voltage drives the VCO. The negative feedback loop forces the phase/frequency error to zero. Like any other feedback system, a CPLL has to be designed with a proper consideration for stability.

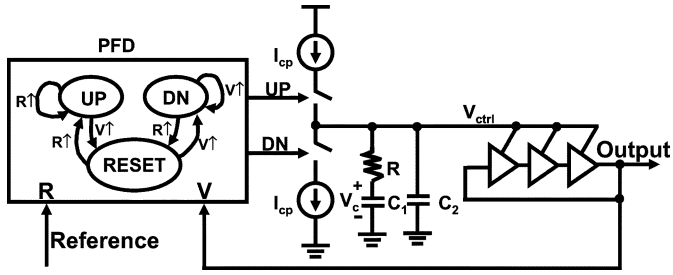

Fig. 1. Third-order CPLL block diagram.

The majority of IC designers analyze CPLLs by treating the PLL loop as a continuous-time system and by using a basic s-domain model. However, due to the sampling nature of the PFD, the continuous-time approximation introduces a considerable amount of error. For example, the effective phase margin of the CPLL is degraded due to the inherent sampling operation which can lead to excessive peaking in the jitter transfer function and, if one is not careful, to instability. Therefore, it is important to incorporate the sampling nature into the CPLL model. For this reason, IC designers have been faithful in keeping the loop bandwidth of the PLL to about 1/10 of the PFD update frequency (or lower). The loop delay effects are also modeled by adding $e^{(-sT_d)}$ into the s-domain transfer function. A discrete-time model using the impulse-invariant transformation was proposed by Hein and Scott in [9], where the derivations focus on a second-order loop. Since a second-order loop does not represent a real/practical CPLL system, the simulation/verification/comparison results were presented for a third-order loop without explicitly specifying so. Moreover, the impulse-invariant transformation requires that the PFD output be impulses. It is not clear from [9], as to what pulse width can be considered narrow enough to be an impulse. A more rigorous and exact analysis of a second-order loop is presented by Gardner in [10], where only the denominator of jitter transfer functions of second- and third-order loops are presented. In this paper, we present an

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exact analysis for a third-order CPLL.[1] The rigorous side of our presentation will expand on Gardner's work in [10]. In addition, we show that the linearized form of the state-space model resulting in the z-domain transfer function is identical to that obtained from the impulse-invariant transformation. Our analysis provides this important connection and insight between the two approaches. This paper expands on the important thrusts of the *exact analysis* of the CPLL, and the information that can be extracted from the analysis to gain useful insight of the loop dynamics. Even though this paper derives various equations describing the behavior of the CPLL, some simplifying assumptions are made in order to keep the algebra simple. Hence, this analysis in its current form can not be used as a substitute for modern day PLL simulation tools. Readers interested in accurate and fast behavioral models and simulation of CPLLs are referred to [13].

This paper is organized in the following manner. Section II briefly describes the operation of a third-order CPLL and its continuous-time steady-state model. The complete state-space analysis of the CPLL and linearization of the state equations along with the noise analysis is described in Section III. We will also briefly summarize the impulse-invariant transformation results in this section and show how the result matches the linearized form of the exact analysis. The large- and small-signal models derived in Section III are verified using behavioral simulations in SPECTRE and MATLAB in Section IV. Finally, the key concluding remarks of the paper are given in Section V.

II. Third-Order CPLL

The functional block diagram of the third-order CPLL is shown in Fig. 1 along with the state diagram of the PFD. The three state PFD generates UP and DN signals depending on the time (phase) difference between the positive edges of the reference and the VCO output. The CP converts the digital pulse to an analog control voltage through a loop filter. The loop filter consists of a resistor R in series with a capacitor C_1. The CP current source and the capacitor C_1 form an integrator in the loop and the resistor introduces a stabilizing zero to improve the phase margin and hence improve the transient response of the CPLL. However, the resistor causes a ripple of value $I_{\rm cp}R$ on the control voltage at the beginning of each PFD pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction. This ripple modulates the VCO frequency and introduces excessive jitter in the output. To suppress the ripple induced jitter a small capacitor C_2 is added in parallel with the R and C_1 network as shown in Fig. 1. However, this capacitor introduces a pole, thus increasing the order of the system to three. Therefore, the phase degradation due to this pole has to be accounted for by a proper choice of the other loop parameters. The choice of the loop parameters $I_{\rm cp}$, R, C_1, and C_2 is determined by assuming a continuous-time approximation. This process is briefly described in the following section.

[1]A real/practical CPLL system is at least third-order due to the parasitic capacitance at the input of the VCO, with or without the explicit "ripple bypass capacitor."

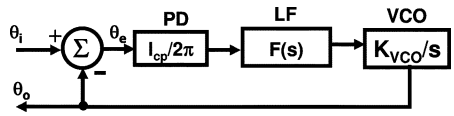
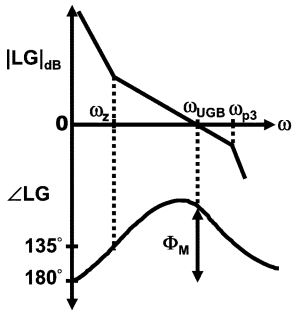


Fig. 2. Steady-state phase-domain CPLL block diagram.



$$\Phi_M = \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_{p3}}\right)$$

$$\omega_z = \frac{1}{RC_1}$$

$$\omega_{p3} = \frac{1}{R\left[\frac{C_1C_2}{C_1+C_2}\right]}$$

Fig. 3. Third-order loop-gain Bode plot.

A. s-Domain Analysis

When the CPLL is in near lock condition, it can be represented in a phase-domain block diagram format as shown in Fig. 2. The gain of the PFD along with the CP can be shown to be $I_{\rm cp}/2\pi$. The transfer function, $F(s)$, of the loop filter can be derived using linear analysis and is equal to

$$F(s) = \frac{s + \frac{1}{RC_1}}{C_2\, s\left(s + \frac{1}{R\left(\frac{C_1C_2}{C_1+C_2}\right)}\right)}. \tag{1}$$

The VCO is an ideal integrator with gain $K_{\rm vco}$.[2] The loop-gain of the third-order CPLL[3] is

$$LG_3(s) = \frac{K_{\rm vco}I_{\rm cp}}{2\pi}\,\frac{s + \frac{1}{RC_1}}{C_2\, s^2\left(s + \frac{1}{R\left(\frac{C_1C_2}{C_1+C_2}\right)}\right)}. \tag{2}$$

As mentioned earlier, the loop has a zero and three poles and the conceptual Bode plot is shown in Fig. 3. The phase margin degradation due to the third pole is obvious and is mathematically expressed by

$$\Phi_M = \arctan\left(\frac{\omega_{UGB}}{\omega_z}\right) - \arctan\left(\frac{\omega_{UGB}}{\omega_{p3}}\right). \tag{3}$$

A careful look at the Bode plot reveals a relatively flat portion of the phase plot where the phase lag due to the third pole nearly cancels the phase lead introduced by the zero. An optimal choice of the capacitor ratio C_1/C_2 leads to a phase margin that is relatively immune to process variations. The maximum phase margin can be calculated by equating the first derivative of Φ_M

[2]In an integrated VCO, the gain is a nonlinear function of the control voltage. This makes the loop dynamics vary with the operating frequency. In this analysis we assume that the loop dynamics are designed for the worst case and that the PLL is stable for all operating conditions.

[3]In many PLL designs, several higher order poles and zeros exist due to transistor and interconnect parasitics. Careful circuit simulations are required to analyze the effect of the higher order poles and zeros. However, in most PLL designs the loop bandwidths are in the range of a few tens of megahertz. Therefore, PLL loop dynamics are dominated by the loop filter as opposed to the parasitic poles which are in the hundreds of megahertz range.

to zero. It can be shown that the maximum phase margin occurs when

$$\omega_{UGB} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}. \tag{4}$$

Substituting (4) into the phase margin expression (3), we get

$$\Phi_M = \arctan\left(\sqrt{\frac{C_1}{C_2} + 1}\right) - \arctan\left(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}}\right) \tag{5}$$

$$C_1 = 2C_2\left(\tan^2\Phi_M + \tan\Phi_M\sqrt{\tan^2\Phi_M + 1}\right). \tag{6}$$

Equation (6) describes the relationship between the two capacitors that place the zero and the third pole so as to yield a robust phase margin. The loop bandwidth and phase margin are mandated by the application. For example, in the case of clock generators with a poor phase noise VCO and a pure low-frequency reference, a relatively high bandwidth is required, while some optical standards require a low loop bandwidth and a large phase margin to avoid any jitter peaking. For a given loop bandwidth and phase margin, the three variables C_1, C_2, and $I_{\rm cp}$ can be calculated using (4)–(6) while noting unity loop-gain of (2) (i.e., $|LG_3(j\omega_{UGB})| = 1$). The loop filter resistance is typically chosen based on noise and area constraints. The closed-loop transfer function is given by

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{LG_3(s)}{1 + LG_3(s)} = \frac{K_{\rm vco}I_{\rm cp}}{2\pi C_2}\frac{s + \frac{1}{RC_1}}{s^3 + \left(\frac{1}{R\frac{C_1C_2}{C_1+C_2}}\right)s^2 + \frac{K_{\rm vco}I_{\rm cp}}{2\pi C_2}s + \frac{K_{\rm vco}I_{\rm cp}}{2\pi RC_2C_1}}. \tag{7}$$

III. State-Space Analysis

The s-domain analysis based on a continuous-time approximation of CPLLs suffers notably from two key drawbacks. First, due to the discrete-time nature of the PFD operation, sampling is inherent in any CPLL employing a digital PFD. The s-domain analysis does not comprehend the sampling nature and, hence, can lead to degraded performance particularly in terms of input jitter peaking. Second, since s-domain analysis is a steady-state analysis it does not predict the nonlinear acquisition process of the CPLL. An analysis using the difference equations and a state-space model for the loop filter can accurately define the functioning of the CPLL. We describe this methodology in the following. The difference equations describing the input and output phase are given by [10]

$$\theta_i(t) = \theta_i(0) + \omega_i t \tag{8}$$

$$\theta_o(t) = \theta_o(0) + \omega_{fr}t + K_{\rm vco}\int_0^t v_{\rm ctrl}(\tau)d\tau \tag{9}$$

$$\theta_e = \theta_i - \theta_o \tag{10}$$

where ω_i is the input reference frequency and ω_{fr} is the free running frequency of the oscillator and $K_{\rm vco}$ is the gain of the VCO. The initial conditions on the input and the output phase are represented by $\theta_i(0)$ and $\theta_o(0)$, respectively. For a positive phase error ($\theta_e > 0$) the loop filter capacitors are charged, and for a negative phase error the capacitors are discharged. The charging/discharging current can be represented by

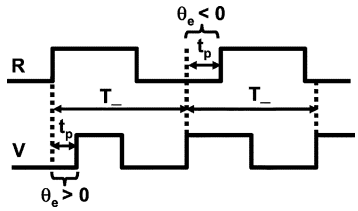


Fig. 4. Definition of t_p and $T_{\_}$.

$$i_p = \begin{cases} I_{\rm cp}\,\mathrm{sgn}(\theta_e), & \text{if } 0 \le t \le t_p \\ 0, & \text{if } t_p < t < T_{\_} \end{cases} \tag{11}$$

where $\mathrm{sgn}(\theta_e)$ is the polarity (i.e., $+1$ or -1) of θ_e. The variable t_p is the time equivalent of the phase error, while $T_{\_}$ represents the time at which the next rising edge, either the VCO or the reference, occurs. Fig. 4 shows the definitions of the variables t_p and $T_{\_}$ for both positive and negative phase errors. The relationship between the phase error and charging/discharging time t_p will be shown in the later part of this section. A common problem associated with the CPLLs is the dead zone in the CP. The dead zone is the amount of phase error that does not result in a charging/discharging pump current. For a three-state phase detector and CP, the dead zone is overcome by generating small equal width U/D pulses when the CPLL is in phase lock. Using this simple technique, a well designed PFD and CP combination [14], [15] has a very small dead zone and hence has negligible effect on the PLL behavior and therefore we assume zero dead zone in this analysis. In addition to the dead zone problem, in a practical PLL the current sources implementing the CP suffer from various nonidealities. For example, in a MOS-based implementation, the current sources suffer from channel length modulation thus leading to a CP current that depends on the control voltage. This nonlinearity can be incorporated into the analysis by defining the CP current as a function of the control voltage for a given channel length modulation factor. However, several circuit design techniques exist to mitigate this effect. One design example uses an active loop filter [16]. Also, there is an inherent mismatch between PMOS and NMOS current sources in the CP which causes pattern jitter. This mismatch can be reduced by using replica biased current sources [17]. To simplify the analysis we assume that the effect of the nonlinearity and the current mismatch is negligible.

The *RC* network representing the loop filter can be described by two differential equations as shown below:

$$\frac{dv_{\rm ctrl}}{dt} = \frac{-v_{\rm ctrl}}{RC_2} + \frac{v_c}{RC_2} + \frac{i_p}{C_2} \tag{12}$$

$$\frac{dv_c}{dt} = \frac{v_{\rm ctrl}}{RC_1} - \frac{v_c}{RC_1} \tag{13}$$

where the VCO control voltage $v_{\rm ctrl}$ represents the voltage across the "ripple bypass capacitor" C_2 and v_c represents the voltage across the primary loop filter capacitor C_1. This type of formulation for a linear system with two state variables, $v_{\rm ctrl}$

and v_c, is also referred to as a state-space representation. We present the final solution of these state equations calculated using the procedure in [18]

$$\text{for } 0 < t \le t_p$$

$$v_{\text{ctrl}}(t) = v_{\text{ctrl}}(0)\left(g_1(t) + \omega_z g_2(t)\right) + v_c(0)\omega_2 g_2(t) + \frac{i_p}{C_2}\left(g_2(t) + \frac{\omega_z(g_1(t)-1)}{\omega_{p3}^2} + \frac{\omega_z t}{\omega_{p3}}\right) \quad (14)$$

$$v_c(t) = v_{\text{ctrl}}(0)\omega_z g_2(t) + v_c(0)\left(g_1(t) + \omega_2 g_2(t)\right) + \frac{i_p}{C_2}\left(\frac{\omega_z(g_1(t)-1)}{\omega_{p3}^2} + \frac{\omega_z t}{\omega_{p3}}\right) \quad (15)$$

$$\text{for } t_p < t \le T_-$$

$$v_{\text{ctrl}}(t) = v_{\text{ctrl}}(t_p)\left(g_1(t) + \omega_z g_2(t)\right) + v_c(t_p)\omega_2 g_2(t) \quad (16)$$

$$v_c(t) = v_{\text{ctrl}}(t_p)\omega_z g_2(t) + v_c(t_p)\left(g_1(t) + \omega_2 g_2(t)\right). \quad (17)$$

In the above, $\omega_2 = 1/RC_2$, $g_1(t) = \exp(-\omega_{p3}t)$, and $g_2(t) = (1/\omega_{p3})(1 - \exp(-\omega_{p3}t))$. In order to accurately define the lock acquisition process, it is sufficient to evaluate the output phase at two time instances t_p and T_- as shown in Fig. 4. The relationship between the phase error θ_e and its time equivalent t_p depends on the sign of the phase error. When the phase error is negative (i.e., the VCO edge occurred prior to the reference edge) t_p is given by

$$t_p = \frac{2\pi - \theta_i(0)}{\omega_i} \quad \text{when } \theta_e < 0. \quad (18)$$

However, when the phase error is positive (i.e., the reference edge occurred prior to the VCO edge), the charging current continuously charges the loop filter capacitance thereby increasing the control voltage. This leads to a faster accumulation of the phase in the VCO thus preventing us from using a linear relationship to calculate t_p. In this case, t_p is the solution of the equation

$$K_{\text{vco}}\int_0^{t_p} v_{\text{ctrl}}(\tau)d\tau + \omega_{fr}t_p + \theta_o(0) - 2\pi = 0 \quad \text{when } \theta_e > 0 \quad (19)$$

where

$$\int_0^{t_p} v_{\text{ctrl}}(\tau)d\tau = v_{\text{ctrl}}(0)\left(g_2(t_p) + \frac{\omega_z(t_p - g_2(t_p))}{\omega_{p3}}\right) + v_c(0)\frac{\omega_2(t_p - g_2(t_p))}{\omega_{p3}} + \frac{i_p}{C_2\omega_{p3}}\left(t_p - g_2(t_p) + \frac{\omega_z(g_2(t_p) - t_p)}{\omega_{p3}} + \frac{\omega_z t_p^2}{2}\right) \quad (20)$$

This integral (20) is derived from (14). Once t_p is found, the input and output phase at t_p can be calculated by substituting t_p into (8) and (9), respectively. Similarly, the time T_- at which the next rising edge occurs, either the reference (T_-^{ref}) or the VCO (T_-^{VCO}), can be calculated using the equations

$$T_-^{ref} = \frac{2\pi - \theta_i(t_p)}{\omega_i} \quad (21)$$

$$K_{\text{vco}}\int_{t_p}^{T_-^{VCO}} v_{\text{ctrl}}(\tau)d\tau + \omega_{fr}T_-^{VCO} + \theta_o(t_p) - 2\pi = 0 \quad (22)$$

$$T_- = \min\left(T_-^{ref}, T_-^{VCO}\right) \quad (23)$$

where

$$\int_{t_p}^{T_-} v_{\text{ctrl}}(\tau)d\tau = \frac{v_{\text{ctrl}}(t_p)}{\omega_{p3}}\left[\left(g_1(T_-) - g_1(t_p)\right)\left(\frac{\omega_z}{\omega_{p3}} - 1\right) + \omega_z(T_- - t_p)\right] + \frac{v_c(t_p)\omega_2}{\omega_{p3}}\left[\frac{\left(g_1(T_-) - g_1(t_p)\right)}{\omega_{p3}} + T_- - t_p\right]. \quad (24)$$

This integral (24) is derived from (16). Equations (8) to (24) are exact and they define the complete CPLL behavior. The accuracy of these expressions is verified through behavioral simulations and the results are shown in Section IV.

A. Linear Analysis

The state-space analysis presented so far captures the nonlinear acquisition process and the linear tracking as well. However, due to the nonlinear nature of all the equations describing the various state variables, the linear filtering behavior of the CPLL in the phase domain is not apparent. The steady-state small-signal analysis of the CPLL can be performed by approximating the nonlinear equations as linear equations using small-signal assumptions. This linearization process is described in the following. Since most of the expressions derived so far are in terms of $g_1(t)$ and $g_2(t)$, we first approximate them as follows using first-order Taylor's expansion:

$$g_1(t) = \exp(-\omega_{p3}t) \approx 1 - \omega_{p3}t \quad (25)$$

$$g_2(t) = \frac{1}{\omega_{p3}}\left(1 - \exp(-\omega_{p3}t)\right) \approx t. \quad (26)$$

When the CPLL is in near-lock condition, the phase error is very small and equivalently t_p is very small. In most design examples, the error is less than 0.1% in the two approximations above for $t = t_p$ if t_p is less than about 5% of the time period. Applying the approximations to the control and the capacitor voltages of (14) and (15), we get

$$v_{\text{ctrl}}(t_p) \approx v_{\text{ctrl}}(0) + \omega_2 t_p\left(v_c(0) - v_{\text{ctrl}}(0)\right) + \frac{i_p t_p}{C_2} \quad (27)$$

$$v_c(t_p) \approx v_c(0) + \omega_z t_p\left(v_{\text{ctrl}}(0) - v_c(0)\right). \quad (28)$$

A further approximation can be made for $v_c(0) \cong v_{\text{ctrl}}(0)$ (i.e., $t_p \ll T_-$), resulting in

$$v_{\text{ctrl}}(t_p) \approx v_{\text{ctrl}}(0) + \frac{i_p t_p}{C_2} \quad (29)$$

$$v_c(t_p) \approx v_c(0). \quad (30)$$

These approximations can be explained intuitively in the following manner. When the CPLL is in lock, the control voltage is exactly equal to the capacitor voltage. When the input phase is

perturbed by a small amount, a narrow pulse of width t_p is generated by the PFD. For a small t_p, roughly all of the CP current linearly charges the C_2 capacitor. Therefore, at the end of t_p, v_c does not change and $v_{\rm ctrl}$ is incremented by $i_p t_p/C_2$. At the end of the pulse, the CP current is off and then the charge redistribution occurs between the two capacitors C_1 and C_2 with a time constant approximately inversely proportional to the third pole frequency ω_{p3}. The capacitor voltages $v_{\rm ctrl}$ and v_c settle to approximately equal steady-state values. This is expressed in the follwoing equations:

$$v_{\rm ctrl}(T_-) \approx v_{\rm ctrl}(0)\left(a+\frac{C_2\,(1-a)}{C_1+C_2}\right)+v_c(0)\left(\frac{C_1(1-a)}{C_1+C_2}\right) + \frac{i_p t_p}{C_2}\left(a+\frac{C_2\,(1-a)}{C_1+C_2}\right) \tag{31}$$

$$v_c(T_-) \approx v_{\rm ctrl}(0)\left(\frac{C_2\,(1-a)}{C_1+C_2}\right)+v_c(0)\left(a+\frac{C_1\,(1-a)}{C_1+C_2}\right) + \frac{i_p t_p}{C_2}\left(\frac{C_2\,(1-a)}{C_1+C_2}\right) \tag{32}$$

where $a = \exp(-\omega_{p3}T)$. Note that when a is small, the two voltages $v_{\rm ctrl}(T_-)$ and $v_c(T_-)$ are equal. Similarly, applying the approximations from (25) and (26) to the integral of the control voltage (20) and (24), we get

$$\int_0^{t_p} v_{\rm ctrl}(\tau)d\tau \approx v_{\rm ctrl}(0)t_p + \frac{i_p}{C_2\omega_{p3}}\frac{\omega_z t_p^2}{2} \approx 0 \tag{33}$$

$$\begin{aligned}\int_{t_p}^{T_-} v_{\rm ctrl}(\tau)d\tau &\approx \frac{v_{\rm ctrl}(t_p)}{\omega_{p3}}\left(1-t_p\omega_{p3}-a+\omega_z\left(T_-+\frac{a-1}{\omega_{p3}}\right)\right) + \frac{v_c(t_p)\omega_2}{\omega_{p3}}\left(T_-+\frac{a-1}{\omega_{p3}}\right)\\ &\approx \frac{v_{\rm ctrl}(t_p)}{\omega_{p3}}\left(1-a+\omega_z\left(T_-+\frac{a-1}{\omega_{p3}}\right)\right) + \frac{v_c(t_p)\omega_2}{\omega_{p3}}\left(T_-+\frac{a-1}{\omega_{p3}}\right).\end{aligned} \tag{34}$$

The output phase can be linearized using the approximations presented while noting that $i_p t_p$ is equal to $I_{\rm cp}\theta_e/\omega_i$. The final expression merging the above equations into (9) is

$$\begin{aligned}\theta_o(T_-) &= \theta_o(0)+\omega_{fr}t+K_{\rm vco}\int_0^{T_-} v_{\rm ctrl}(\tau)d\tau \\ &\approx \theta_o(0)+\omega_{fr}t+\left(\frac{K_{\rm vco}\omega_2}{\omega_{p3}}\left(T_-+\frac{a-1}{\omega_{p3}}\right)\right)v_c(0) + \left(\frac{K_{\rm vco}}{\omega_{p3}}\left(1-a+\omega_1\left(T_-+\frac{a-1}{\omega_{p3}}\right)\right)\right) \cdot\left(v_{\rm ctrl}(0)+\frac{I_{\rm cp}(\theta_i-\theta_o)}{\omega_i C_2}\right).\end{aligned} \tag{35, 36}$$

Given the linearized approximations between various state variables, we can now derive the noise transfer functions of the CPLL.

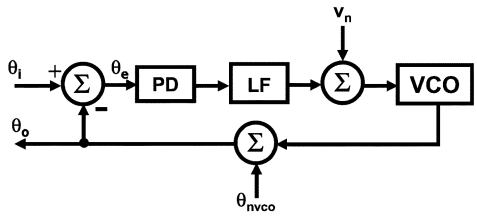


Fig. 5. Block diagram of the CPLL indicating various noise sources.

B. Noise Transfer Function Analysis

The output phase noise is of paramount importance in various applications. Even though phase noise is caused by various circuit-level parameters such as thermal and flicker noise of the transistors and power supply noise, it is important to analyze the shaping of the noise injected at the various nodes of the CPLL as shown in Fig. 5. In this figure, v_n represents the control voltage noise and $\theta_{n\rm vco}$ represents VCO phase noise. The input jitter transfer function of the PLL can be derived by taking z-transforms on both sides of (31), (32), and (36), resulting in the following equations:

$$v_{\rm ctrl}(z)=\frac{v_c(z)\left(\frac{C_1(1-a)}{C_1+C_2}\right)+(\theta_i(z)-\theta_o(z))\frac{I_{\rm cp}}{\omega_i C_2}\left(a+\frac{C_2(1-a)}{C_1+C_2}\right)}{\left(z-a-\frac{C_1\cdot(1-a)}{C_1+C_2}\right)} \tag{37}$$

$$v_c(z)=\frac{v_{\rm ctrl}(z)\left(\frac{C_2(1-a)}{C_1+C_2}\right)+(\theta_i(z)-\theta_o(z))\frac{I_{\rm cp}}{\omega_i C_2}\left(\frac{C_2(1-a)}{C_1+C_2}\right)}{\left(z-a-\frac{C_1\cdot(1-a)}{C_1+C_2}\right)} \tag{38}$$

$$\begin{aligned}z\,\theta_o(z)=&\theta_o(z)+v_c(z)\left(\frac{K_{\rm vco}\omega_2}{\omega_{p3}}\cdot\left(T_-+\frac{a-1}{\omega_{p3}}\right)\right) + \left(\frac{K_{\rm vco}}{\omega_{p3}}\left(1-a+\omega_1\left(T_-+\frac{a-1}{\omega_{p3}}\right)\right)\right) \cdot\left(v_{\rm ctrl}(z)+\frac{I_{\rm cp}(\theta_i(z)-\theta_o(z))}{\omega_i C_2}\right).\end{aligned} \tag{39}$$

Solving the above three equations yields the input jitter transfer function shown in (40) at the bottom of the page, where $K = K_{\rm vco}I_{\rm cp}RC_1/(\omega_i\,(C_1+C_2))$. Recall that $a = \exp(-\omega_{p3}T)$. Similarly, the VCO output phase noise transfer function can be derived to yield (41) shown at the bottom of the next page. In order to arrive at the control voltage noise transfer function, we rewrite the output phase state equation (36) in the presence of the control voltage noise as

$$\begin{aligned}\theta_o(T_-) =&\theta_o(0)+\left(\frac{K_{\rm vco}}{\omega_1+\omega_2}\left(1-a+\omega_1\left(T_-+\frac{a-1}{\omega_1+\omega_2}\right)\right)\right) \cdot\left(v_{\rm ctrl}(0)+\frac{i_p t_p}{C_2}\right)+\left(\frac{K_{\rm vco}\omega_2}{\omega_1+\omega_2}\left(T_-+\frac{a-1}{\omega_1+\omega_2}\right)\right)v_c(0) \\ &+K_{\rm vco}\int_0^{T_-} v_n(\tau)d\tau\,.\end{aligned} \tag{42}$$

$$\frac{\theta_o(z)}{\theta_i(z)}=\frac{K\left(z^2\left(\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right)-z\left(\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi a}{RC_1\omega_i}\right)\right)}{z^3+\left(-a-2+K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right]\right)z^2+\left(2a+1-K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi a}{RC_1\omega_i}\right]\right)z-a} \tag{40}$$

As is apparent in the above expression, the VCO converts the control voltage noise to phase noise by an integrating operation. The integral can be replaced by its Laplace transform $1/s$ and a mixed s/z-domain transfer function can be derived to yield (43) shown at the bottom of the page. This transfer function can be interpreted as follows. A small change in the control voltage with frequency ω, results in an output phase disturbance with the same frequency ω obtained by evaluating the above expression at $s = j\omega$ and $z = e^{j\omega T}$. Having derived various transfer functions, we will now derive the jitter transfer function using the impulse invariance method in order to compare with the state-space method.

C. Equivalence to Impulse Invariant Transformation

The impulse-invariant transformation was first used in [9] to incorporate the discrete-time nature of the PFD in a second-order CPLL. We will extend that analysis to a more practical third-order CPLL. The basic premise of using impulse-invariant transformation to map the continuous-time s-domain model into the z-domain is that the error pulses generated by the PFD are so narrow that we can effectively approximate the PFD output as an impulse train. This transformation is illustrated in Fig. 6. The procedure to map the s-domain model into the z-domain using impulse-invariant transformation can be summarized in following three steps.

1. Calculate the impulse response $LG_3(t)$ corresponding to the transfer function $LG_3(s)$.
2. Sample the impulse response $LG_3(t)$ using a periodic impulse train to get the sampled impulse response $LG_3(nT)$.
3. Calculate the z-transform of $LG_3(nT)$ to obtain the discrete-time transfer function $LG_3(z)$.

The discrete-time loop-gain transfer function is obtained using the above procedure and the final result is given by

$$LG_3(z) = K\frac{z^2\left(\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right)-z\left(\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}a\right)}{z^3-z^2(2+a)+z(1+2a)-a}. \tag{44}$$

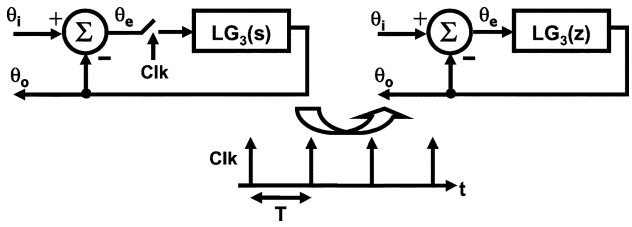


Fig. 6. Impulse-invariant transformation of a s-domain CPLL.

The closed-loop transfer function $\theta_o(z)/\theta_i(z) = LG_3(z)/(1+LG_3(z))$ calculated using (44) is shown in (45) at the bottom of the page. It is interesting to note that the input jitter transfer function calculated using the linearized state-space equations (40) is identical to the input to output jitter transfer function calculated using the impulse-invariant transformation for a third-order CPLL.

In the case of a second-order CPLL, the z-domain transfer functions derived using the impulse-invariant transformation [9] and the linearized state-space analysis [10] are not the same. This can be explained intuitively in the following manner. In a truly second-order CPLL ($C_2 = 0$), the ripple on the control voltage depends on the magnitude and sign of the phase error resulting in a highly nonlinear behavior. Thus, it cannot be accounted for by a linear analysis. However, we have noticed in the simulation environment that even a very small ripple bypass capacitor ($C_2 > 50$ fF) sufficiently reduces the nonlinearity (the ripples) on the control voltage and the z-domain transfer function accurately models the resulting third-order CPLL. As mentioned earlier, one comforting point to note here is that no CPLL system is second order. Even without the use of a ripple bypass capacitor, there will always be an equivalent capacitor C_2 due to circuit parasitics (e.g., CP output, VCO input, etc.).

D. Stability Analysis

The stability of the CPLL depends primarily on the loop-gain phase margin and the reference frequency. The instability due to an inadequate phase margin is accurately predicted by the

$$\frac{\theta_o(z)}{\theta_{n\mathrm{vco}}(z)} = \frac{z^3-(a+2)z^2+(2a+1)z-a}{z^3+\left(-a-2+K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right]\right)z^2+\left(2a+1-K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi a}{RC_1\omega_i}\right]\right)z-a} \tag{41}$$

$$\frac{\theta_o(z)}{v_n(s)} = \frac{\left(z^3-(a+2)z^2+(2a+1)z-a\right)\frac{K_{\mathrm{vco}}}{s}}{z^3+\left(-a-2+K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right]\right)z^2+\left(2a+1-K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi a}{RC_1\omega_i}\right]\right)z-a} \tag{43}$$

$$\frac{\theta_o(z)}{\theta_i(z)} = \frac{K\left(z^2\left(\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right)-z\left(\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi a}{RC_1\omega_i}\right)\right)}{z^3+\left(-a-2+K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi}{RC_1\omega_i}\right]\right)z^2+\left(2a+1-K\left[\frac{C_1(1-a)}{C_1+C_2}+\frac{2\pi a}{RC_1\omega_i}\right]\right)z-a} \tag{45}$$

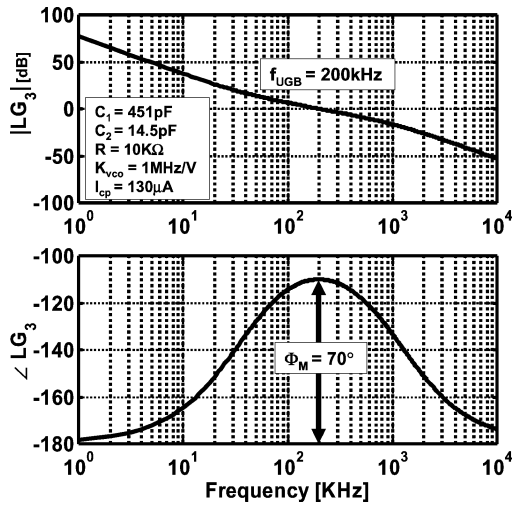


Fig. 7. Loop gain Bode plot and the corresponding loop parameters.

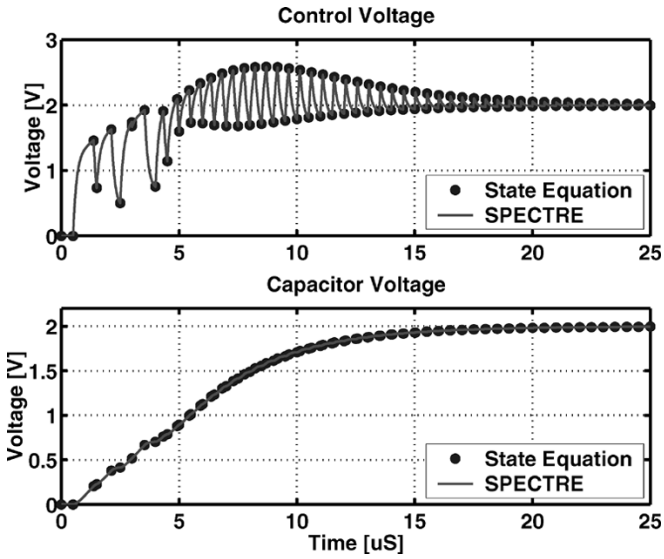


Fig. 8. Control voltage and capacitor voltage settling simulation. The state equations and SPECTRE simulations give identical results.

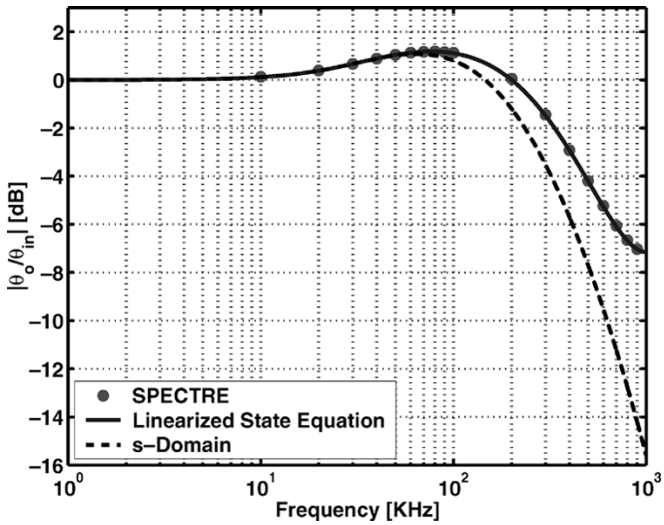


Fig. 9. Jitter transfer function with $F_{\rm in} = 2$ MHz ($10\times$ loop bandwidth).

s-domain analysis. However, the discrete-time analysis such as the one proposed in the previous section is required to explain the instability caused due to an increased PLL loop bandwidth for a given PFD update rate/frequency. Intuitively, when the PFD update frequency is comparable to the loop bandwidth, the delay around the feed back loop introduces excessive phase shift which can lead to instability. This can also be explained mathematically by the root locus analysis of the poles of the z-domain jitter transfer function. The CPLL is unstable when the poles are outside the unit circle. This is illustrated along with other simulations in the next section.

IV. Behavioral Simulations

The results derived in the previous section are now verified in behavioral simulations. Using SPECTRE, the PFD and the VCO are designed in a hardware description language (HDL) while the CP and loop filter are built using ideal circuit elements. Such behavioral models provide the advantage of short simulation time without compromising the fundamental functionality of a CPLL architecture. In these behavioral simulations, the CPLL is designed for a loop bandwidth of 200 kHz and a loop phase margin of 70°. The corresponding loop parameters are chosen using the design methodology described in Section III.A. The loop-gain Bode plot using the calculated parameters is shown in Fig. 7. The state-space model of the CPLL is simulated using the state equations (8)–(24) described in Section III using MATLAB. The validity of the state equations during lock acquisition is verified by comparing the control voltage and the capacitor voltage obtained from MATLAB and SPECTRE simulations. The simulation results for an input/VCO frequency of 2 MHz (PFD update rate) are shown in Fig. 8. The match between theoretical calculations and the SPECTRE simulations shows the accuracy of the state equations.

Having demonstrated the *large-signal* accuracy of the state equations we will now verify the *small-signal* accuracy of the linearized state equations. This is performed by injecting a small signal sinusoid input at the node of interest and measuring the output. For example, in the case of the input jitter transfer function, the input/reference is phase modulated with a sinusoid of amplitude 0.01 rad and the output phase modulation is measured in the steady-state (locked) condition. The simulated input jitter transfer function is shown in Fig. 9 for a PFD update frequency of 2 MHz which is ten times the loop bandwidth of 200 kHz. Note that the jitter peaking due to the inherent sampling behavior is not predicted by the s-domain analysis while it is accurately predicted by the linearized state-equation model. This jitter peaking is proportional to the loop delay around the feedback, hence, this peaking becomes worse at lower sampling rates or at higher loop bandwidths for a fixed sampling rate (i.e., at lower PFD update frequency to loop bandwidth ratios). Due to the same reason the s-domain analysis accurately models the real system under high over sampling conditions (i.e., higher PFD update frequency to loop bandwidth ratios). These two cases are verified in simulation and the results are summarized in Figs. 10 and 11.

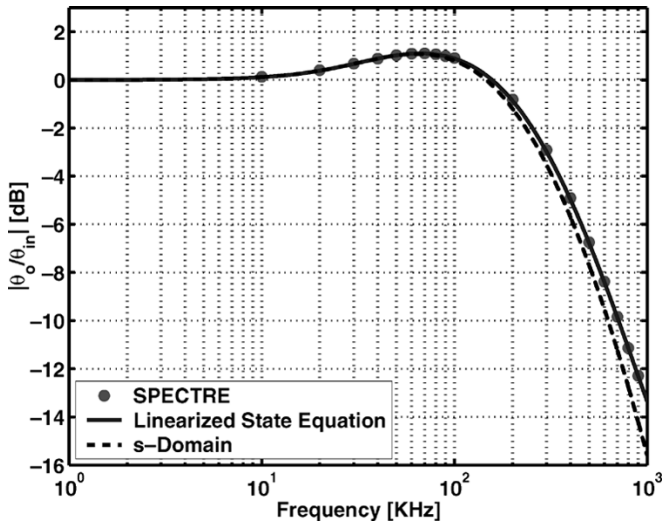


Fig. 10. Jitter transfer function with $F_{\rm in} = 4$ MHz (20 × loop bandwidth).

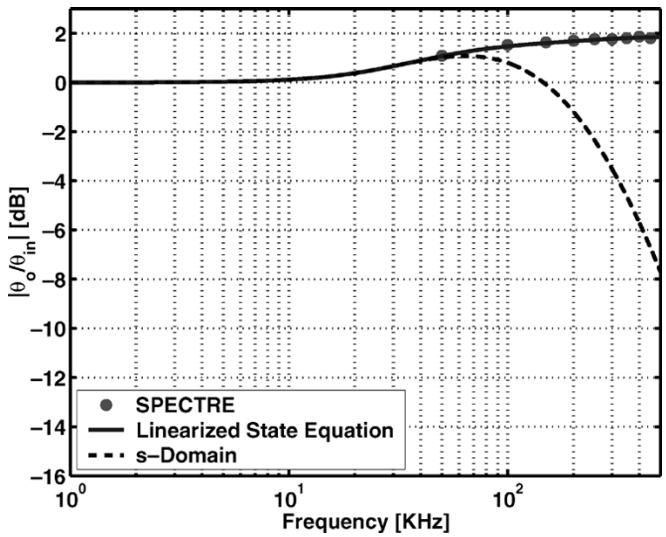


Fig. 11. Jitter transfer function with $F_{\rm in} = 1.2$ MHz (6 × loop bandwidth).

The control voltage (VCO input) noise and the VCO output phase noise to the PLL output transfer functions are also simulated and the results are shown in Figs. 12 and 13, respectively. In the case of the control voltage to output transfer function, a 1-mV sinusoid noise voltage was added to the control voltage. For the VCO output phase noise to the PLL output transfer function, a VCO with a phase noise tone of amplitude 0.01 radians at the modulating frequency is used. Again, the transfer functions match well with the expressions derived using the linearized state equations.

The stability limit of the CPLL is determined by plotting the pole locus of the jitter transfer function as shown in Fig. 14. For this particular CPLL, the loop goes unstable when the ratio of the reference frequency to the loop bandwidth is around 3. However, the pole location depends not only on the reference frequency but also on the loop parameters. The variation of the stability limit with loop parameters is not obvious. This variation can be quantified by looking at the stability limit (PFD update frequency to loop bandwidth ratio) variation versus the phase margin as shown in Fig. 15. It is interesting to note that the

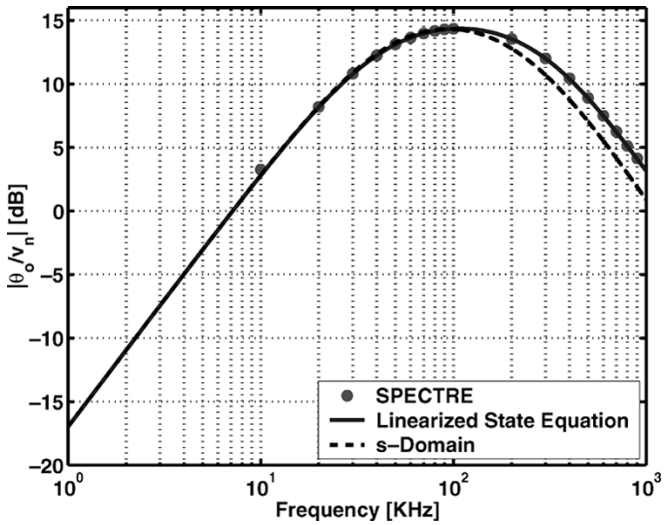


Fig. 12. Simulated control voltage noise transfer function $F_{\rm in} = 2$ MHz.

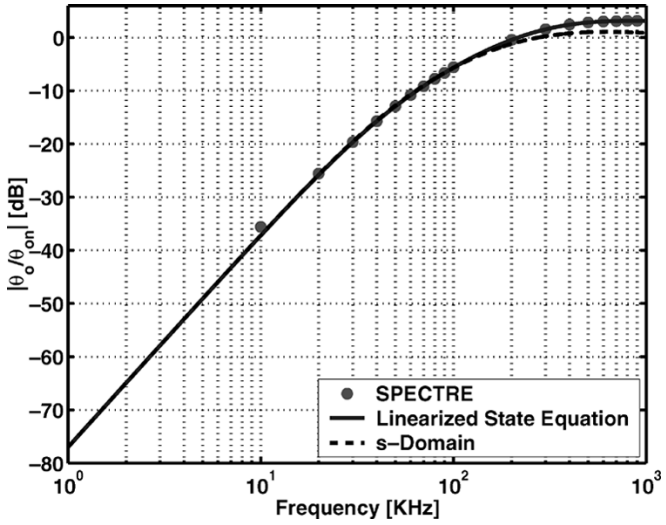


Fig. 13. Simulated VCO phase noise transfer function with $F_{\rm in} = 2$ MHz.

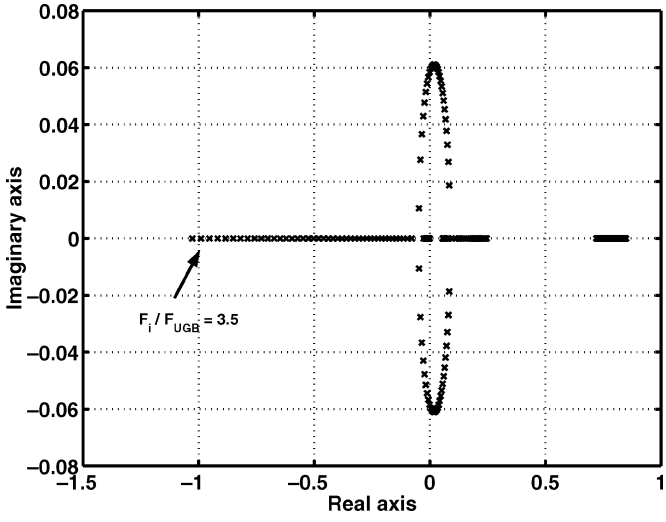


Fig. 14. Pole locus for $F_{\rm in} = 2$ MHz and $\Phi_M = 70°$.

stability limit is nominally constant for various loop parameters and is primarily defined by the reference (PFD) frequency to

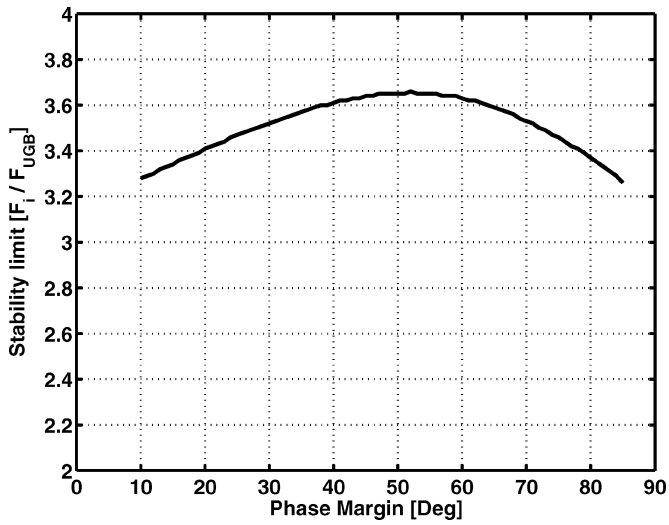


Fig. 15. Stability limit variation with phase margin.

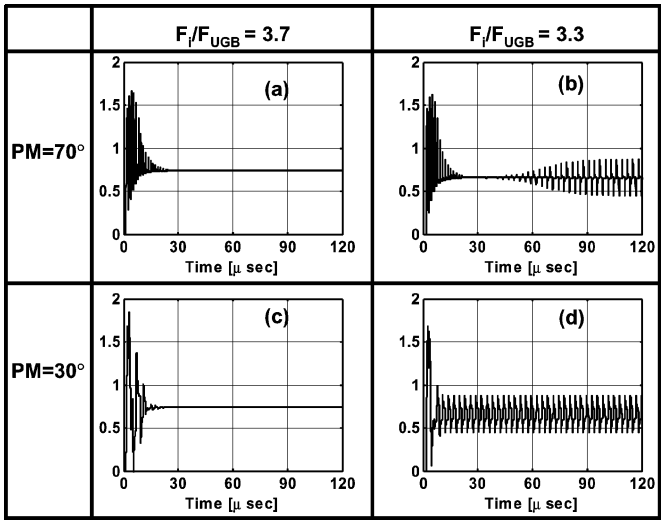


Fig. 16. Control voltage settling behavior for different update rates and phase margins. (a) Phase margin $= 70^\circ$ and $F_i/F_{UGB} = 3.7$. (b) Phase margin $= 70^\circ$ and $F_i/F_{UGB} = 3.3$. (c) Phase margin $= 30^\circ$ and $F_i/F_{UGB} = 3.7$. (d) Phase margin $= 30^\circ$ and $F_i/F_{UGB} = 3.3$.

loop bandwidth ratio. This observation is further verified using transient simulations and the results from two representative cases are shown in Fig. 16. Shown in Fig. 16(a) and (b) is the control voltage settling behavior when the phase margin is 70° and the update rates are equal to 3.7 and 3.3 times the loop bandwidth, respectively. It can be seen that the loop is stable when the ratio of the update rate to the loop bandwidth is equal to 3.7 while it is unstable when this ratio is equal to 3.3. Note that the instability due to the lower sampling rate manifests itself as an over-correction or as an under-correction by the feedback loop. Similar simulation results for a phase margin of 30° are shown in Fig. 16(c) and (d). It is clear from these simulation results that the stability limit due to sampling is independent of the loop parameters for a given update rate.

V. Conclusion

The dynamics of PLLs can be accurately described using state equations derived from first principles. The analysis of a third-order CPLL is presented in detail using the state equations. This generic analysis can be extended to other PLL systems. The state equations accurately model both the transient lock acquisition and the steady-state tracking behavior of the CPLL. Since it is common practice to use transfer functions to analyze the linearized behavior under small-signal conditions, the nonlinear state equations are linearized and the z-domain noise transfer functions are derived. It is shown that the z-domain jitter transfer function derived using the impulse-invariant transformation is the same as the one derived using the linearized state equations. However, unlike the impulse-invariant method, the state-space analysis provides useful insight into the approximations used to arrive at the jitter transfer functions. Finally, behavioral simulations in SPECTRE and MATLAB indicate excellent correlation between the state-space analysis and the practical PLL system.

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References

[1] I. Young, J. Greason, and K. Wong, "PLL clock generator with 5 to 10 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1599–1607, Nov. 1992.

[2] H. Ahn and D. Allstot, "A low-jitter 1.9-V CMOS PLL for UltraSPARC microprocessor applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 450–454, Mar. 2000.

[3] V. Kaenel, "A high-speed, low-power clock generator for a microprocessor application," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1634–1639, Nov. 1998.

[4] H. Rategh, H. Samavati, and T. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver," *IEEE J. Solid-State Circuits*, vol. 35, pp. 780–787, May 2000.

[5] J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2054–2065, Dec. 1998.

[6] M. Meghelli, B. Parker, H. Ainspan, and M. Soyuer, "SiGe BiCMOS 3.3-V clock and data recovery circuits for 10-Gb/s serial transmission systems," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1992–1995, Dec. 2000.

[7] K. Lee, S. Kim, G. Ahn, and D. Jeong, "A CMOS serial link for fully duplexed data communication," *IEEE J. Solid-State Circuits*, vol. 30, pp. 353–364, Apr. 1995.

[8] S. Miyazawa, R. Horita, K. Hase, K. Kato, and S. Kojima, "A BiCMOS PLL-based data separator circuit with high stability and accuracy," *IEEE J. Solid-State Circuits*, vol. 26, pp. 116–121, Feb. 1991.

[9] J. Hein and J. Scott, "z-domain model for discrete-time PLLs," *IEEE Trans. Circuits Syst.*, vol. 35, pp. 1393–1400, Nov. 1988.

[10] F. Gardner, "Charge pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849–1858, Nov 1980.

[11] I. Novof, J. Austin, R. Kelkar, D. Strayer, and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and ± 50 ps jitter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1259–1266, Nov. 1995.

[12] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1723–1732, Nov. 1996.

[13] M. Perrott, "Fast and accurate behavioral simulation of fractional-N frequency synthesizers and other PLL/DLL circuits," in *Proc. Design Automation Conf.*, June 2002, pp. 498–503.

[14] V. von Kaenel, D. Aebischer, C. Piguet, and E. Dijkstra, "A 320 MHz, 1.5 mW@1.35 V CMOS PLL for microprocessor clock generation," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1715–1722, Nov 1996.

[15] H. Yang, K. Lee, and R. Co, "A low jitter 0.3–165 MHz CMOS PLL frequency synthesizer for 3 V/5 V operation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 582–586, Apr. 1997.

[16] L. Lin, L. Tee, and P. Gray, "A 1.4 GHz differential low-noise CMOS frequency synthesizer using a wideband PLL architecture," *Dig. Tech. Papers ISSCC*, pp. 204–205, Feb. 2000.
[17] M. Perrott, T. Tewksbury, and C. Sodini, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2048–2060, Dec. 1997.
[18] C. Chen, *Linear System Theory and Design*, 3rd ed. Oxford, U.K.: Oxford University Press, 1999.

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