Background Digital Calibration Techniques for Pipelined ADC's

Un-Ku Moon and Bang-Sup Song

***Abstract*— A skip and fill algorithm is developed to digitally self-calibrate pipelined analog-to-digital converters (ADC's) in real time. The proposed digital calibration technique is applicable to capacitor-ratioed multiplying digital-to-analog converters (MDAC's) commonly used in multistep or pipelined ADC's. This background calibration process can replace, in effect, a trimming procedure usually done in the factory with a hidden electronic calibration. Unlike other self-calibration techniques working in the foreground, the proposed technique is based on the concept of skipping conversion cycles randomly but filling in data later by nonlinear interpolation. This opens up the feasibility of digitally implementing calibration hardware and simplifying the task of self-calibrating multistep or pipelined ADC's. The proposed method improves the performance of the inherently fast ADC's by maintaining simple system architectures. To measure errors resulting from capacitor mismatch, op amp dc gain, offset, and switch feedthrough in real time, the calibration test signal is injected in place of the input signal using a split-reference injection technique. Ultimately, the missing signal within two-thirds of the Nyquist bandwidth is recovered with 16-b accuracy using a forty-fourth order polynomial interpolation, behaving essentially as an FIR filter.**

***Index Terms*— Analog–digital converters, calibration, pipeline processing.**

I. Introduction

DIGITAL PROCESSING applications in modern high-resolution video and graphics, ultrasonic imaging, and wireless communications have created a need for very high-speed but high-resolution ADC's with extremely wide dynamic range. High-resolution ADC's, limited by component mismatch, have relied on a variety of circuit techniques to improve linearity. Self-calibration techniques, for example, have been developed to measure capacitor ratio errors and to subtract the code errors calculated from the measured capacitor ratio errors during the normal operation. Although the code errors are computed digitally in these early self-calibration techniques, the measured errors are actually subtracted in the analog domain using a separate calibration DAC [1]–[4], or physically trimming capacitor sizes [5]. In recent years, digital calibration techniques have been introduced so that the error subtraction may be done digitally to relieve the accuracy requirements of analog calibration circuits, thereby enabling higher-speed operation [6]–[8]. On the other hand, oversampling ADC's are promising for high-resolution applications, but their upper range of the Nyquist sampling rate is limited to several MHz even with 50 MHz sampling rate [9]. As a result, there is a renewed interest in the Nyquist-rate ADC to achieve a high sampling rate above several MHz either using an analog circuit technique [10] or using a digital calibration technique [11].

All existing calibration techniques are *foreground* techniques, implying that the normal operation should be interrupted to start a calibration cycle. Usually measurement cycles in self-calibration can be completed just after power is turned on, but any miscalibration or sudden environmental changes such as power supply or temperature may make the measured errors invalid. Many communication as well as video and imaging applications have predetermined stand-by modes in which the ADC can be placed in idling or in calibration. However, the ideal solution to this is to operate calibration circuits all the time synchronously so that measurement cycles may be hidden in background and be transparent to the normal operation. This process is called *background* technique.

Concepts equivalent to the background calibration can be found in analog techniques such as a sampled-reference DAC [12] and a sampled-current source DAC [13], that refresh voltage or current samples periodically to maintain accurate values. However, analog techniques relying on sampled voltages or currents are sensitive to analog processing inaccuracies, and demand premium care in design. Therefore, background digital calibration may be more robust in practical applications, and it is easier to achieve high-frequency performance by adding real-time trimming circuits operating in the background and leaving fast original architectures intact. This approach can benefit both from the speed advantage of conventional architectures and from the sophisticated digital processing capability of scaled CMOS technologies. The first background digital calibration concept has been demonstrated using a resistor-string DAC, calibrated by a highly accurate 2^{16} times oversampling first-order delta-sigma converter to measure resistor ratio errors [11].

An effort to apply the background calibration concept to the capacitor DAC raises a fundamental question on how capacitors that hold signal charges can be calibrated. Our approach to this seemingly unsolvable problem is to randomly skip conversion cycles and fill in the missing samples with nonlinearly interpolated data. The calibration procedure is to apply a known calibration voltage, usually $\pm V_{ref}/2$, to different stages of the ADC to generate the associated nonlinear

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components and to estimate them accurately for nonlinearity computations. The proposed technique can be applied to any multistep or pipelined converter with digital correction [14], but for simplicity, a 1-b pipelined converter is chosen for this paper [15]. Since the calibration voltage injected into a specific stage experiences a path gain set by the capacitor ratios along the signal path, the gain error of the path can be measured indirectly by measuring the gain of the calibration voltage. To estimate the missing digital output, a hardware-efficient interpolation algorithm is proposed. It is similar to an algorithm described in [16].

In Section II, a general description is given on the calibration method, computation, and storing of error terms. Skip and fill cycles for the background calibration are covered in Section III. Details and net results of the nonlinear interpolation method and its limitations are covered in Section IV, and considerations in interpolation related to the quantization effects (finite resolution and linearity) are discussed in Section V.

II. Calibration of Pipelined ADC's

A. Error Sources of Pipelined ADC's

A multiply-by-2 functional block (2-b MDAC) using two identical capacitors, as shown in Fig. 1, has been used as a pipelined ADC building block [17]. If three DAC levels are used, the input reference added to this multiply-by-2 residue amplifier is V_{ref}, 0, or $-V_{ref}$ [15]. According to the schematic in Fig. 1, at each stage, after the input is first sampled on the bottom plates of capacitors and the op amp offset is sampled at the top plates, the input nodes are switched to 0, $+V_{ref}$, or $-V_{ref}$ in the following phase of the clock cycle. After the op amp settles, the corresponding output voltages become $2V_{in}$, $2V_{in} - V_{ref}$, or $2V_{in} + V_{ref}$, if the capacitor mismatch coefficient α is ignored for the moment. Given this, we can observe the entire pipelined 1-b/stage ADC with a systematic approach, as shown in Fig. 2. Simple summing nodes and gain paths, expressed by multiplying nodes or by solid triangles similar to the signal-flow graph, summarize the whole system. It is evident from the figure that the nonideal terms including capacitor mismatch errors, offsets, and op amp dc gain errors are denoted by the extra terms α_i, o_i, and δ_i, respectively. Because of these error terms, the converter would require some sort of calibration.

On a side note, the finite dc gain errors δ_i will always be negative numbers. The op amp dc gain has been known as a key design issue of high-resolution converters, but in the background calibration, the op amp gain can be canceled together with the capacitor errors as far as the gain is linear. Even the gain drift is not a major concern because measurement data are constantly updated while the converter is in operation.

Two fundamental error sources of nonlinearity errors have been identified: capacitor mismatch error and finite gain error. At 16-b level, however, the input dependence of sampling switches in CMOS can limit the nonlinearity of ADC's as well. Also, for converters with a resolution of 12 b or above, kT/C noise determines the size of the capacitors rather than matching. Although these are important design issues, they are not covered in this paper.

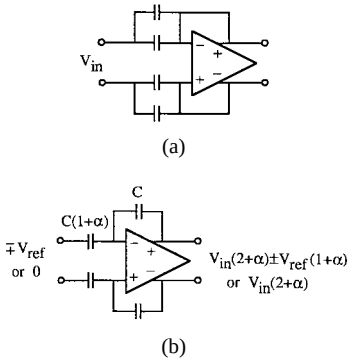


Fig. 1. Multiply-by-2 residue amplifier: (a) Sampling phase. (b) Amplification phase.

B. Calibration Principle

To see how the calibration process works, refer to Fig. 2. Seeing that a fixed number of the lower bits are inherently linear to its required resolution (say about 8-b for example), we will only need to calibrate upper bits above and beyond this inherent resolution and linearity. These inherently satisfactory lower bits can be viewed as an ideal ADC for convenience in analysis, as delineated in the figure. To calibrate the upper bits, the actual gain for each of the reference paths should be measured and compared to the ideal value. The reference paths are referred to as V_{cal-1}, V_{cal-2}, and V_{cal-3} from the right in the three-stage calibration example of Fig. 2. The difference can be stored in memory, and during normal operation, the stored error terms can be used to deliver the digitally-calibrated data.

Analyzing one path at a time, we see that each path sees an ideal gain plus some additional gain error. The gain seen from the input V_i to the input of the ideal ADC is

$$(2+\alpha_3)(1+\delta_3)(2+\alpha_2)(1+\delta_2)(2+\alpha_1)(1+\delta_1) = 8+\epsilon_i. \quad (1)$$

The actual gain has an error of ϵ_i from the ideal gain, 8. In this case, the input gain error imposes no real problem to the overall linearity of the converter. But the gain seen by each of the reference points (V_{cal-i}) has great importance to the overall linearity. The gain seen by V_{cal-1}, V_{cal-2}, and V_{cal-3}, are

$$\begin{aligned}&(1+\alpha_1)(1+\delta_1) = 1+\epsilon_1,\\ &(1+\alpha_2)(1+\delta_2)(2+\alpha_1)(1+\delta_1) = 2+\epsilon_2, \text{ and}\\ &(1+\alpha_3)(1+\delta_3)(2+\alpha_2)(1+\delta_2)(2+\alpha_1)(1+\delta_1) = 4+\epsilon_3.\end{aligned} \quad (2)$$

Also having the measure of the total offset, this yields from the figure

$$\begin{aligned}&o_3(1+\delta_3)(2+\alpha_2)(1+\delta_2)(2+\alpha_1)(1+\delta_1)\\ &+ o_2(1+\delta_2)(2+\alpha_1)(1+\delta_1) + o_1(1+\delta_1)\\ &= o_3(4+\epsilon_{o3}) + o_2(2+\epsilon_{o2}) + o_1(1+\epsilon_{o1})\\ &= V_{\text{offset}}.\end{aligned} \quad (3)$$

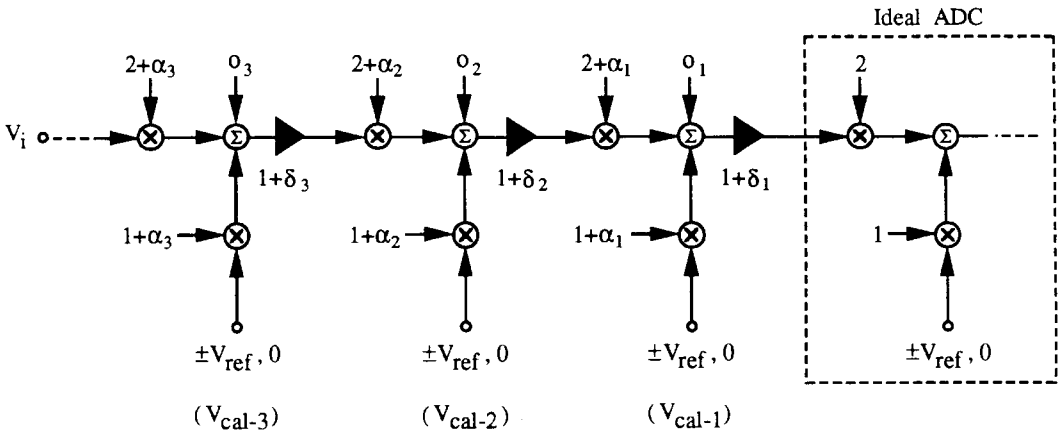


Fig. 2. Model of a pipelined ADC with error sources.

The errors can be easily compensated in the digital-domain. For example, if the reference voltages are set to $[+V_{ref}, -V_{ref}, +V_{ref}]$ for the digital code "101," the total code error would be

$$Error(+1,-1,+1) = -(\epsilon_3 - \epsilon_2 + \epsilon_1)V_{ref} - V_{offset}. \quad (4)$$

This implies that the converter, once calibrated, has an equal voltage step of V_{ref} at the input of the ideal ADC as the digital input code changes by 1. It is identical in concept to the digital code-error calibration principle [6], [8]. Since the constant offset does not affect ADC linearity, it does not need calibration for most applications.

C. Error Measurement Cycles

Even though the discussion of the error measurement approach has been directed in reference to the signal measured (or seen) at the "ideal ADC" (lower bits), the practical implementation cannot allow each of the gain paths to be greater than 1. Recall that the given nominal/ideal gains for the calibration voltages V_{cal-1}, V_{cal-2}, and V_{cal-3} are 1, 2, and 4, respectively. In reality, each of the calibration gain paths will be measured not only by the "ideal ADC" but also by the previously calibrated bits. For example, the calibration path gain measurement for V_{cal-3} is accomplished by using the previously calibrated bits, which are the paths corresponding to V_{cal-2} and V_{cal-1}. Therefore, the calibration procedure to measure errors starts from the low resolution bit. In general terms, the ADC is calibrated progressively from the less-significant-bit side.

To measure the gain error of a stage, any known calibration voltage, which is smaller than V_{ref}, is amplified to yield an output of $(2^{i-1} + \epsilon_i)V_{cal-i} + V_{offset-i}$ as in (2), where the constant offset error includes the switch feedthrough voltage of the current stage. This output voltage is measured using the following stages assuming that all stages up to the current stage are either ideal or precalibrated. After this measurement, the negative calibration voltage is similarly applied. Then the output voltage becomes $-(2^{i-1}+\epsilon_i)V_{cal-i}+V_{offset-i}$, assuming the offset stays constant. Note that the negative calibration voltage with the same magnitude generates an error with the opposite sign except for the offset term. Therefore, the gain errors can be obtained by subtracting these two measurements. The final bit errors for this three-stage calibration case are obtained after V_{cal}, $2V_{cal}$, and $4V_{cal}$ are digitally subtracted, assuming all three calibration voltages equal V_{cal}. Since the calibration voltage is a fraction of V_{ref}, the bit errors computed should be scaled by the ratio of V_{ref}/V_{cal} to make full-scale bit errors. This kind of error scaling (to the full scale) is not necessary if the split-reference injection technique is used. This technique is described in the paragraphs below. From three bit errors, all eight code errors can be digitally computed as in (4). Errors can be stored either as code errors or as bit errors. As is true in all digital processing, two extra bits are required to make up for the digital truncation error.

D. Split-Reference Injection Technique

Considering offsets and gain errors, V_{cal-i} cannot be the full reference value $\pm V_{ref}$ unless a radix less than 2 is used to keep the conversion range within $\pm V_{ref}$ [7]. Therefore, a fraction of the reference voltage, for example $\pm V_{ref}/2$, must be used. Because the un-calibrated lower bits operate with $\pm V_{ref}$, it becomes important that the fraction of the V_{ref} used for calibration is accurate. It is true that a calibration voltage lower than the reference voltage need not be generated if the op amp gain is high enough, because it is possible to separate the op amp gain error from the capacitor mismatch error. For example, assume that the feedback pair of capacitors in Fig. 1 samples $-V_{ref}$ during the sampling phase while the input pair samples V_{ref}. If the capacitors are switched to 0 in the following clock phase, nonzero residue output will result only from capacitor mismatch error (not from finite op-amp gain). However, in the background calibration, the gain error needs to be measured so that it can be constantly calibrated. Therefore, an accurate calibration voltage, which should be less than V_{ref}, needs to be generated. In this paper, a split-reference injection technique is devised to use the full reference voltage in two different paths with a gain of 1/2 each, as described in the following.

Because it is nearly impossible to create a fraction of the reference voltage, for example $V_{cal} = \pm V_{ref}/2$, at the equivalent accuracy level of the final ADC linearity, an alternate circuit topology may be used. Shown in Fig. 3 is

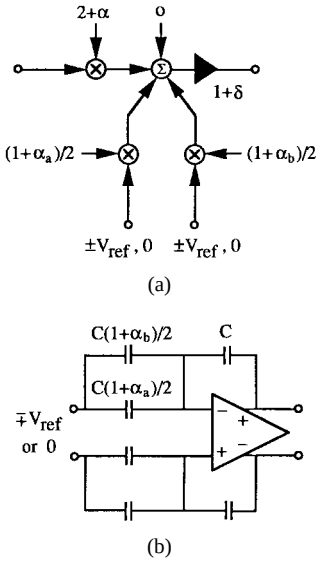


Fig. 3. Split-reference injection technique: (a) Error model and (b) modified residue amplifier.

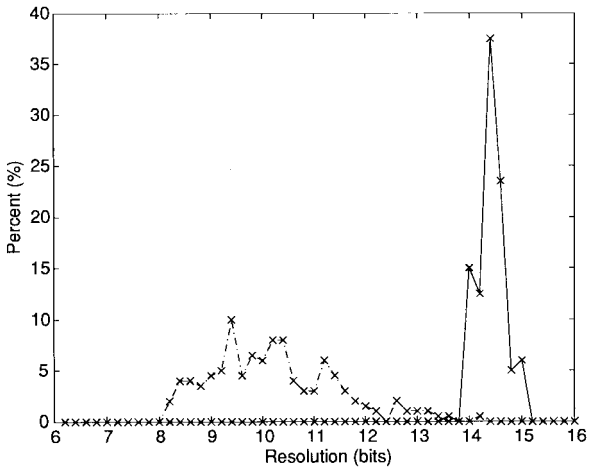


Fig. 4. Probability density from Monte Carlo behavioral simulations. Dashed and solid lines show the difference in DNL before and after calibration.

a circuit implementation which would allow the use of the reference voltage in two steps. Two half-size input capacitors are used as one input sampling capacitor for the input signal, but in the calibration mode, the full reference voltage is applied to one of the half-size input capacitors at a time while the other is grounded. The net result is that it will make available a fraction (1/2 in this case) of the full reference voltage, V_{ref}. Naturally, due to the mismatches of the two half-size capacitors, each capacitor mismatch coefficient (α_a and α_b in the figure) needs to be calibrated separately. As shown by the systematic block description on the left hand side of the figure, the calibration path is simply subdivided into two paths. The average of the two capacitor mismatch coefficients $(\alpha_a+\alpha_b)/2$ is simply equivalent to a single coefficient α if viewed as a single calibration path.

To verify the functionality of the calibration topology, a C-program for the Monte Carlo behavioral simulations of the ADC is used. The $\pm V_{cal-i}$ used is a $\pm V_{ref}/2$, corresponding

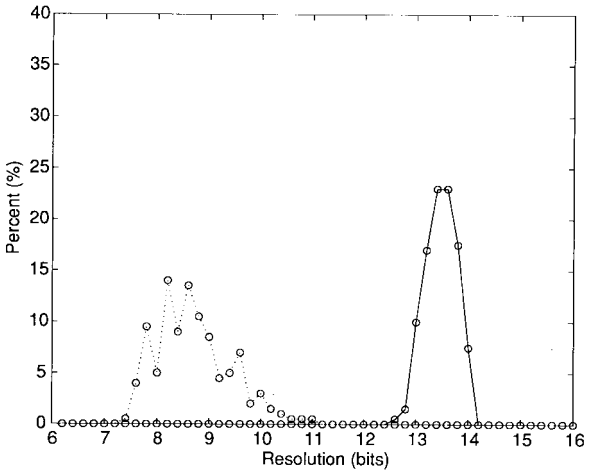


Fig. 5. Probability density from Monte Carlo behavioral simulations. Dashed and solid lines show the difference in INL before and after calibration.

to the modified implementation shown in Fig. 3. Shown in Figs. 4 and 5 are the "before and after" picture of the differential and integral nonlinearities. The simulated ADC is made of an 8-b "ideal ADC" (un-calibrated lower bits) plus 8-b calibrated upper bits.

III. Principle of Background Calibration

We were able to observe in the previous section that the 1-b/stage pipelined ADC can be calibrated to improve linearity from the matching limit. This was done simply by measuring the gain error of each bit by the calibrated lower bits and adjusting the digital word by the appropriate correction term in the digital-domain. The challenge in making this calibration scheme work in the background is to somehow make available the same kind of measurement opportunity while the converter is operating.

Simply speaking, the skip-cycle background calibration refers to the technique where a conversion cycle is stolen for the calibration measurement. In a certain sense, it is similar to the time-interleaved calibration. For example, converters work with a 50% duty cycle while the other 50% is devoted to calibration. This simple arrangement can multiplex two different modes of operation in time, but the sampling rate is reduced by half at least while the calibration is going on. However, in the proposed method, the stolen/missing sample is "filled in" by a nonlinear interpolation method that is discussed in the following section. This pattern repeats intermittently rather than 50% of the time, and the calibration cycle will continue indefinitely, compensating for coefficient drifts due to supply and temperature variation.

To observe the skip-cycle in detail, refer to Fig. 1. There is no difference in switching between the calibration and the normal conversion cycles. For calibration, the bottom plates of the input capacitors are precharged to 0 instead of V_i, and in the following clock phase, the bottom plates are switched to the calibration voltage V_{cal-i}, which is either $V_{ref}/2$ or $-V_{ref}/2$. The output voltage now has an additional term such as $\pm V_{cal}(1+\alpha)$. When this propagates through the rest of the pipeline, the measured value is the ideal $\pm V_{cal}$ plus the error

term that can be separated by subtracting the ideal calibration voltage digitally.

Since this skip-cycle approach steals a cycle from the ordinary conversion process, an input sample is missing. That missing sample has to be compensated in the digital-domain. The nonlinear interpolation method to be described in the next section is able to "recover" this missing point for any band-limited signal up to two-thirds of the Nyquist bandwidth using a 44-point FIR (22 taps causal and 22 taps noncausal). Depending upon the size of the FIR, the accuracy and bandwidth limitation of the interpolation will vary. Because of the real-time operation in this skip-cycle approach, assuming that one can build digital multiplier (parallel type) and accumulator that would execute within one clock cycle, the FIR filter needed for the interpolation task would require overall delayed cycles of at least the amount of the taps.

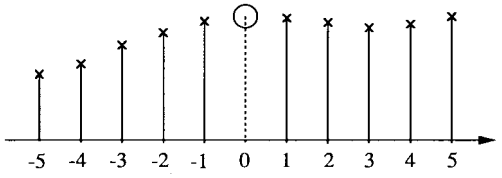
IV. Nonlinear Interpolation

As discussed in the preceding sections, a method of nonlinear interpolation is used in order to "fill" the missing sample in the skip-cycle method. The interpolation accuracy depends on the number of taps used and the frequency of the signal that it is dealing with. The interpolation method and simulation results will be presented in this section. Shown in Fig. 6 is a summary of the nonlinear interpolation condition and result for a ninth-order (10 points) polynomial example. Simulation results have verified that an equal number of taps before and after the missing datum display the best accuracy for a given total number of taps (fixed order polynomial). In the figure, the "n" stands for the number of taps on each side of the missing point. Therefore, in the example shown, $n = 5$.

The linear equations regarding the maximum-order polynomial that will fit perfectly with all crossing points are shown below in the matrix representation. The perfect fit for all crossing points is based on the $(2n-1)$th polynomial

$$a_0 + a_1 k + a_2 k^2 + a_3 k^3 + \ldots + a_{2n-2} k^{2n-2} + a_{2n-1} k^{2n-1} = x(k) \tag{5}$$

where $x(k)$ represents the data points. The unknown value is $x(0)$, which will be interpolated by using the coefficients calculated from the matrix. In this setup, $x(0)$ is conveniently the first coefficient of the polynomial a_0 since the $k = 0$ condition



$$x(0) = \sum_{k=-1}^{-n} x(k)\,C(k) + \sum_{k=1}^{n} x(k)\,C(k)$$

$$C(k) = \frac{n!\,n!}{(n+k)!\,(n-k)!}(-1)^{k+1}$$

Fig. 6. Interpolation example for $n = 5$ (ninth-order polynomial).

nullifies the effect of the rest of the polynomial coefficients. Solving for the polynomial coefficient a_0, equivalent to the missing point $x(0)$, many different values of "n" follows an interesting trend that is very similar to what is often referred to as Pascal's triangle, which is

$$\begin{array}{ccccccccccccccccccc}
 & & & & & & & & 1 & & & & & & & & & & \\
 & & & & & & & 1 & & 1 & & & & & & & & & \\
 & & & & & & 1 & & 2 & & 1 & & & & & & & & \\
 & & & & & 1 & & 3 & & 3 & & 1 & & & & & & & \\
 & & & & 1 & & 4 & & 6 & & 4 & & 1 & & & & & & \\
 & & & 1 & & 5 & & 10 & & 10 & & 5 & & 1 & & & & & \\
 & & 1 & & 6 & & 15 & & 20 & & 15 & & 6 & & 1 & & & & \\
 & . & & . & & . & & . & & . & & . & & . & & . & & . & \\
\end{array}$$

Taking the rows with the odd number of terms (largest term in the center) and normalizing the coefficients with the largest term and by placing an alternating sign, we have the equation shown at the bottom of the next page. And this is the exact pattern the interpolating coefficients follow for the calculation of $x(0)$ (or a_0), except for the "1" in the center which cannot apply (remember the sample in the center is missing). In summary, as already shown in Fig. 6, the interpolating coefficients follow a simplified equation

$$C(k) = \frac{n!n!}{(n+k)!(n-k)!}(-1)^{k+1} \tag{6}$$

$$\begin{bmatrix}
1 & -n & -n^2 & . & . & -n^{2n-1} \\
1 & -n+1 & (-n+1)^2 & . & . & (-n+1)^{2n-1} \\
. & . & . & . & . & . \\
. & . & . & . & . & . \\
1 & -2 & -2^2 & . & . & -2^{2n-1} \\
1 & -1 & -1^2 & . & . & -1^{2n-1} \\
1 & 1 & 1 & . & . & 1 \\
1 & 2 & 2^2 & . & . & 2^{2n-1} \\
. & . & . & . & . & . \\
. & . & . & . & . & . \\
1 & n-1 & (n-1)^2 & . & . & (n-1)^{2n-1} \\
1 & n & n^2 & . & . & n^{2n-1}
\end{bmatrix}
\begin{bmatrix}
a_0 \\ a_1 \\ a_2 \\ a_3 \\ . \\ . \\ . \\ . \\ . \\ . \\ a_{2n-2} \\ a_{2n-1}
\end{bmatrix}
=
\begin{bmatrix}
x(-n) \\ x(-n+1) \\ . \\ . \\ x(-2) \\ x(-1) \\ x(1) \\ x(2) \\ . \\ . \\ x(n-1) \\ x(n)
\end{bmatrix}.$$

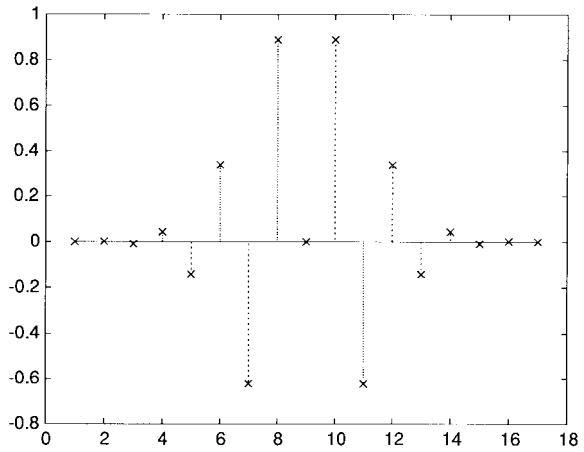


Fig. 7. 16-tap coefficients for interpolation.

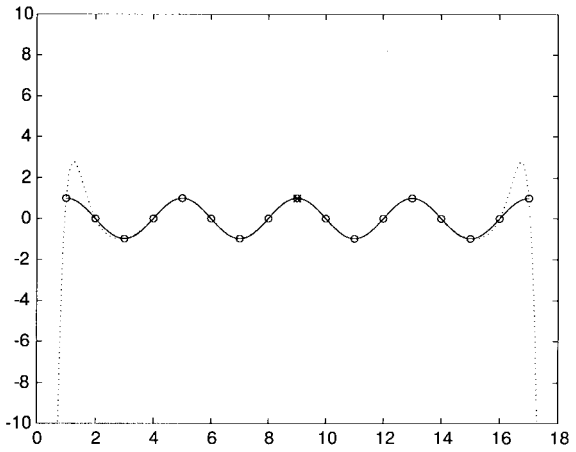


Fig. 8. Example of a successful interpolation in the middle for n =8 (16 taps).

for $k = \pm 1, \pm 2, \ldots, \pm n$. Using these coefficients, the interpolated value is simply calculated as

$$x(0) = \sum_{k=-1}^{-n} x(k)C(k) + \sum_{k=1}^{n} x(k)C(k). \tag{7}$$

In order to provide some visual presentation of the nonlinear interpolation, we can first see the decaying trend of the coefficients for the 16-tap ($n = 8$) example shown in Fig. 7. Using these coefficients, the plot in Fig. 8 shows how the polynomial, perfectly fitting all 16 crossing points successfully, interpolates for the missing point in the middle. In this example, the signal is a quarter of the sampling frequency-one half of the Nyquist bandwidth. Fig. 9 shows the extreme condition where the interpolation method is unable to produce the missing sample. The example is simulated for one of the worst cases where the input signal is at the Nyquist sampling condition, for the case where n =4.

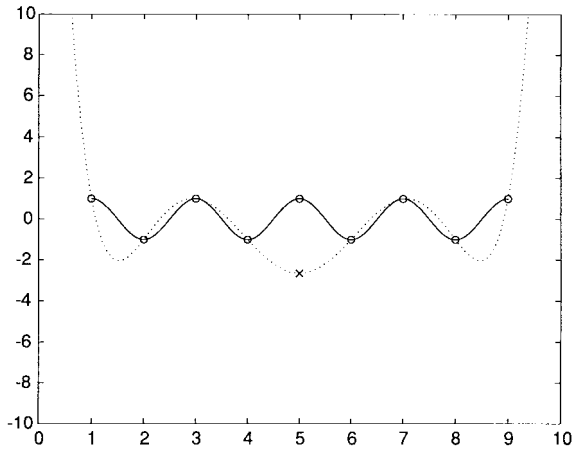


Fig. 9. Example of a failed interpolation in the middle for n =4 (8 taps).

A global view of the nonlinear interpolation trends and limitations is shown in Fig. 10. The x-axis represent the order of the polynomial N, which is equivalent to $2n - 1$, and the y-axis is the frequency of the normalized ± 1 full-swing sinusoidal input signal. The z-axis simply represents the magnitude of the interpolation error. The error magnitude is measured at the worst case condition where the phase of the missing sample in the sinusoidal input signal is $\pi/2$ or $3\pi/2$. This is where the second derivative of the sinusoid is at its maximum.

Further exploring a higher-order polynomial, the 99th-order ($n = 50$) condition can easily display a 16-b accurate range to about two-thirds of the Nyquist bandwidth. Since the 99th-order is too high, a more realistic and implementable conditions are simulated. For the set of ideal coefficients given for $n = 46$, it was first truncated by a finite window size equivalent to $n = 22$, preserving the coefficients that is quantizable at the 17-b level. A 2-b improved resolution of 19 b is used as the coefficients for the calculation process, and the multiply/accumulate block was simulated for 21-b accuracy. The result of this setup for the interpolation applied to a 16-b accurate input signal is shown in Fig. 11. To see the effects of phase where the missing point occurs on the interpolation accuracy, the figure displays the error contour in log scale.

$$\begin{array}{ccccccccccccc}
 & & & & & & 1 & & & & & & \\
 & & & & & \cdot & & \cdot & & & & & \\
 & & & & 1/2 & & 1 & & 1/2 & & & & \\
 & & & \cdot & & \cdot & & \cdot & & \cdot & & & \\
 & & -1/6 & & 4/6 & & 1 & & 4/6 & & -1/6 & & \\
 & \cdot & & \cdot & & \cdot & & \cdot & & \cdot & & \cdot & \\
1/20 & & -6/20 & & 15/20 & & 1 & & 15/20 & & -6/20 & & 1/20 \\
\cdot & & \cdot & & \cdot & & \cdot & & \cdot & & \cdot & & \cdot
\end{array}$$

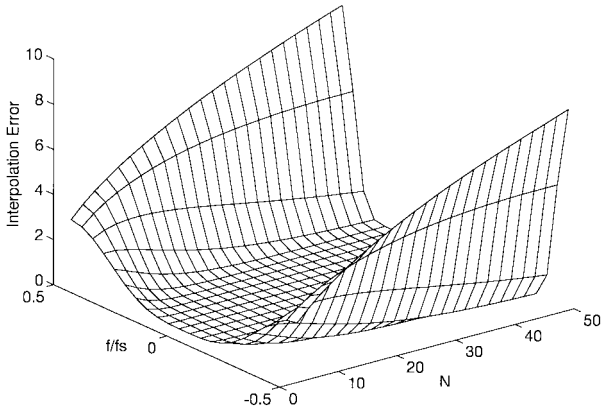


Fig. 10. Interpolation error versus input frequency and N.

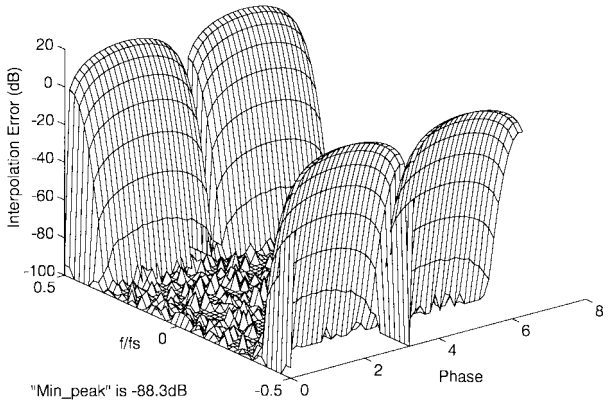


Fig. 11. Interpolation error using truncated coefficients (from n =46 to n =22).

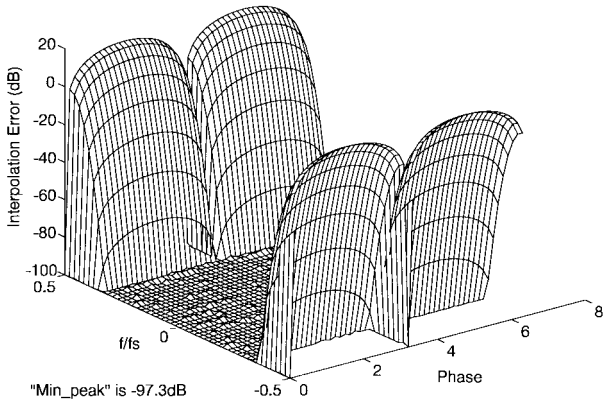


Fig. 12. Averaged interpolation error (99 samples).

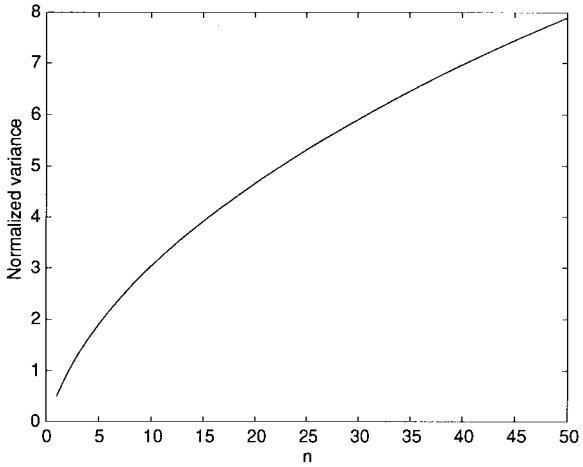


Fig. 13. Uncertainty of the interpolated value.

The resolution has been limited (clipped) at −100 dB level for this figure. The 16-b accuracy of the input signal in the simulation is performed by adding a 16-b level uncertainty (uniform distribution) to an ideal input signal. As noted in the figure the worst case measure in the noise-floor of the contour, referred to as the "min-peak," is −88.3 dB. The fact that this min-peak value is not as low as the 16-b level (≈ −96 dB) is due to the extra uncertainty added to the interpolated ("filled") value. The analysis in the following section will show that this is a function of the order of the interpolating polynomial (i.e., function of "n"). Despite this fact, when the errors from the interpolation are averaged, as shown in Fig. 12 for the 99 samples, the noise-floor is much flatter and the min-peak value is lowered to −97.3 dB in this case. These plots, Figs. 11 and 12, display the flat region (noise-floor) extending to two-thirds of the Nyquist bandwidth.

V. Quantization Effects on Interpolation

If the input data samples, on which the nonlinear interpolation is applied, were ideal (infinite resolution), the interpolation would not suffer from any additional drawbacks. However, because of the nature of the quantized (digitized) data, the interpolated value (the missing point) calculated from a weighted sum of the digitized data will end up with an increased uncertainty (variance).

The analysis is straightforward. First we realize that the digitized data samples represent a set of independent uniformly distributed random variables with variance σ_i^2. As an example, for an n-bit word,

$$\sigma_i^2 = \frac{\Delta^2}{12}, \quad \text{where } \Delta = (\text{Full Range})\, 2^{-n}. \tag{8}$$

When the missing point is calculated using (7), the uncertainties (variances) associated with the data $x(1), x(-1), x(2), x(-2), \ \ldots, x(n), x(-n)$ are summed up according to the weight of the coefficients $C(k)$. With the variance σ_i^2 referring to the sample point $x(i)$ the interpolated value $x(0)$ would have a sum variance as follows:

$$\sigma_0^2 = \sum_{i=-1}^{-n} \sigma_i^2 C(i)^2 + \sum_{i=1}^{n} \sigma_i^2 C(i)^2. \tag{9}$$

From the expression given in the above, we would naturally expect an increasing variance of the interpolated value, σ_0^2, as the order of the nonlinear interpolation increases. Fig. 13 shows the plot showing the overall trend of this normalized variance. For the truncated (or windowed) coefficients used for the simulation result shown in Figs. 11 and 12 ($n = 46$ reduced to $n = 22$), the variance of the interpolated value sees an increase of 7.5, which translates to nearly a 1.5-b reduction.

VI. Conclusions

A background calibration technique is developed to digitally self-calibrate pipelined ADC's in real time. The proposed skip and fill algorithm as well as the split-reference injection technique are adapted specially for 1-b pipelined ADC's that use capacitor-ratioed MDAC's. The skip-cycle approach allows for real-time background calibration by filling the skipped sample before the digital values are delivered. The accuracy of this background calibration will be identical to that of general foreground calibration schemes. The nonlinear interpolation technique that would be used in the background calibration method has been derived for an arbitrary $(2n-1)$th-order polynomial. An exemplary reference of $n = 46$ truncated to $n = 22$ yields two-thirds of the Nyquist bandwidth to have low interpolation noise-floor that is adequate for 16-b accuracy.

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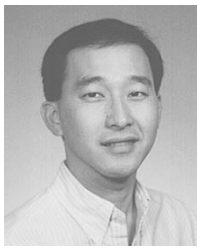

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