Adaptive Digital Correction of Analog Errors in MASH ADC's—Part II: Correction Using Test-Signal Injection

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***Abstract*—The first part of this two-part paper, published separately, discusses the quantization noise leakage problem caused in cascaded delta–sigma (MASH) analog-to-digital converters (ADC's) by the imperfections of the first-stage analog circuitry. It also proposes adaptive digital techniques based on detecting and minimizing the leakage noise in the output signal. In some cases, this is difficult to accomplish, since the noise is correlated with the input signal, and since the adaptation relies on acquiring the unknown out-of-band noise signal. The second part of the paper, given below, describes a different adaptation strategy. It relies on the injection of a pseudorandom two-level test signal at the input of the first-stage quantizer, where it is added to the quantization noise. The test signal then leaks into the output signal, where it can be detected and used to control the digital noise-cancellation filter. This paper describes the correction process, as well as some efficient structures for implementing it, and demonstrates the effectiveness of the technique by describing three design examples.**

***Index Terms*—ADC, delta sigma, digital correction, MASH, on-line adaptive compensation, sigma delta, test signal.**

I. Introduction

CASCADED delta–sigma (MASH) data converters offer a good compromise between high accuracy, robust stability, and speed. However, they are very sensitive to analog circuit imperfections because they rely on the *accurate* matching of the transfer functions of two internal signal paths, one predominantly analog and the other predominantly digital [1]. The actual mismatch can be reduced in the analog domain by careful analog circuit design [2]–[4] or by the use of multibit first stage [5], but only to a limited degree, especially if low-cost fabrication must be used. On the other hand, several digital-domain solutions have been developed including off-line calibration [6] and on-line correction [7], [8].

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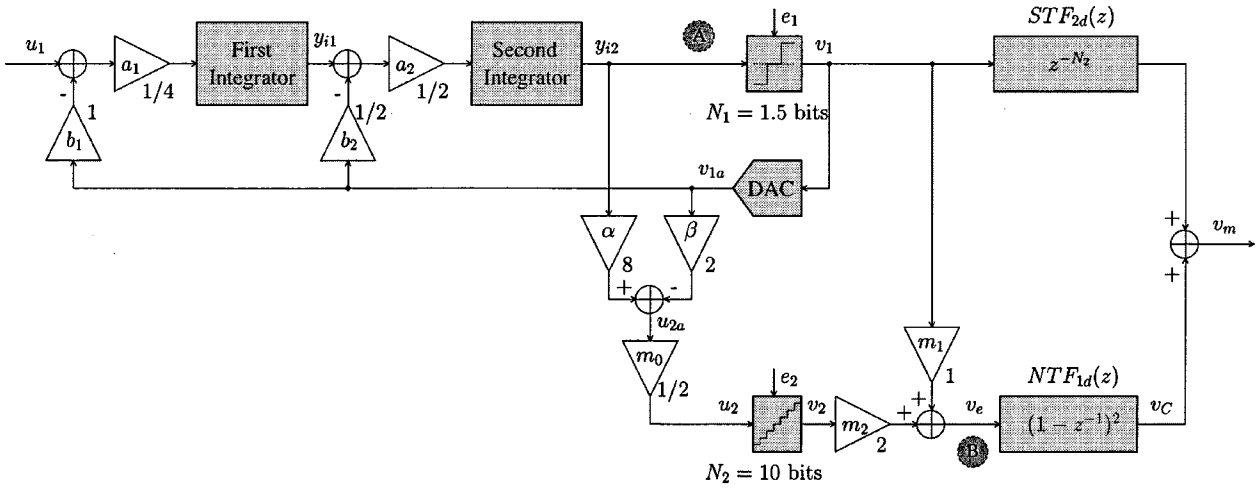
We proposed earlier an adaptive on-line digital error correction technique based on injecting a test-signal reference before the first-stage quantizer [9], [10]. It was shown that low hardware complexity and robust adaptation can be achieved using this technique. An experimental 2-0 MASH CMOS analog-to-digital converter (ADC) was also successfully fabricated and tested [11], [12]. This demonstrated that the 3-bit improvement in signal-to-noise-and-distortion ratio (SNDR) predicted by previous simulations [9] is in fact achievable in IC implementation. By using on-line correction, the effects of temperature variations, changes in process parameters, as well as of aging and drift were eliminated.

In this paper, the basic theory of this approach and the related design considerations will be presented in Section II. In the following section, the design of three adaptive 2-0 MASH ADC's is described to illustrate the application of the principle of adaptive error correction. First, a simple but functional prototype [11], [12] is described (Section III-A). The next two design examples deal with recently developed improvements to this technique, and with its application in a very fast (sampling frequency f_S =100 MHz, oversampling ratio OSR $= 4 \sim 8$, signal bandwidth $f_B = 6 \sim 12$ MHz), and high-accuracy (signal-to-noise ratio SNR $= 13 \sim 16$-bit) ADC implementation [13]. Significant improvements over the earlier results were achieved by using a 1.5-bit quantizer (Section III-B) or a 5-bit one (Section III-C) in the first stage instead of a simple comparator (Section III-A), and also by redesigning the MASH ADC structure by adding a differentiator to the adaptation filter and choosing the adaptation parameters differently. Measurement results are also described (Section III-A). Finally, a summary of the results achieved is given in Section IV.

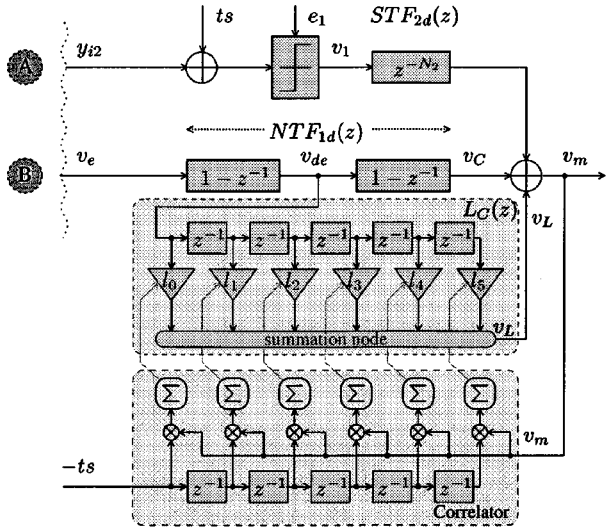
II. Adaptive Correction Using Test Signal Injection

As shown in Part I [1], the key analog imperfections of the MASH ADC are the pole and gain errors of the first-stage integrators. Detailed analysis of the effects of these linear errors [10], [12] indicates that they introduce a parasitic leakage path for the first-stage quantization noise e_1 to the output v_m [Fig. 1(a)], so that the output voltage in the z-domain is given by

$$V_{m_{\rm real}}(z) = V_{m_{\rm ideal}}(z) + H_{\rm leakage}(z)\, E_1(z). \qquad (1)$$



(a)



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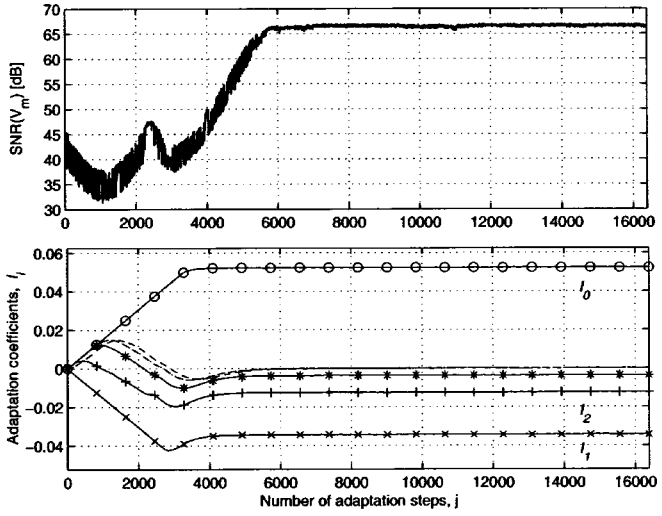

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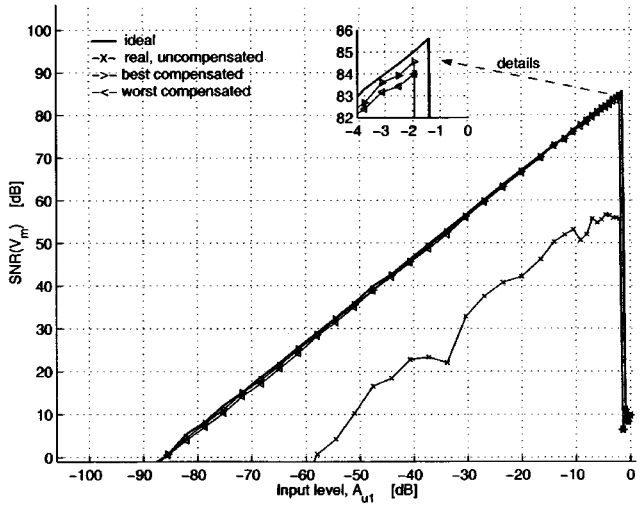

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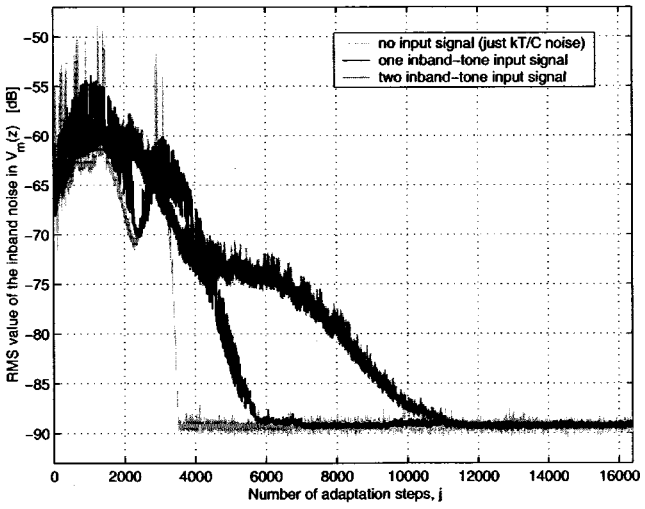


(e)

Fig. 1. Improved adaptive 2-0 MASH ADC. (a) Improved structure. (b) Improved adaptive digital noise-leakage compensation scheme. (c) Convergence curves for an adaptive error-correction process for an inband-tone input of amplitude $A_{u1} = 10\%$ of full scale. Top: corrected SNR *versus* adaptation number. Bottom: curves from top are l_0, l_5, l_4, l_3, l_2, and l_1 *versus* adaptation step number. (d) Simulated SNR performance after correction. (e) Convergence curves for various inband input signals with amplitudes $A_{u1} = 10\%$ of full scale. Imperfections considered for (c)–(e): $\Delta_C = 0.8\%$, $A_{\rm dc} = 54$ dB, and $N(kT/C) = -92$ dB; OSR $= 8$.

Assuming small relative errors, the transfer function $H_{\text{leakage}}(z)$ of this noise leakage can be approximated accurately with a finite Taylor series expansion

$$\begin{aligned} H_{\text{leakage}}(z) &= \left.\frac{V_{m_{\text{real}}}(z)}{E_1(z)}\right|_{\substack{U_1(z)=0\\E_2(z)=0}} \\ &= A_0 + A_1(1-z^{-1}) + A_2(1-z^{-1})^2 \\ &\quad + \cdots + A_{M-1}(1-z^{-1})^{M-1} \end{aligned} \tag{2}$$

where the coefficients $A_0 \cdots A_{M-1}$ are functions of the dc op-amp gain A_{dc} and of the relative capacitor errors $\Delta_C = (\Delta C_2/C_2) - (\Delta C_1/C_1)$ of the integrators. The filtering effect of the $(1-z^{-1})^i$ factors depends on the oversampling ratio (OSR). To estimate the order of magnitude of the noise leakage, the first five coefficients $A_0 \cdots A_4$ were calculated for the 2-0 MASH ADC presented in Fig. 1(a) [10], which will be analyzed in more detail in Section III-B, giving

$$\begin{aligned} A_0 &= \frac{a_1 a_2}{A_{\text{dc}}^2} \\ A_1 &= \frac{a_1 + a_2}{A_{\text{dc}}} \\ A_2 &= 4\Delta_C + \frac{-2a_1 + b_1 + \alpha + 4}{A_{\text{dc}}} \\ A_3 &= -2\Delta_C + \frac{a_1 - a_2 - 2b_1 + 2b_2 - 2}{A_{\text{dc}}} \\ A_4 &= \left(\frac{\beta}{a_1 a_2 \alpha} - 2\right)\Delta_C \\ &\quad + \left(b_1 - 2b_2 + \alpha + \frac{\beta(1+\beta)}{a_1 a_2 \alpha} - 2\right)\frac{1}{A_{\text{dc}}}. \end{aligned} \tag{3}$$

The parameters a_i, b_i, α, and β are defined in Fig. 1(a). Assuming $A_{\text{dc}} = 54$ dB and $\Delta_C = 0.8\%$, the order of magnitude of A_0 is 10^{-6} and of $A_1 \cdots A_4$ is 10^{-3} to 10^{-2}. It can be observed from (3) that the first two terms (A_0 and A_1) depend only on the finite dc op-amp gain A_{dc}, and that A_0 is usually negligibly small. Note that an accurate *a priori* estimation of $A_0 \cdots A_{M-1}$ is not possible, because of the random nature of the variables A_{dc} and Δ_C. However, an accurate evaluation is necessary, because of the high sensitivity of the SNR performance to these values. In our approach, we have hence adopted an *adaptive* estimation of the errors introduced by these analog circuit imperfections [9]. This is explained below.

In the expression (2) for the noise-leakage transfer function $H_{\text{leakage}}(z)$, the output errors introduced by the terms $A_i(1-z^{-1})^i$ decrease rapidly with the order i of the term. This shows that the effect of the analog imperfections can be suppressed by incorporating in the structure a simple low-order digital correction path for the quantization error which cancels the leakage signal. This correction can be provided by an adaptive digital finite-impulse response (FIR) filter $L_C(z)$ (Fig. 2) which adds a digital correction term v_L to the output v_m of the MASH [9]. Therefore, the digital correction signal v_L should be a negative estimate of the noise leakage.

Since the main component of v_e in Fig. 1(a) is the negative first-stage quantization noise $(-e_1)$ converted by the second stage, its z-transform is given by

$$V_e(z) = -E_1(z) + m_2 E_2(z) \cong -E_1(z) \tag{4}$$

and hence, the digital correction signal v_L in Fig. 2 is given by

$$\begin{aligned} V_L(z) &= V_e(z) L_C(z) \\ &\cong -E_1(z)\left(l_0 + l_1 z^{-1} + l_2 z^{-2} + \cdots + l_{M-1} z^{-(M-1)}\right) \end{aligned} \tag{5}$$

where $L_C(z)$ has M coefficients l_i forming the vector $\boldsymbol{l} = [l_0, l_1, \cdots l_{M-1}]^T$. Equations (1), (2), and (5) indicate that v_L can be a negative estimate of the noise leakage if the coefficient vector $\boldsymbol{l}$ of the FIR filter $L_C(z)$ is properly chosen. Since the exact values of the analog imperfections are *a priori* unknown, the parameters of the digital correction filter $L_C(z)$ must be adaptively controlled.

A. Test-Signal Based Adaptation

For adaptively adjusting on-line the coefficient vector $\boldsymbol{l}$, a test signal ts is entered into the modulator at its least sensitive node, i.e., before the first-stage quantizer, and it is detected and adaptively cancelled in the output signal v_m [Fig. 2(b)]. The test signal ts is a pseudorandom two-level zero-mean white noise, so it is uncorrelated with the input signal u_1 and with the quantization noises e_1 and e_2. The test signal ts is added to the quantization noise e_1, and it behaves similarly to the quantization noise. Since the test signal ts follows the same parasitic leakage path toward the output v_m as the quantization noise e_1, removing the test signal ts from the output v_m requires the same operation as removing the remainder of the quantization noise e_1 from v_m. In other words, the minimization of the test signal ts in the output v_m is equivalent to the minimization of the noise leakage.

Even though the test signal ts has statistical properties similar to those of band-limited white noise, it is deterministic and fully known. Therefore, it can be detected in the output v_m by using a correlation process between the output v_m and the digital replica of ts [Fig. 2(b)] which generates an error signal. This error signal is then used to update the coefficient vector $\boldsymbol{l}$ by a gradient method such as the block least-mean-square (BLMS) algorithm [14]. For simple hardware implementation, we chose the sign-sign version of the BLMS (SSBLMS) algorithm [10]. The update equation is given by

$$\begin{aligned} &\boldsymbol{l}[(j+1)K] \\ &\quad = \boldsymbol{l}[jK] - \gamma \cdot \text{sign}\left\{\sum_{k=0}^{K-1} v_m[jK-k]\,\text{sign}\{\boldsymbol{ts}[jK-k]\}\right\} \end{aligned} \tag{6}$$

where K is the block size, j is the current adaptation step, and γ is the adaptation coefficient. The M-element column vector

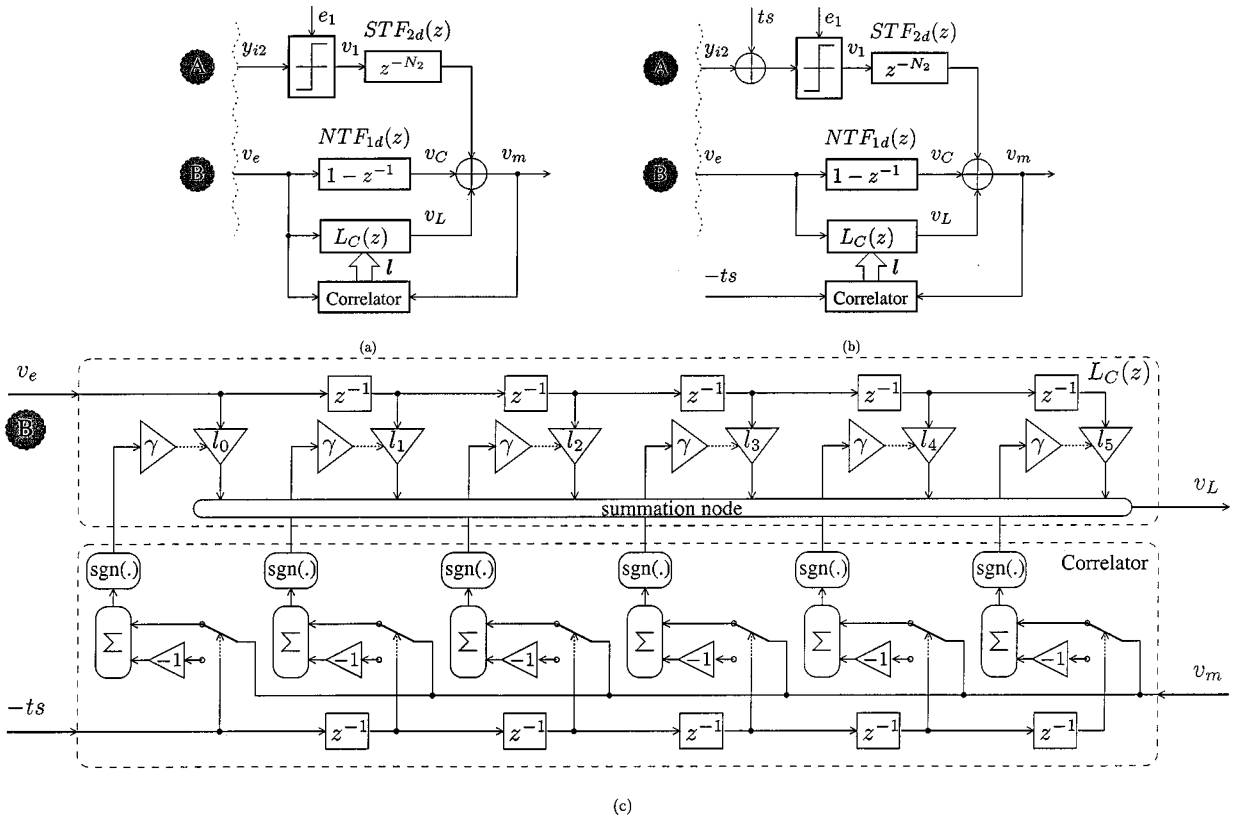


Fig. 2. Adaptive error correction scheme and its hardware implementation (a) without and (b) with test signal ts. (c) Hardware implementation of $L_C(z)$ using the SSBLMS algorithm for coefficient update.

$\boldsymbol{ts}[jK-k]$ contains the entries $ts[jK-k]$, $ts[jK-k-1]$, $\cdots$ $ts[jK-k-(M-1)]$. The detailed form of (6) is

$$\begin{aligned}
&l_0[(j+1)K] \\
&\quad = l_0[jK] - \gamma \\
&\qquad \cdot \operatorname{sign}\left\{\sum_{k=0}^{K-1} v_m[jK-k]\ \operatorname{sign}\{ts[jK-k]\}\right\} \\
&l_1[(j+1)K] \\
&\quad = l_1[jK] - \gamma \\
&\qquad \cdot \operatorname{sign}\left\{\sum_{k=0}^{K-1} v_m[jK-k]\ \operatorname{sign}\{ts[jK-k-1]\}\right\} \\
&\qquad \vdots \\
&l_{M-1}[(j+1)K] \\
&\quad = l_{M-1}[jK] - \gamma \\
&\qquad \cdot \operatorname{sign}\left\{\sum_{k=0}^{K-1} v_m[jK-k]\right. \\
&\qquad \left. \cdot \operatorname{sign}\{ts[jK-k-(M-1)]\}\right\}. \qquad (7)
\end{aligned}$$

Of course, the same adaptive scheme can be used without a test signal by replacing the test-signal power measurement with the first-stage quantization error e_1 measurement [Fig. 2(a)]. But the power of e_1 cannot be measured with the same accuracy, because e_1 is not known, and it is strongly correlated with the input signal u_1. Therefore, an adaptation process using the correlation between v_m and e_1 is input-signal dependent, and hence it is more suitable for *off-line* calibration. However, the test-signal approach described in this paper offers a robust *on-line* error correction strategy.

Since the test signal ts is uncorrelated with other components of the output signal v_m, such as u_1, e_1, and e_2, its power can be measured selectively. Simulations show that even if the test-signal power is much lower than the power of other components of the output signal v_m (say, 1% of the full-scale input signal power), its power can still be determined with high accuracy, and hence, the updating of the coefficient vector $\boldsymbol{l}$ can be done accurately. Note that the error correction using the test signal ts takes place on-line, in the background during the actual data conversion, so it can follow any drift introduced, e.g., by aging or temperature changes. Also, the test signal acts as a dither signal for the first stage of the MASH, thus improving its performance [15, Ch. 3].

A minor drawback of using test-signal injection is a slight loss ($\sim$1 dB) in the dynamic range (DR) due to the earlier overflow of the first-stage quantizer. Finally, note that the proposed test-signal approach is a *linear* correction method, so it can be used only for correcting linear errors, but not any harmonic distortion introduced by the analog circuits in the analog circuitry [6].

B. Adaptive Filter Implementation

To update the coefficient vector $\boldsymbol{l}$ of $L_C(z)$, the simple SSBLMS algorithm was selected, since it can be implemented using digital logic circuitry with finite precision, integrated on

the same chip with the MASH modulator. Therefore, high-speed multiplications in the correlator are replaced by summations, and the updating of the coefficients in $\boldsymbol{l}$ can be performed by simple additions or subtractions with a constant step size γ, as illustrated by (6). These are performed as up–down counting operations in the SSBLMS update, which are easy to implement especially if γ is chosen to be equal to the step size (1 LSB) of the coefficient vector $\boldsymbol{l}$. Then, every update requires only $K \cdot M$ additions. Since the updating is performed only once after each K samples, M additions per sample are required [10]. The resulting hardware implementation of the compensation filter $L_C(z)$ is presented in Fig. 2(c). The estimated die size of this adaptation digital logic is 0.57 mm^2 in a 0.25-μm standard CMOS process. It allows high-speed operation [12].

III. Design Examples

The adaptive error-correction technique using test-signal injection, described in the previous section, is generally applicable to any cascaded delta–sigma structure. In order to simplify the discussion, the application of this technique to the Leslie–Singh (2-0 MASH) [16] topology is considered in this paper. Three design examples involving 2-0 MASH ADC's with consecutively increasing structural complexity will be presented next.

The 2-0 MASH ADC contains as a first stage a second-order delta-sigma modulator with a N_1-bit quantizer, and as its second stage a multibit pipelined ADC with N_2 bits of resolution [Fig. 1(a)]. The transfer function of this structure with ideal analog circuits is given by

$$V_{m_{\text{ideal}}}(z) = z^{-2}\, z^{-N_2}\, U_1(z) + m_2\,(1 - z^{-1})^2\, E_2(z) \quad (8)$$

where z^{-2} describes the delay of the two switched-capacitor integrators in the first stage, and z^{-N_2} the latency of the second stage, assuming single-bit stages in the pipelined ADC. Note that ideally, the first-stage quantization noise e_1 is completely cancelled in $v_{m_{\text{ideal}}}$ as expressed in (8), because the digital filter's transfer function $NTF_{1d}(z)$ matches *perfectly* the first-stage noise transfer function $NTF_1(z) = (1 - z^{-1})^2$.

A. 2-0 MASH ADC with 1-bit First-Stage Quantization

In this first design, the simplest 2-0 MASH ADC was considered, which was then successfully fabricated and tested [11], [12] in order to get a working prototype for the adaptive error-correction scheme, and to verify the simulation results [9]. The first-stage modulator was chosen to be a second-order single-bit ($N_1 = 1$ bit) delta–sigma modulator, followed by an external multibit ($N_2 = 12$ bit) pipelined ADC [Fig. 3(a)]. The interstage coupling (α, β, m_0, m_1 and m_2 of Fig. 1(a)) was designed to allow the lowest possible analog hardware complexity, which eliminates the analog subtraction block ($\alpha = 1, \beta = 0$). This simple interstage coupling circuit results in a loss of approximately 6 dB in the DR of the modulator compared to the general coupling path presented in Fig. 1(a). However, this degradation was considered acceptable, because the main purpose of this design was to show the effectiveness of the adaptive noise-leakage compensation rather than producing an ADC optimized for DR.

The second-order first stage incorporating the test-signal path was fabricated in the Orbit 1.2-μm double-poly CMOS process [11]. The die photo is shown in Fig. 3(b). The MASH operated at a $f_S = 1$-MHz sampling rate and OSR $= 4$. The second stage was realized by an AD9220 chip. The digital outputs of the two chips were collected by a data-acquisition board and post-processed in a PC. Fig. 3(c) shows the measured output spectra with and without compensation for a sinewave input. The input signal frequency was 1.5 kHz, and the full-scale differential input voltage was 5 V$_{pp}$. Using compensation, the SNDR [Fig. 3(d)] was improved by 16–18 dB over the linear input signal range, which verified the effectiveness of the compensation.

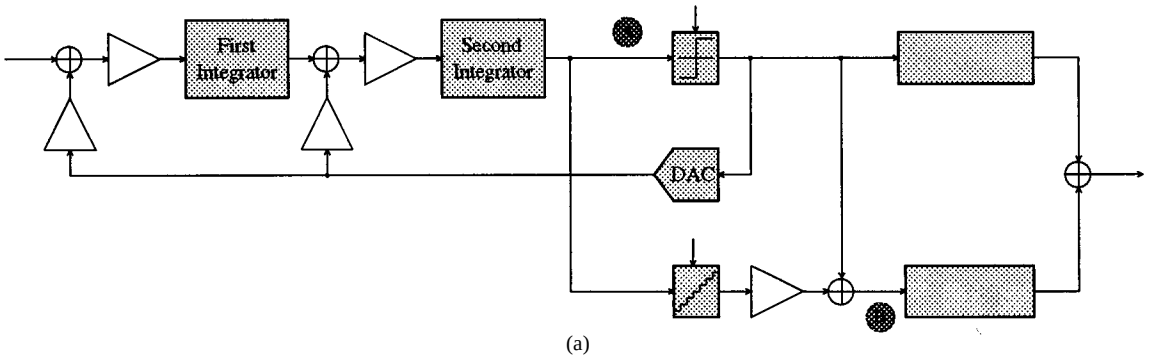
B. 2-0 MASH ADC with 1.5-bit First-Stage Quantization

Next, an improved 2-0 MASH ADC structure is presented [Fig. 1(a)]. There are several structural changes [13]. The multiplier $m_0 < 1$ was added to prevent the second stage from overloading. To compensate for this attenuation, the digital output v_2 must be scaled up by $m_2 = (1/m_0) > 1$, which amplifies the quantization noise e_2 of the second stage as indicated in (8), and reduces the SNR of the system. In this structure, by adjusting β and m_1, an optimal weighting of the input y_{i2} and the output v_{1a} of the first-stage quantizer in the second-stage input signal u_{2a} can be achieved. This results in the largest possible value for m_0 and, in turn, the least possible amplification of the quantization noise e_2 [15, Sec. 7.3.1].

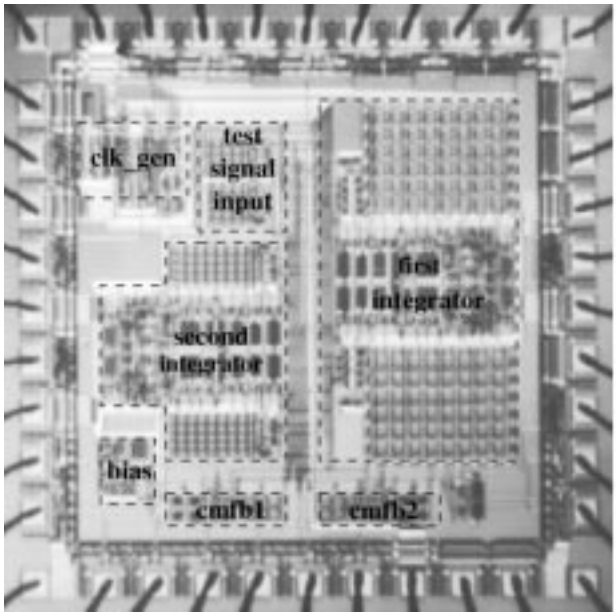
The usable input signal range u_1 was also increased by a modification in the first stage. Using a tri-level quantizer in the first stage instead of a simple comparator [17], the usable input signal range u_1 was extended by 6 dB [Fig. 1(d)]. The linearity of the tri-level feedback DAC is critical, but a highly accurate tri-level DAC was described in [18] which used extra switches and simple circuitry to insure linearity. This tri-level quantizer offers a good tradeoff between SNR performance and circuit complexity, especially if one wants to avoid a multibit mismatch-shaping DAC [15, Sec. 8.3.3] in order to reduce the chip area. The optimized parameters are also shown in Fig. 1(a).

Since we are aiming for a large-bandwidth and high-resolution ADC, a high sampling frequency ($f_S = 100$ MHz) was chosen combined with a low oversampling ratio (OSR $= 8$). For the second stage, a 10-bit pipelined ADC was chosen. Because the coefficient $\beta \neq 1$, a delayed version of the analog input signal u_1 is introduced into the second-stage input u_2. Therefore, the nonlinearities of the second stage may affect the linearity of the overall system. However, the harmonics of u_1 introduced by the pipelined ADC are attenuated by $NTF_{1d}(z)$, e.g., by 18 dB for OSR $= 8$, so a 13-bit linear performance is still easily achievable. Note that the linearity requirement for the second stage can be relaxed if $\beta = 1$ is chosen, and hence $u_{2a} = -e_1$ [Fig. 1(a)]. Therefore, the nonlinearity of the pipelined ADC will not introduce harmonic distortion of the input signal u_1, but only a colored pseudorandom error [19]. However, $\beta = 1$ changes the probability density function of u_{2a}, which causes an approximately 6-dB drop in the SNR compared to when $\beta = 2$. In conclusion, one should be aware of the THD *versus* SNR tradeoff described above.

With an input sampling capacitor $C_S = 6$ pF, the kT/C noise floor can be lowered to $N(kT/C) = -92$ dB (15 bits). The



(a)



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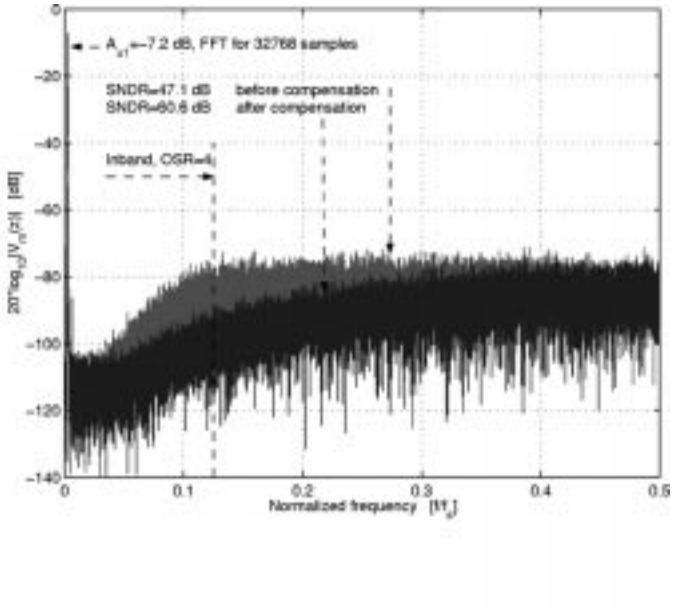

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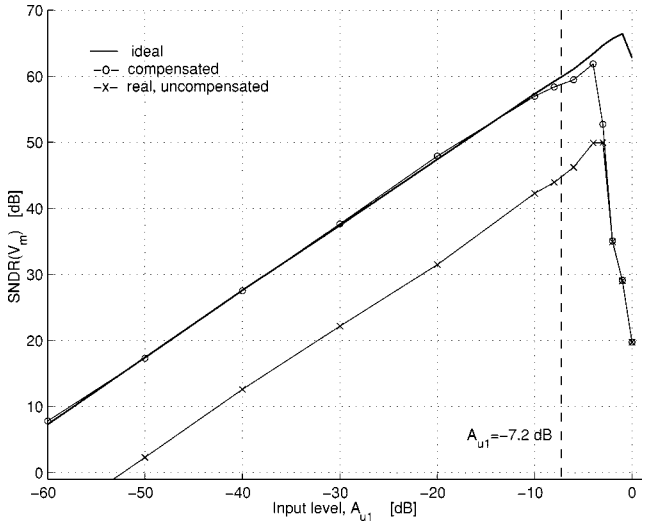


(d)

Fig. 3. Simple adaptive 2-0 MASH ADC (structure and performance). (a) Simple structure. (b) Die photo of the second-order delta–sigma modulator. (c) Measured output spectra and (d) measured SNDR of the prototype 2-0 MASH ADC, with and without correction.

resulting performance, assuming ideal analog circuitry, is presented in Fig. 1(d); a peak SNR of 86 dB was obtained for the optimized 2-0 MASH structure presented in Fig. 1(a). Due to the analog circuit imperfections, the SNR performance drops by more than 25 dB [Fig. 1(d)]. However, as shown next, using the adaptive error correction method the effects of the analog circuit imperfections can be effectively reduced, and a 13-bit 6-MHz bandwidth ADC becomes realizable.

1) Improved Error Cancellation: For the improved ADC, the properties of the noise leakage were studied in detail in order to determine the influence of the analog circuit imperfections on the performance of the cascaded ADC, and to build an effective compensator. Our study indicated that a modification of the previously used adaptive FIR filter [11] can improve the performance.

First, (3) shows that A_0 is negligible compared to the other terms. Therefore, (2) becomes

$$H_{\text{leakage}}(z) \cong (1-z^{-1})\ \left(A_1 + A_2(1-z^{-1}) + \cdots + A_{M-1}(1-z^{-1})^{M-2}\right) \quad (9)$$

and the input of $L_C(z)$ can be provided by v_{ed}, a differentiated version of v_e, as shown in Fig. 1(b). Hence, the effective order of the adaptive noise-leakage correction block (i.e., with input v_e and output v_L) has increased by 1. This simple operation does not even need additional hardware, because the differentiator can be provided by the first block of $NTF_{1d}(z)$. Furthermore, adding a differentiator at the front of $L_C(z)$ reduced the fluctuation of $\boldsymbol{l}$, which reduced the sample-by-sample ripple of the adaptation noise significantly, by 6 dB. Also, by choosing suitable parameters for the adaptation process (i.e., a block size of $K = 2^{16}$ and resolution of $N_{\boldsymbol{l}} = 16$ bits for the coefficient vector $\boldsymbol{l}$ of $L_C(z)$), the ripple of the adaptation noise was further reduced to the very comfortable value of 1 dB [13].

The evolution in time of the improved adaptive noise-leakage compensation process is presented in Fig. 1(c) for an inband sinewave input signal. The coefficients $l_0 \cdots l_5$ of the fifth-order FIR filter $L_C(z)$ were updated by the SSBLMS algorithm according to (6). After about 6000 adaptation steps, the adaptive process converged. The corrected SNR is close to its ideal value [Fig. 1(d)]. After convergence, the coefficient vector $\boldsymbol{l}$ still fluctuates slightly around its steady-state value, due to the inherent error of the SSBLMS update (i.e., the correlation process given in (6) is performed over a *finite* block length K, which leads to nonzero error terms in the gradient estimate; the resulting ripple of this fluctuation is approximately 0.0002, and is not visible on Fig. 1(c).) However, this fluctuation in $\boldsymbol{l}$ causes about a 1-dB adaptation noise in the corrected SNR [Fig. 1(c) and (d)]. Clearly, the performance of the compensated practical circuit approaches closely that of the ideal MASH ADC.

The adaptive correction process was verified by extensive simulations for various input signals with different inband frequencies and amplitudes. Fig. 1(e) shows the adaptation process for two-tone, one-tone, and zero input signals. The numbers of iterations required for convergence were different, but the converter behaved similarly in the steady state, maintaining its performance near that of the ideal MASH ADC.

2) Circuit-Level Design: To verify the performance of the improved adaptive 2-0 MASH ADC, a new chip is being designed in a 0.25-μm 3.3-V digital CMOS process. The circuit implementation offers some special challenges due to the targeted high-speed operation. In the first stage, all blocks are to be operated with a clock frequency $f_S = 100$ MHz. An existing 10-bit pipelined ADC core is used for the second stage. This ADC needs to be clocked at only 50 MHz, if the technique suggested in [20] is used.

C. 2-0 MASH ADC with 5-bit First-Stage Quantization

Finally, to improve further the accuracy of the 2-0 MASH ADC, while preserving its bandwidth, a multibit quantizer can be used in the second-order delta–sigma ADC [5], [21]. However, the linearity of the multibit DAC in the feedback path is critical, so it needs to be improved by using mismatch shaping [15, Sec. 8.3.3], which requires a large chip area and/or an analog calibration method [22], which provides a high linearity (18 bits) even for low oversampling ratios.

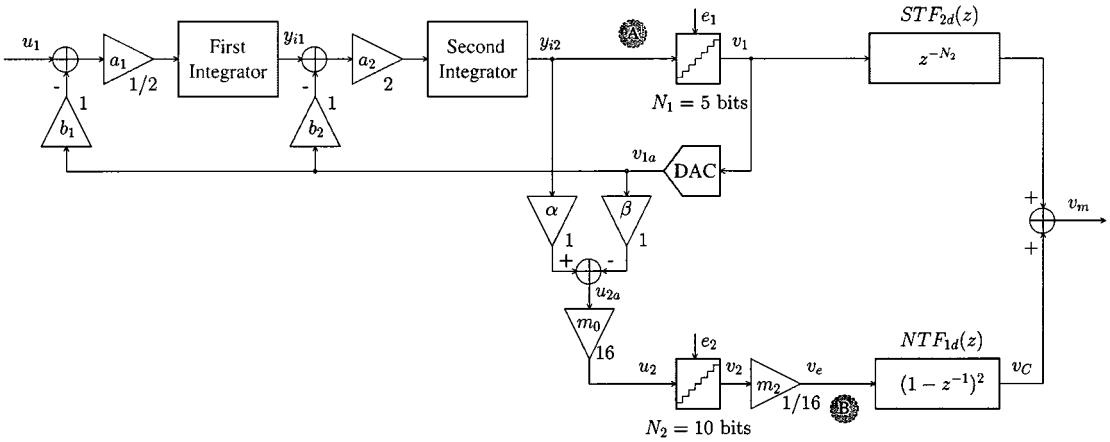
For a multibit first stage, the reduced quantization noise e_1 allows the scaling of the input of the second stage u_2 by using $m_0 > 1$ and $m_2 = (1/m_1) < 1$. This will reduce the power of e_2, and hence improve the SNR performance of the MASH, as expressed by (8). In addition, the multibit first stage leads to decreased sensitivity to analog circuit imperfections [5], because the noise leakage is proportional to the power of e_1, as indicated in (1). However, the mismatch between $NTF_1(z)$ and $NTF_{1d}(z)$ is still critical, especially when high sampling rates (e.g. $f_S = 100$ MHz) allow only modest dc op-amp gains ($A_{\text{dc}} = 40 \sim 50$ dB). Therefore, our adaptive on-line error correction technique is needed to cancel the negative effect of analog imperfections even for a multibit first stage.

An adaptively corrected 2-0 MASH architecture, similar to the one presented in Fig. 1(a), but with a multibit first stage ($N_1 = 5$ bit) and slightly different coefficients [23], was investigated at the behavioral level [Fig. 4(a)]. Extensive system-level simulation results (with ideal quantizers and DAC) indicated that by using a 5-bit quantizer in the first stage, and a lowered oversampling ratio of OSR $= 4$, it may achieve 16-bit accuracy with a 12-MHz signal bandwidth [Fig. 4(b)].

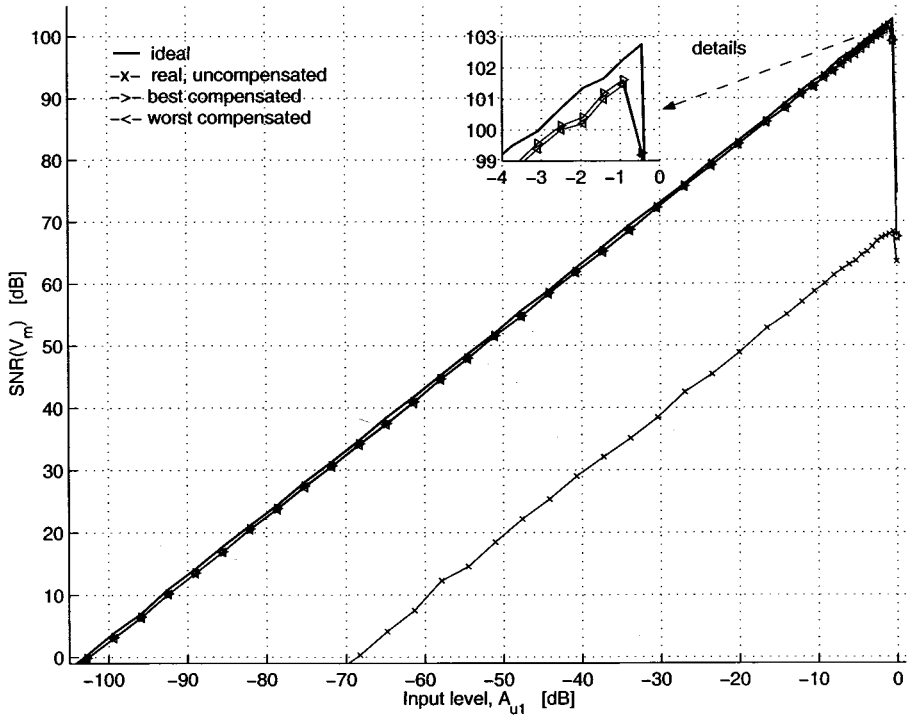
IV. Conclusion

In this part of the two-part paper, an adaptive correction technique based on the injection of a pseudorandom test signal was described for cascaded delta–sigma ADC's. It promises to be more robust and sensitive than earlier algorithms. The main results reported were the following.

1) An efficient approximating analysis was given for the estimation of the quantization noise leakage [(1)–(3)].
2) A digital structure, utilizing the correlation of the output signal with the test signal, was described for providing a compensation path in the noise canceling logic (Fig. 2).
3) A simple adaptive process, based on the sign-sign block LMS algorithm, was introduced for the control of the compensation path [(6) and (7)].
4) Three design examples were described to illustrate the use and effectiveness of the proposed correction techniques. The first (and simplest) of the corrected systems was implemented on a chip, and it successfully demonstrated the ability of the adaptive process to achieve nearly ideal SNDR performance even for low-accuracy analog circuits. The other two structures were improved versions of the first one, and simulations indicated that they can provide very fast and accurate ADC performance, surpassing the present state of the art for ADC's.



(a)



(b)

Fig. 4. High-performance 2-0 MASH ADC (structure and performance). (a) Structure and (b) simulated SNR performance. Imperfections considered: $A_{\rm dc} = 54$ dB, $\Delta_C = 0.4\%$, and $N((kT)/(C)) = -110$ dB; OSR $= 4$.

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