A Low-Voltage 10-Bit CMOS DAC in 0.01-mm^2 Die Area

Brandon Greenley, Raymond Veith, Dong-Young Chang, and Un-Ku Moon

***Abstract*—A low-voltage 10-bit digital-to-analog converter (DAC) for static/dc operation is fabricated in a standard 0.18-μm CMOS process. The DAC is optimized for large integrated circuit systems where possibly dozens of such DAC would be employed for the purpose of digitally controlled analog circuit calibration. The DAC occupies 110 μm$\times$ 94 μm die area. A segmented R-2R architecture is used for the DAC core in order to maximize matching accuracy for a minimal use of die area. A pseudocommon centroid layout is introduced to overcome the layout restrictions of conventional common centroid techniques. A linear current mirror is proposed in order to achieve linear output current with reduced voltage headroom. The measured differential nonlinearity by integral nonlinearity (DNL/INL) is better than 0.7/0.75 LSB and 0.8/2 LSB for 1.8-V and 1.4-V power supplies, respectively. The DAC remains monotonic ($|\mathrm{DNL}| < 1$ LSB) as INL reaches 4 LSB down to 1.3-V operation. The DAC consumes 2.2 mA of current at all supply voltage settings.**

***Index Terms*—Die area, digital–analog (D/A), digital-to-analog conversion (DAC), low voltage.**

I. Introduction

DIGITALLY controlled and area-efficient calibration circuits play an important role in the design of complex, multifunction mixed-signal application-specific integrated circuits (ASICs). Because these calibration circuits are commonly sprinkled throughout the chip to maximize flexibility and programmability, their impact on the total chip design should be minimal. One highly critical factor to consider when designing these calibration circuits is the area consumption. Especially in high-speed circuits, the die area of such calibration circuit is most critical in determining its usefulness. This is because the high-speed blocks need to be placed close together to minimize the effects of parasitics on the interconnects. The area occupied by the calibration circuit should be minimized so that the overhead circuitry/footprint does not interfere with the surrounding circuitry. The proposed area-efficient and accurate low-frequency (static/dc) digital-to-analog converter (DAC) is an effective calibration circuit for such applications.

In this brief, we will start by placing most technical emphasis in the discussion of architectural and transistor-level design considerations in Section II, followed by circuit implementation description in Section III and measurement results in Section IV.

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B. Greenley and R. Veith are with Tektronix, Beaverton, OR 97077 USA.

D.-Y. Chang is with Engim Inc., Acton, MA 01720 USA.

U. Moon is with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: moon@ece.orst.edu).

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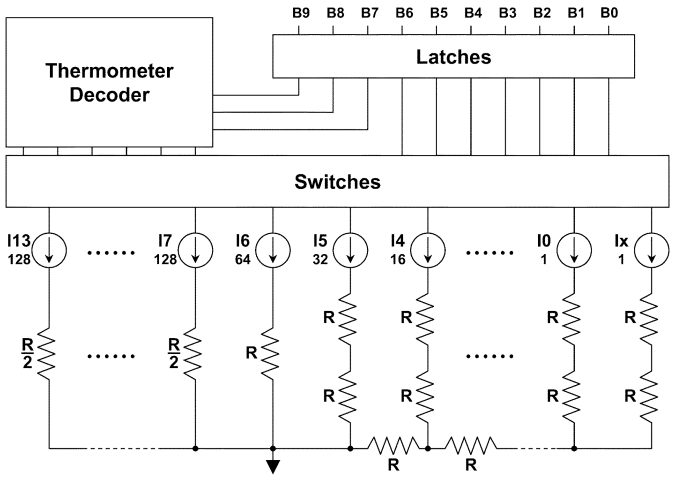

Fig. 1. The 10-bit segmented architecture.

II. Design Considerations

A. Architecture

A segmented R-2R ladder architecture implementation achieves the highest area efficiency in the design of the 10 b CMOS current-steering DAC for dc operation. Fig. 1 shows an overview of the segmented DAC architecture. The single-ended CMOS logic input digital word is received and latched before being passed on to the switches. The purpose of latching the input data is to allow the DAC to be used along a common programming bus. This programming bus may run throughout the chip and provide data to many calibration circuits along the way. This minimizes the routing overhead consumed by the calibration and control circuitry.

The three most significant bits (MSBs) are implemented using thermometer coding, while the lower 6 bits are implemented with a straight R-2R ladder. In between the thermometer portion (128 $\times$) and the R-2R portion (1 $\times$ to 32 $\times$), there exists a binary weighted branch (64 $\times$). A typical thermometer plus R-2R architecture [1] would include the 64 $\times$ branch in the R-2R ladder, hence placing two resistors in the 64 $\times$ branch and adding a resistor between the 32 $\times$ and 64 $\times$ branches. This typical approach would require one resistor per branch for the thermometer portion.

The proposed architecture has two resistors in parallel for each branch of the thermometer portion. This method is effective in eliminating linear process gradients by placing the MSB resistors in a common centroid scheme in the layout. The chosen architecture results in a good trade-off of static performance and area consumption. Table I summarizes the tradeoff between die area and performance/matching. The number of resistors, switches, and 2-input logic gates needed are summarized

TABLE I
TRADEOFF ANALYSIS: AREA VERSUS PERFORMANCE

Upper Bits	Element	Architecture		Performance
		R-2R	Chosen	
3	resistors	9	7	Good
	switches	6	8	
	gates	0	3	
4	resistors	12	15	Better
	switches	8	16	
	gates	0	8	
5	resistors	15	31	Best
	switches	10	32	
	gates	0	23	

for implementations requiring upper 3, 4, or 5 MSBs in a given architecture.

For the case when 4 upper bits are considered, the number of resistors required to implement these 4 MSB bits in a R-2R architecture is 12, while the chosen architecture (segmented R-2R) requires 15. This comparison confirms that the added circuitry is acceptable when considering the upper 4 bits for segmentation. The die area cost of the chosen architecture (in comparison to a straight R-2R) would be too high for 5 bits segmentation, and the performance improvement is not justified.

B. Device Sizing

Because the measured performance of a DAC is highly dependent on multiple process variations, it is essential to examine these effects during the design process. The effect of random mismatch errors on the required relative current source matching is commonly characterized with the use of Monte Carlo analysis [2] in a SPICE-equivalent simulator. Recent works have provided a more simplified closed form method of determining the constraint on current source matching for a given yield [3].

The relative variance of a unit current source is then used in conjunction with closed form equations [4], [5] to determine the current source device dimensions. As in the case of lengthy Monte Carlo simulations, an effective answer can only be obtained from these equations when reliable matching data is known for the process.

The effects of random mismatch errors and process gradients for the nMOS transistors and resistors were examined by mathematically modeling the DAC exactly as it appears in the layout. The random and gradient variations associated with the nMOS device were modeled with W/L and threshold voltage variations including the body effect. The random and gradient errors associated with the resistors were modeled as resistivity variations. At the time this DAC was designed and fabricated, no matching data was available to us for this 0.18-μm CMOS process. Thus, the random parameters for the mathematical model were estimated/extrapolated based on the matching statistics of older generation CMOS processes.

The resulting dimensions of the unity current source device (cascode nMOS transistor) are $W = 0.52$ μm and $L = 0.36$ μm, and the width of the poly resistors is $W = 1.06$ μm. Since the DAC operates primarily at dc, there is no need to give special attention to the input latches or decoding logic. The digital portion of the DAC was implemented with minimum device geometry.

Note that the consideration of the random parameters estimated/extrapolated based on the matching statistics of older generation CMOS processes is found to be quite accurate in producing the anticipated results.

C. Layout

Every current source shown in Fig. 1 is a parallel combination of the unity current source device (cascode nMOS transistor). These 1024 unity current source devices are laid out in a pseudo common centroid scheme to reduce the effects of thermal and process gradients. Fig. 2 shows the arrangement of the devices in the implemented layout. Traditional common centroid layouts [6] or double common centroid [3] layouts provide the greatest immunity from random and gradient errors, but at the expense of being difficult to wire and consuming larger amounts of die area.

The layout shown in Fig. 2 was studied extensively using a mathematical model that accounts for the individual location of each unit current source device and each unit resistor. Errors can be applied in a purely random fashion, or in any combination of horizontal and vertical gradients. This layout has proven to be a beneficial tradeoff of area and performance.

Four rows and columns of dummy devices are added to the current source array to create the same boundary conditions for the current source devices placed at the edges. Dummy devices are also added to both ends of the resistor string. The resistor string also acts as a pseudo common centroid string since the MSB resistors are spaced alternately on the ends of the R-2R string to counteract linear gradient errors while simplifying routing.

Using minimum sized devices and the lowest extremes of the layout design rules for the digital portion helps create maximum device density, which correlates directly to die area conservation. Minimizing the complexity of the digital portion of a DAC leads to a smaller area, and since the digital portion has no effect on the static performance, a considerable area trade-off between the digital and analog portions can take place in DACs for dc operation.

D. Linear Current Mirror

The applications where static DACs are used most commonly require a linear and especially monotonic output. As is the case with most low-voltage circuits, output voltage swing range becomes a key design challenge. The low-voltage power supply introduces many difficulties, particularly when attempting to produce a sufficiently linear output current.

The user desires the DAC to effectively act as an ideal, adjustable current source or sink. In order for the current source/sink to be effective, it should take up as little percentage of the power supply as possible. In order to achieve an output current that takes up minimum headroom, this DAC uses the linear current mirror stage shown in Fig. 3. The opamps shown

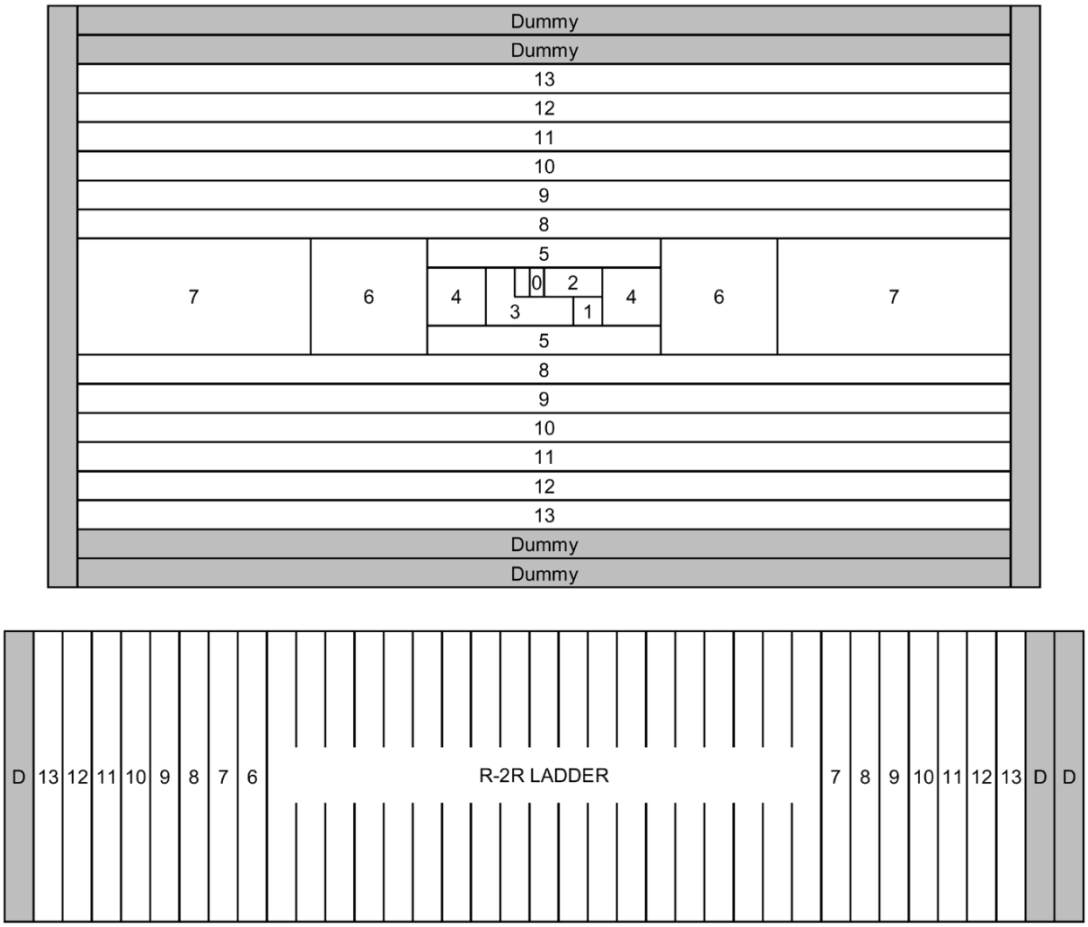

Fig. 2. Pseudocommon centroid layout.

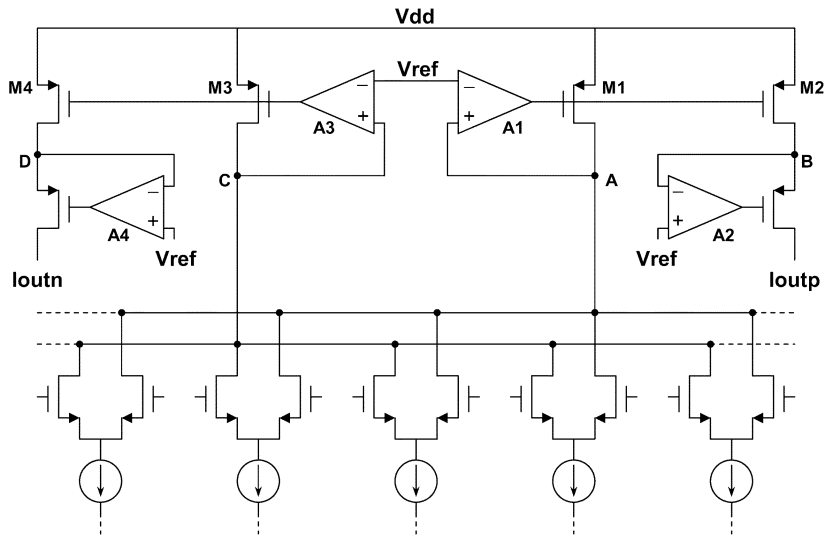

Fig. 3. Current output/mirror detail.

in Fig. 3 (A1–A4) are the critical blocks in the mirroring operation. Using opamps with high dc gain, nodes A-D are effectively held at $V_{\rm ref} \approx V_{dd} - 0.2$ V regardless of the current passing through devices M1–M4. Since the gates of M1 and M2 are tied together, and the drains are each servoed to the same voltage, the current produced in M1 will be replicated in M2. The code-dependent channel length modulation of the current cells inside the DAC core is also eliminated by the servoed opamps A1 and A3. Any opamp offsets contribute to the overall DAC gain (linear), but do not affect DAC linearity. The implemented two-stage opamp is shown in Fig. 4. The inverter-based design lends itself nicely when the headroom is limited. The straightforward approach gave us adequate gain, bandwidth, and most importantly small area consumption.

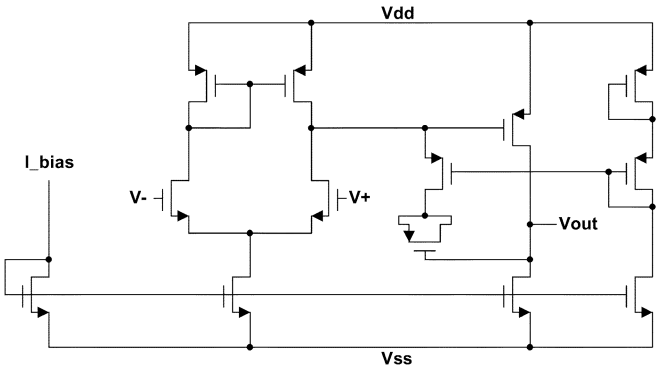

Fig. 4. Servo opamp.

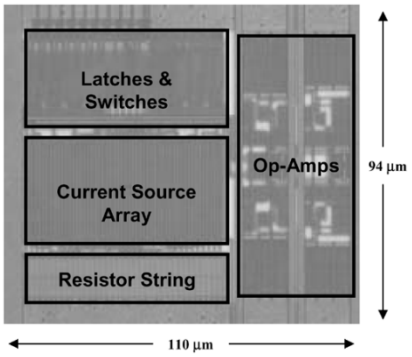

Fig. 5. Chip micrograph.

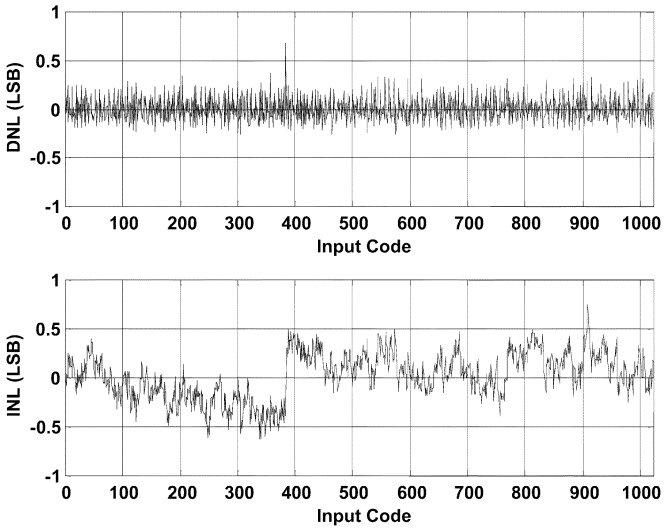

Fig. 6. Measured INL and DNL at 1.8-V supply.

III. Implementation

The prototype IC is realized in a standard 0.18-μm CMOS technology. Considerable efforts were given to the layout in order to minimize the total die area while maximizing the matching accuracy. Because of the dc operation of the DAC, there is no need for a separate power supply for the digital portion, thereby removing excess metal routing. Routing all the current source connections on top of the current source array also significantly reduced the die area. Although the DAC was realized in a five-metal layer process, the entire converter

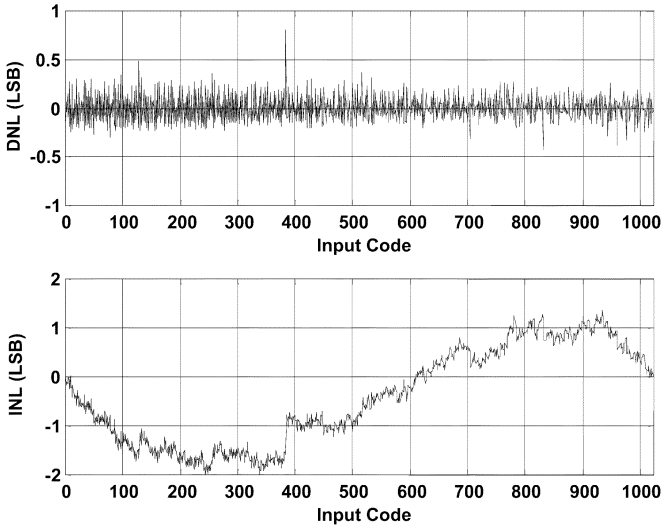

Fig. 7. Measured INL and DNL at 1.4-V supply.

was routed using only the first two metal layers. The circuitry surrounding the DAC can be organized such that the routing to/from the circuitry takes place on upper metal layers, allowing placement of the area-efficient DAC under the routing path. The entire die area of the DAC, including the opamps and power supply lines, is 110 μm$\times$ 94 μm), which is the size of a typical bond-pad. Shown in Fig. 5 is the die micrograph. The resistor string is shown in the lower left corner with the current source array directly above. Above the current sources is the digital portion, and the 4 opamps are shown on the right side of the micrograph. Power supplies surround the perimeter.

IV. Measured Results

Fig. 6 shows the measured integral nonlinearity (INL) and differential nonlinearity (DNL) when operating under a 1.8 V power supply. Fig. 7 shows the measured INL and DNL operating under a 1.4-V supply. The INL is better than 0.75 LSB for the 1.8-V case, and better than 2 LSB for the 1.4-V case. The DNL is better than 0.7 LSB for the 1.8-V case, and better than 0.8 LSB for the 1.4 V case. In both cases, the digital-to-analog converter (DAC) is fully 10-bit monotonic, which complies with the most critical requirement. The DAC remains monotonic ($|\text{DNL}| < 1$ LSB) and INL reaches 4 LSB at 1.3 V.

The symmetrical bending of the INL curve shown in Fig. 7 is due to the nonlinearity of the opamps operating with reduced headroom. Because of the reduced headroom and the opamp nonlinearity, the INL degrades sharply for less than 1.3-V supply. The entire DAC consumes 2.2 mA of current, independent of power-supply voltage.

V. Conclusion

In this brief, the circuit design and layout guidelines to implement a 1.4-V, 10-bit DAC cell were presented. The DAC cell was designed with die area conservation and 10-bit monotonicity as the primary goals. A fundamental tradeoff between overall DAC performance/matching and chip area has been examined and an optimal solution implemented. The DAC employs an accurate method for obtaining a linear output current from the cell.

Measured results show 10-bit monotonicity and linearity at 1.8 V. The presented DAC cell is ideal for applications where a small, low power, low frequency calibration DAC is needed for the plethora of trim adjustments in large mixed-signal ASICs.

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