LOW-VOLTAGE PIPELINED ADC USING OPAMP-RESET SWITCHING TECHNIQUE

Dong-Young Chang, Lei Wu†, and Un-Ku Moon

ECE Oregon State University, Corvallis, OR 97331
† Marvell, Sunnyvale, CA

ABSTRACT

A low-voltage *opamp-reset switching technique* (ORST) which avoids clock boosting/bootstrapping, switched-opamp, and threshold voltage scaling is presented. The switching technique is applied to the design of a 10-bit 25MSPS pipelined ADC. The prototype ADC demonstrates 55dB SNR, 55dB SFDR, and 48dB SNDR at 1.4V power supply. The ADC operates down to 1.3V power supply ($|V_{TH,P}|$=0.9V) with 5dB degradation in performance. Maximum operating frequency is 32MSPS. The ORST is fully compatible with future low-voltage submicron CMOS processes.

I. INTRODUCTION

The continued down scaling of transistor dimensions in submicron CMOS technology brings much optimism to current and future digital IC systems. While this trend directly implies increased digital signal processing power, it also brings to attention difficult analog IC design challenges. One of the key analog limitations of the state-of-the-art and future submicron CMOS technologies remains the restricted power-supply voltage, limited primarily by the thin gate oxide that is prone to voltage stress reliability and breakdown.

One circuit type directly affected by this low-voltage problem is the switched-capacitor circuit, used in many practical analog signal processing applications including data converters. The fundamental limitation on the operation of a floating switch arises when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages. This is illustrated in Fig. 1.

There are several well-known approaches used to bypass this problem. These approaches include the clock boosting scheme (e.g. $2V_{DD}$ clock signal) [1] which cannot be used in the submicron low-voltage CMOS process; the use of scaled/lower threshold transistors which would suffer from an unacceptable amount of leakage current; the use of bootstrapped clocking [2]-[3] which imposes a temporary but large voltage glitch ($2V_{DD}$) across the gate oxide; and the switched-opamp (SO) technique [4] that is fully compatible with low-voltage submicron CMOS but speed limited by transients from the opamp being switched on/off.

This work was supported by the NSF Center for Design of Analog-Digital Integrated Circuits (CDADIC) and Lucent Technologies.

The topology of the *opamp-reset switching technique* (ORST) [5] for low-voltage operation that is fully compatible with current and future submicron CMOS technology is illustrated in Fig. 1. Note that the floating switch of the conventional stage is eliminated (like the SO), and the operation of the grounding/resetting switch used in both conventional and SO circuits is replaced by the sourcing opamp placed in the unity-gain configuration. Unlike the SO, ORST keeps the opamp active during the reset phase.

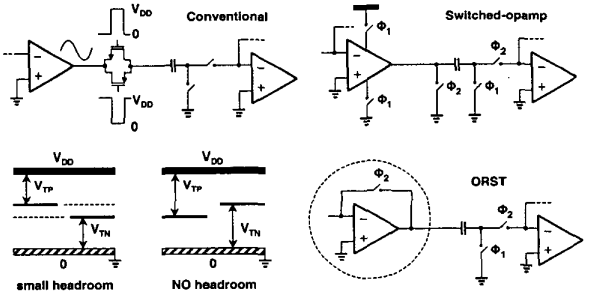

Figure 1: Conventional to low-voltage ORST topology.

II. LOW-VOLTAGE ADC DESIGN

A block diagram of a 10-bit 1.5-bit-per-stage pipelined ADC is presented in Fig. 2. The ADC is composed of 9 cascaded stages with a front-end input sampling circuit. The ORST is employed as a pseudo-differential form in MDACs and the input sampling circuit. The proposed MDAC is shown in Fig. 3. To avoid the common-mode error accumulation problem that would normally result in a pseudo-differential structure without common-mode feedback, cross-coupled feedback capacitors are used to realize the required residue amplification (differential) of 2 while yielding a reduced common-mode gain of 1. The small amount of differential positive feedback created due to cross coupling allows the differential gain of

$$A_{DIFF} = C_S/(C_{CM1} - C_{CM2}) = 2 \qquad (1)$$

0-7803-7250-6/02/$10.00 © 2002 IEEE

and the common-mode gain of

$$A_{CM} = C_S/(C_{CM1} + C_{CM2}) = 1. \qquad (2)$$

The common-mode is retained throughout the stages without requiring additional common-mode feedback circuitry. The reference injection circuits are shown at the top/bottom of the figure as separate branches. Due to the low-voltage operation, they could not be incorporated into the signal path with the capacitor flip-over topology (requires use of floating switches) as in the conventional MDAC [6]. Because the switches are to be connected only to high (V_{DD}) or low (GND) voltages for proper low voltage operation, the reference value is generated by a capacitor ratio. V_{REF} range of $V_{DD}/2$ is created by the input sampling to reference capacitors ratio of 8:1.

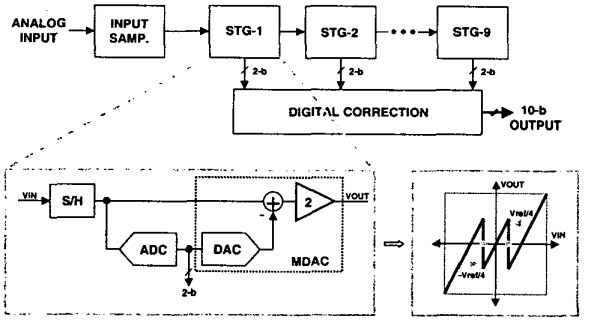

Figure 2: ADC block diagram.

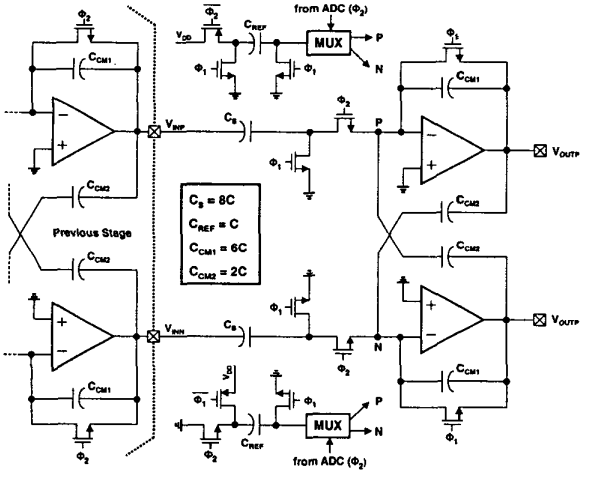

Figure 3: Pseudo-differential 1.5-bit MDAC using ORST.

A major challenge in the low-voltage ADC design is to sample and transfer signals accurately and fast from sources external to IC . One such circuit exists in the context of a SO structure [7]. Fig. 4 shows the proposed input sampling circuit. During the output reset phase (ϕ_2), V_{XP} is pulled up to V_{DD} while C_1 is precharged to V_{DD} and C_2 discharged. During the amplification phase (ϕ_1), V_{XP} becomes $V_{DD}/2$ (i.e. V_{batt}) due to charge sharing between C_1 and C_2. The buffered (inverting gain) input signal appearing at V_{OUTP} (V_{OUTN}) is sampled by the first stage MDAC during this phase. Assuming that the input common-mode voltage is $V_{DD}/2$, the output common-mode voltage also becomes $V_{DD}/2$ because of an intermediate virtual ground V_{XP}. However, the voltage division between R_1 and the on-resistance of MPP introduces nonlinear voltage fluctuation at V_{XP}. Since the output voltage is a function of V_{XP}, signal distortion results. Straightforward way to reduce the distortion is to increase the size of MPP which results in increasing the chip area. In the proposed circuit, a differential resetting switch MPC is employed. It can be made half the size of MPP and achieves the same performance as doubling the size of MPP. Using MPC also helps to suppress even harmonics, that are due to device mismatches in the two pseudo-differential signal paths.

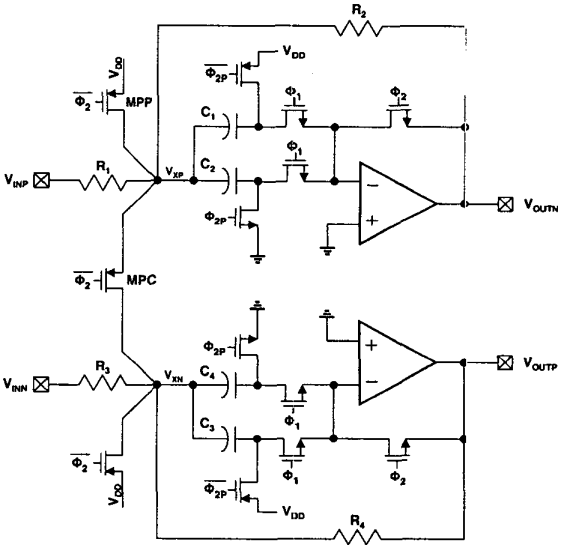

Figure 4: Low-voltage input sampling circuit.

The fully-differential comparator used in the flash ADC is shown in Fig. 5. Similar to the MDAC implementation, to avoid using floating switches, the effective $V_{REF}/4$ reference is provided by a separate capacitor branch C_R. The additional capacitor branch C_C effectively provides level shifting and voltage division to ensure that comparator input nodes T_P and T_N (gates of NMOS differential-pair) remain equal to or below V_{DD}.

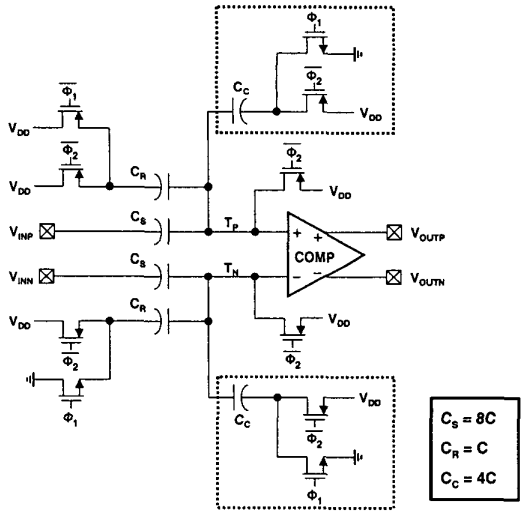

Figure 5: Fully-differential low-voltage comparator.

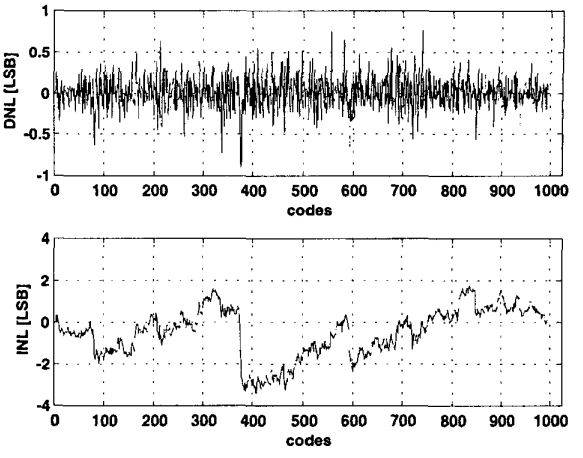

Figure 6: DNL and INL at 25MSPS.

III. Measured Results

The prototype ADC was fabricated in a $0.35\mu m$ CMOS technology where $|V_{TH,P}|$=0.9V and occupies $1.6mm \times 1.4mm$ of active die area. All measurements were obtained with a 1.4V power supply. For a 1MHz input at 25MSPS, measurements demonstrate 55dB SNR, 55dB SFDR, and 48dB SNDR. The measured DNL and INL at 25MSPS are shown in Fig. 6, and the dynamic linearity measurements are summarized in Fig. 7. The large INL jumps are expected to be coming from the poorly matched 0.1pF capacitors. The unchanging SFDR with respect to full scale (all spurious tones were harmonics) over input signal level down to -40dB indicates that the performance limitation is primarily due to poor capacitor matching. The total power consumption at 25MSPS and 1.4V is $21mW$. The prototype ADC is fully functional at 1.3V with 5dB performance degradation. As shown in Fig. 7, the ADC's maximum operating frequency is 32MSPS. The die micrograph is shown in Fig. 8. Table I summarizes the measured performance of the ADC.

IV. Conclusions

A low-voltage switching technique which avoids clock boosting/bootstrapping and switched-opamp is applied to the design of a 10-bit 25MSPS pipelined ADC. The prototype IC fabricated in $0.35\mu m$ CMOS with $|V_{TH,P}|$=0.9V occupies $1.6mm \times 1.4mm$ die area and demonstrates 55dB SNR, 55dB SFDR, 48dB SNDR at 1.4V.

References

[1] J. Wu, Y. Chang, and K. Chang, "1.2V CMOS switched-capacitor circuits," *IEEE ISSCC Dig. of Tech. Papers*, pp. 388–389, Feb. 1996.

[2] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14 MS/s CMOS pipeline analog-to-digital converter," *Symp. VLSI Circuits*, pp. 166–169, June 1998.

[3] J. Steensgaard, "Bootstrapped low-voltage analog switches," *Proc. IEEE Int. Symp. Circuits Syst.*, May 1999.

[4] J. Crols and M. Steyaert, "Switched opamp: an approach to realize full CMOS SC circuits at very low supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936–942, Aug. 1994.

[5] E. Bidari, M. Keskin, F. Maloberti, U. Moon, J. Steensgaard, and G. Temes, "Low-voltage switched-capacitor circuits," *Proc. IEEE Int. Symp. Circuits Syst.*, May 1999.

[6] S. Lewis, S. Fetterman, G. Gross, R. Ramachandran, and T. Viswanathan, "A 10-b 20-Msamples/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, Mar. 1992.

[7] A. Baschirotto, R. Castello, and G. P. Montagna, "Active series switch for switched-opamp circuits," *Electronics Lett.*, vol. 34, no. 14, pp. 1365–1366, July 1998.

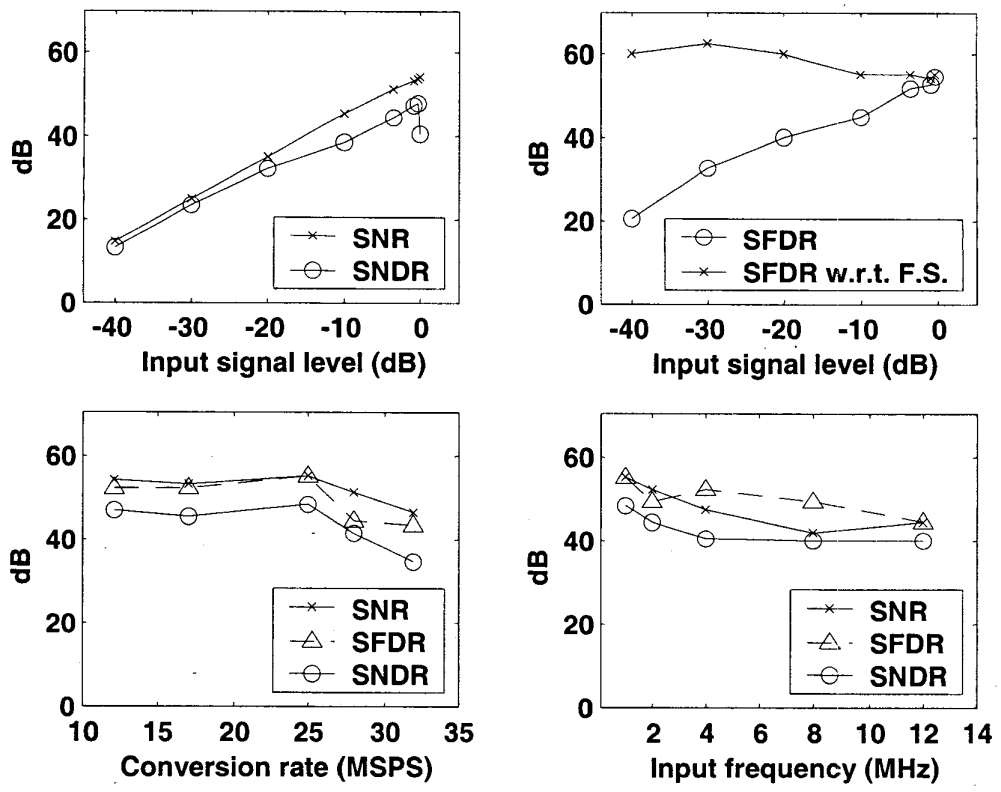

Figure 7: Dynamic measurements with 1MHz input and 25MSPS (unless noted otherwise).

Technology	0.35-μm 1P 5M CMOS
Resolution	10-bit
Chip size	1.6mm x 1.4mm
Supply voltage	1.4 V
Conversion rate	25 MSPS
Power consumption	21 mW
DNL / INL	0.9 LSB / 3.3 LSB
SNR / SNDR	55 dB / 48 dB
SFDR	55 dB

Table 1: Measurement summary.

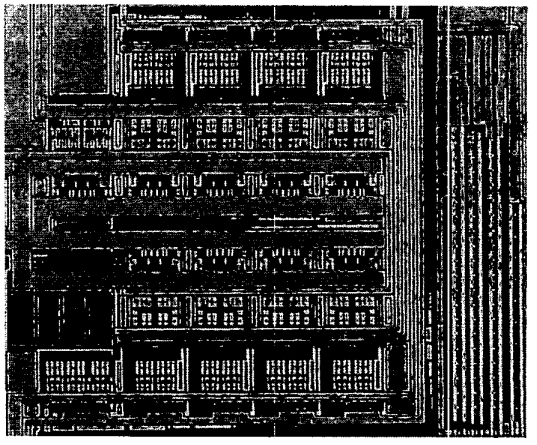

Figure 8: Die photograph.