Digital Techniques for Improved $\Delta\Sigma$ Data Conversion

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Abstract

Two digital techniques are described in this tutorial, both aimed at improving the accuracy of delta-sigma data converters. The first one corrects adaptively for mismatch errors in a MASH ADC, while the other acquires and then corrects for the nonlinearity of the internal multibit DAC used in the ADC.

1 Introduction

This tutorial describes two recently developed digital techniques which can achieve high-performance delta-sigma conversion while using low-performance analog components. The first technique performs an adaptive digital correction of analog errors in MASH ADCs to compensate for the mismatch between the analog and digital noise transfer functions [1]. The second technique acquires a digital estimate of the DAC element errors from the DAC input signal and the overall ADC output signal in multibit $\Delta\Sigma$ ADCs, after both signals were digitally preprocessed and then corrects the output signal. It is independent of the oversampling ratio, and does not raise the noise floor. Both techniques can be used in the background, continuously correcting not only for static defects but also for process variations caused by temperature and aging effects.

The tutorial is organized in two parts as follows. In the first part, the adaptive digital correction technique useful in MASH ADCs is described, and a typical hardware implementation shown. Design examples are given to illustrate the described principles. In the second part, the digital correlation technique for the estimation and correction of DAC errors in multibit MASH $\Delta\Sigma$ ADC is described. System level simulation results are shown to verify the theory.

2 Adaptive Quantization Noise Correction

2.1 Adaptive Correction Using Test Signal Injection

Figure 1 shows the simplified diagram of a 2-0 two-stage MASH ADC.

The key analog imperfections of the MASH ADC are the pole and gain errors of the first-stage integrators. Detailed analysis of the effects of these linear errors [11] [13] indicates that they introduce a parasitic leakage path for the first-stage quantization noise e_1 to the output v_m (Fig. 1), so that the output voltage in the z-domain is given by

$$V_{m_{real}}(z) = V_{m_{ideal}}(z) + H_{leakage}(z)\,E_1(z). \qquad (1)$$

Assuming small relative errors, the transfer function $H_{leakage}(z)$ of this noise leakage can be approximated well with a finite Taylor series expansion

$$\begin{aligned} H_{leakage}(z) &= \left.\frac{V_{m_{real}}(z)}{E_1(z)}\right|_{\substack{U_1(z)=0\\E_2(z)=0}} \\ &= A_0 + A_1(1-z^{-1}) + A_2(1-z^{-1})^2 \\ &\quad +\ldots + A_{M-1}(1-z^{-1})^{M-1}, \end{aligned} \qquad (2)$$

where the coefficients $A_0 \ldots A_{M-1}$ are functions of the DC op-amp gain A_{DC} and of the relative capacitor errors $\Delta_C = \frac{\Delta C_2}{C_2} - \frac{\Delta C_1}{C_1}$ of the integrators. The filtering effect of the $(1-z^{-1})^i$ factors depends on the oversampling ratio OSR. To estimate the order of magnitude of the noise leakage, the first five coefficients $A_0 \ldots A_4$ were calculated for the 2-0 MASH ADC, and presented in [11]. Assuming $A_{DC} = 54$ dB and $\Delta_C = 0.8\%$, the order of magnitude of A_0 is 10^{-6} and of $A_1 \ldots A_4$ it is 10^{-3} to 10^{-2}. The first two terms (A_0 and A_1) depend only on the finite DC op-amp gain A_{DC}, and A_0 is usually negligibly small. Note that an accurate *a priori* estimation of $A_0 \ldots A_M$ is not possible, because of the random nature of the variables A_{DC} and Δ_C. However, an accurate evaluation is necessary, because of the high sensitivity of the SNR performance to these values. In our approach, we have hence adopted an *adaptive* estimation of the errors introduced by these analog circuit imperfections [10]. This is explained below.

In the expression (2) for the noise-leakage transfer function $H_{leakage}(z)$, the output errors introduced by the terms $A_i(1-z^{-1})^i$ decrease rapidly with the order i of the term. This shows that the effect of the analog imperfections can be suppressed by incorporating in the structure a simple low-order digital correction path for the quantization error which cancels the leakage signal. This correction can be provided

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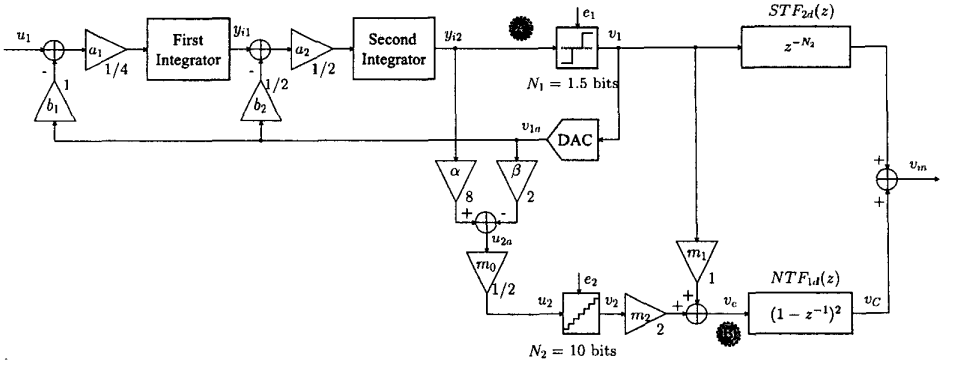

Figure 1: A 2-0 MASH topology

by an adaptive digital FIR filter $L_C(z)$ (Fig. 2) which adds a digital correction term v_L to the output v_m of the MASH [10]. Therefore, the digital correction signal v_L should be a negative estimate of the noise leakage.

Since the main component of v_e in Fig. 1 is the negative first-stage quantization noise $(-e_1)$ converted by the second stage, its z-transform is given by

$$V_e(z) = -E_1(z) + m_2 E_2(z) \cong -E_1(z), \qquad (3)$$

and hence the digital correction signal v_L in Fig. 2 is given by

$$V_L(z) = V_e(z)L_C(z) \cong -E_1(z)(l_0 + l_1 z^{-1} + l_2 z^{-2} + \ldots + l_{M-1} z^{-(M-1)}), \qquad (4)$$

where $L_C(z)$ has M coefficients l_i forming the vector $\boldsymbol{l} = [l_0, l_1, \ldots l_{M-1}]^T$. Eqs. (1), (2) and (4) indicate that v_L can be a negative estimate of the noise leakage if the coefficient vector $\boldsymbol{l}$ of the FIR filter $L_C(z)$ is properly chosen. Since the exact values of the analog imperfections are *a priori* unknown, the parameters of the digital correction filter $L_C(z)$ must be adaptively controlled.

2.2 Test-Signal Based Adaptation

For adaptively adjusting on-line the coefficient vector $\boldsymbol{l}$, a test signal ts is entered into the modulator at its least sensitive node, i.e. before the first-stage quantizer, and it is detected and adaptively cancelled in the output signal v_m (Fig. 2). The test signal ts is a pseudorandom, two-level zero-mean white noise, so it is uncorrelated with the input signal u_1 and with the quantization noises e_1 and e_2. The test signal is added to the quantization noise e_1, and it behaves similarly to the quantization noise. Since ts follows the same parasitic leakage path toward the output v_m as the quantization noise e_1, removing ts from the output v_m requires the same operation as removing the remainder of the quantization noise e_1 from v_m. In other words, the minimization of the test signal in the output is equivalent to the minimization of the noise leakage.

Even though the test signal has statistical properties similar to those of band-limited white noise, it is deterministic and fully known. Therefore, it can be detected in the output v_m by using a correlation process between the output v_m and the digital replica of ts (Fig. 2) which generates an error signal. This error signal is then used to update the coefficient vector $\boldsymbol{l}$ by a gradient method such as the block least-mean-square (BLMS) algorithm [15]. For simple hardware implementation, we chose the sign-sign version of the BLMS (SSBLMS) algorithm [11]. The update equation is given by

$$\boldsymbol{l}[(j+1)K] = \boldsymbol{l}[jK] - \gamma \ \text{sign}\left\{\sum_{k=0}^{K-1} v_m[jK-k] \ \text{sign}\{\boldsymbol{ts}[jK-k]\}\right\}, \qquad (5)$$

where K is the block size, j is the current adaptation step and γ is the adaptation coefficient. The M-element column vector $\boldsymbol{ts}[jK-k]$ contains the entries $ts[jK-k]$, $ts[jK-k-1]$, $\ldots ts[jK-k-(M-1)]$. Of course, the same adaptive scheme can be used without a test signal by replacing the test-signal

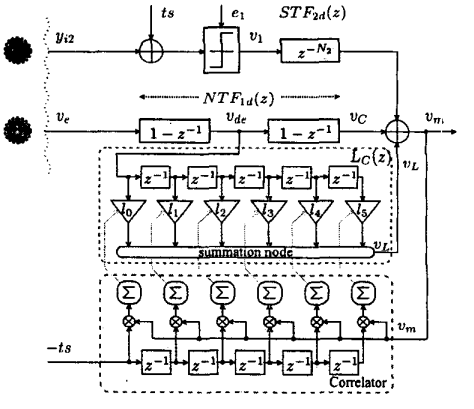

Figure 2: Block diagram of the adaptive error correction scheme.

power measurement with the first-stage quantization error e_1 measurement. But the power of e_1 cannot be measured with the same accuracy, because e_1 is not known, and it is strongly correlated with the input signal u_1. Therefore, an adaptation process using the correlation between v_m and e_1 is input-signal dependent, and hence it is more suitable for *off-line* calibration. However, the test-signal approach described in this paper offers a robust *on-line* error correction strategy.

Since the test signal ts is uncorrelated with other components of the output signal v_m such as u_1, e_1 and e_2, its power can be measured selectively. Simulations show that even if the test-signal power is much lower than the power of other components of the output signal v_m (say, 1% of the full scale input signal power), its power can still be determined with high accuracy, and hence the updating of the coefficient vector $\boldsymbol{l}$ can be done accurately. Note that the error correction using the test signal ts takes place on-line, in the background during the actual data conversion, so it can follow any drift introduced, e.g. by aging or temperature changes. Also, the test signal acts as a dither signal for the first stage of the MASH, thus improving its performance [16, Chapter 3].

A minor drawback of using test-signal injection is a slight loss ($\sim$1 dB) in the dynamic range due to the earlier overflow of the first-stage quantizer. Finally, note that the proposed test-signal approach is a *linear* correction method, so it can be used only for correcting linear errors, but not any harmonic distortion introduced by the analog circuitry [7].

2.3 Adaptive Filter Implementation

To update the coefficient vector $\boldsymbol{l}$ of $L_C(z)$, the simple SSBLMS algorithm was selected, since it can be implemented using digital logic circuitry with finite precision, and integrated on the same chip with the MASH modulator. Therefore, high-speed multiplications in the correlator are replaced by summations, and the updating of the coefficients in $\boldsymbol{l}$ can be performed by simple additions or subtractions with a constant step size γ, as illustrated by eq. (5). These are performed as up-down counting operations in the SSBLMS update, which are easy to implement especially if γ is chosen to be equal to the step size (1 LSB) of the coefficient vector $\boldsymbol{l}$. Then, every update requires only $K \cdot M$ additions. Since the updating is performed only once after each K samples, M additions per sample are required [11]. The resulting hardware implementation of the compensation filter $L_C(z)$ is presented in Fig. 3 (on the next page). The estimated die size of this adaptation digital logic is 0.57 mm^2 in a 0.25 μm standard CMOS process. It allows high-speed operation [13].

2.4 Design Examples

2.4.1 2-0 MASH ADC with 1-bit First-Stage Quantization

In this first design, a simple 2-0 MASH ADC was considered, which was then successfully fabricated and tested [12] [13] in order to get a working prototype for the adaptive error-correction scheme, and to verify the simulation results [10]. The first-stage modulator was chosen to be a second-order single-bit ($N_1 = 1$ bit) delta-sigma modulator, followed by an external multibit ($N_2 = 12$ bit) pipelined ADC. The interstage coupling (α, β, m_0, m_1 and m_2 of Fig. 1) was designed to allow the lowest possible analog hardware complexity, which eliminates the analog subtraction block ($\alpha = 1$, $\beta = 0$). This simple interstage coupling circuit results in a loss of approximately 6 dB in the dynamic range of the modulator compared to the general coupling path presented in Fig. 1. However, this degradation was considered acceptable, because the main purpose of this design was to show the effectiveness of the adaptive noise-leakage compensation rather than producing an ADC optimized for dynamic range.

The second-order first stage incorporating the test-signal path was fabricated in the Orbit 1.2 μm double-poly CMOS process [12]. The die photo is shown in Fig. 4. The MASH operated at a $f_S = 1$ MHz sampling rate and $OSR = 4$. The second stage was realized by an AD9220 chip. The digital outputs of the two chips were collected by a data-acquisition board and post-processed in a PC. Fig. 5 shows the measured output spectra with and without compensation for a sine-wave input. The input signal frequency was 1.5 kHz, and the full-scale differential input voltage was 5 V_{pp}. Using compensation, the $SNDR$ (Fig. 6) was improved by 16 to 18 dB over the linear input signal range, which verified the effectiveness of the compensation.

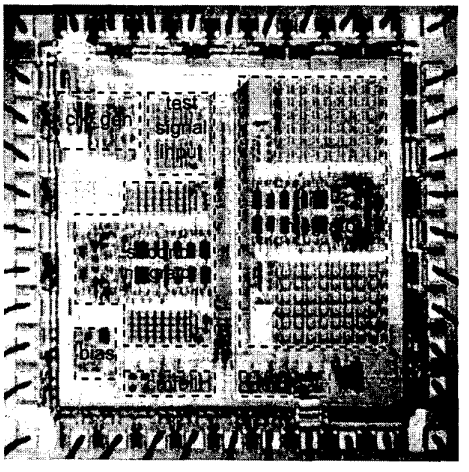

Figure 4: Die photo of the second-order delta-sigma modulator.

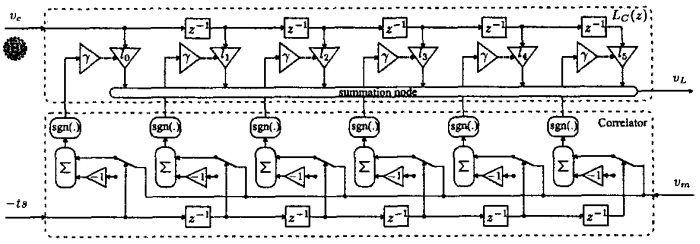

Figure 3: Hardware implementation of $L_C(z)$ using the SSBLMS algorithm for coefficient update.

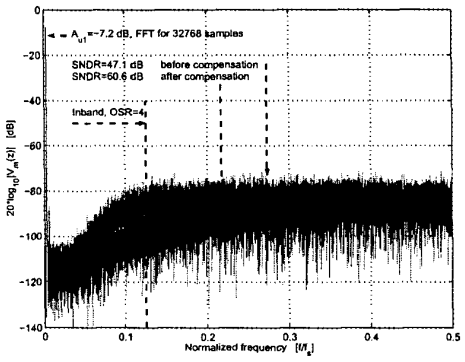

Figure 5: Measured output spectra.

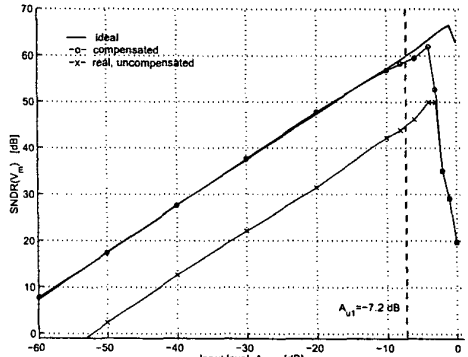

Figure 6: Measured SNDR of prototype 2-0 MASH ADC, with and without correction.

2.4.2 2-0 MASH ADC with 1.5-bit First-Stage Quantization

Next, an improved 2-0 MASH ADC structure is presented (Fig. 1). There are several structural changes [14]. The multiplier $m_0 < 1$ was added to prevent the second stage from overloading. To compensate for this attenuation, the digital output v_2 must be scaled up by $m_2 = \frac{1}{m_0} > 1$, which amplifies the quantization noise e_2 of the second stage, and reduces the SNR of the system. In this structure, by adjusting β and m_1, an optimal weighting of the input y_{i2} and the output v_{1a} of the first-stage quantizer in the second-stage input signal u_{2a} can be achieved. This results in the largest possible value for m_0 and, in turn, the least possible amplification of the quantization noise e_2 [16, Section 7.3.1].

The usable input signal range u_1 was also increased by a modification in the first stage. Using a tri-level quantizer in the first stage instead of a simple comparator [18], the usable input signal range u_1 was extended by 6 dB (Fig. 8). The linearity of the tri-level feedback DAC is critical, but a highly-accurate tri-level DAC was described in [19] which used extra switches and simple circuitry to insure linearity. This tri-level quantizer offers a good trade-off between SNR performance and circuit complexity, especially if one wants to avoid a multibit mismatch-shaping DAC [16, Section 8.3.3] in order to reduce the chip area. The optimized parameters are also shown in Fig. 1.

To obtain a large-bandwidth and high-resolution ADC, a high sampling frequency ($f_S = 100$ MHz) was chosen combined with a low oversampling ratio ($OSR = 8$). For the second stage, a 10-bit pipelined ADC was chosen. Because the coefficient $\beta \neq 1$, a delayed version of the analog input signal u_1 is introduced into the second-stage input u_2. Therefore, the nonlinearities of the second stage may affect the linearity of the overall system. However, the harmonics of u_1 introduced by the pipelined ADC are attenuated by $NTF_{1d}(z)$, e.g. by 18 dB for $OSR = 8$, so a 13-bit linear performance is still easily achievable. Note that the linearity requirement for the second stage can be relaxed if $\beta = 1$ is chosen, and hence $u_{2a} = -e_1$ (Fig. 1). Therefore, the nonlinearity of the pipelined ADC will not introduce harmonic distortion of the input signal u_1, but only a colored pseudo-noise error [20].

However, $\beta = 1$ changes the probability density function of u_{2a}, which causes an approximately 6 dB drop in the SNR compared to when $\beta = 2$. In conclusion, one should be aware of the THD *versus* SNR trade-off described above.

With an input sampling capacitor $C_S = 6$ pF, the $\frac{kT}{C}$ noise floor can be lowered to -92 dB (15 bits). The progression of the adaptive process is illustrated in Fig. 7, and the resulting performance is presented in Fig. 8; a peak SNR of 86 dB was obtained for the optimized 2-0 MASH structure presented in Fig. 1. Due to the analog circuit imperfections, the SNR performance drops by more than 25 dB (Fig. 8). However, as shown in the same Figure, using the adaptive error correction method the effects of the analog circuit imperfections can be nearly completely suppressed.

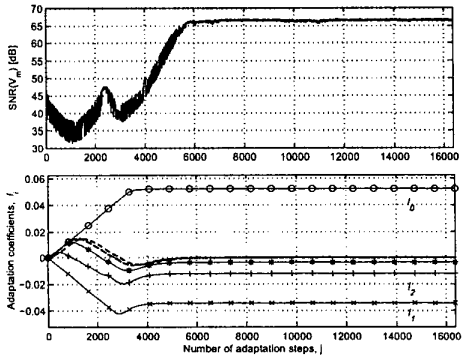

Figure 7: Convergence curves for an adaptive error-correction process.

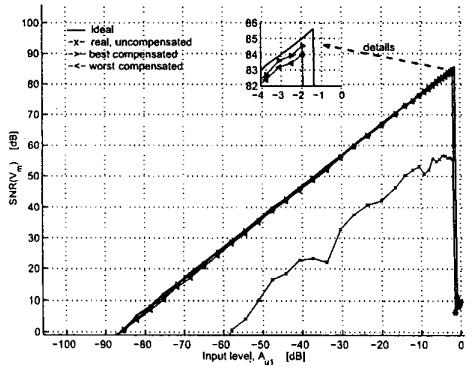

Figure 8: Simulated SNR performance before and after correction.

3 Digital Estimation and Correction of DAC Errors in Multibit $\Delta\Sigma$ ADCs

3.1 Principle of the estimation and correction

Next, the digital algorithm correcting for multibit DAC nonlinearities will be discussed.

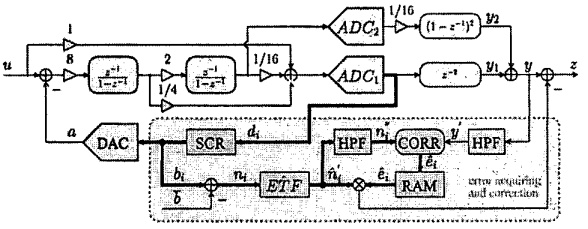

Figure 9: MASH ADC with the proposed error correction system.

Fig. 9 shows a MASH $\Delta\Sigma$ ADC which uses the proposed technique. The first stage of the ADC is a second-order structure with relaxed linearity requirements on the first integrator proposed in [24]. Here, it uses a multibit quantizer. Errors of the DAC in its feedback path limit the overall conversion linearity and need to be corrected. The DAC has $M+1$ levels and M unit elements, so the thermometer-coded output of the ADC, $d(k)$, has a wordlength of M. A scrambler (SCR) precedes the DAC which randomly reorders these M bits. $b(k)$ is the scrambled data, each bit of which determines the use of one unit element. Suppose each unit element has an ideal output value of 1. The average of their real outputs are α. The real output of the ith element deviates from α by e_i, and

$$\sum_{i=1}^{M} e_i = 0. \tag{6}$$

Then, the output of the DAC is

$$a(k) = \alpha \sum_{i=1}^{M} b_i(k) + \alpha \sum_{i=1}^{M} b_i(k) \cdot e_i + v_{off}, \tag{7}$$

where v_{off} is the constant DAC offset. Each error e_i is modulated by a sequence $b_i(k)$.

In the output of the ADC, the modulated errors are also affected by the DAC error transfer function, as shown below:

$$\begin{aligned} y(k) \;=\; & u(k) \circledast stf(k) + q(k) \circledast ntf(k) \\ & + \alpha \sum_{i=1}^{M} [b_i(k) \circledast etf(k)] \cdot e_i + v_{off} \circledast etf(k), \end{aligned} \tag{8}$$

where $u(k)$ is the input signal and $q(k)$ is the quantization noise introduced by the quantizer in the second stage, while $stf(k)$, $ntf(k)$ and $etf(k)$ are the impulse responses of signal transfer function, noise transfer function and DAC error

transfer function, respectively. The symbol $\circledast$ denotes discrete convolution.

To acquire the error values from the ADC output, we need to suppress sufficiently the interferences from the input signal, quantization noise and DAC offset. The input signal is at lower frequencies, and hence can be partially suppressed by a high-pass filter, which also suppresses the DAC offset. This filtering will not attenuate the modulated errors too much, because due to the random scrambling the $b_i(k)$ have their power distributed over a wide spectrum. For the quantization noise, which also has a wide spectrum, filtering does not work. However, quantization noise is a random signal and is uncorrelated with the modulated errors. Therefore, correlating the high-pass-filtered ADC output with the modulating sequences $b_i(k)$ should suppress the quantization noise and extract the errors. Unfortunately, the sequences $b_i(k)$ used in the correlation are correlated among themselves, so the result contains linear combinations of the errors. To separate out single errors, which is necessary for later correction, the exact relationship between the sequences should be known.

Sequences $b_i(k)$ can be separated into two parts: the mean value of all M bit streams plus the individual deviations $n_i(k)$ [25]:

$$b_i(k) = \frac{1}{M}\sum_{j=1}^{M} b_j(k) + n_i(k) \tag{9}$$

Here,

$$n_i(k) = -\sum_{j=1, j\neq i}^{M} n_j(k) \tag{10}$$

holds. The sequences $n_j(k)$ on the right side of (10) can be separated into two parts, a scaled version of $n_i(k)$ plus a sequence $m_i(k)$ which is uncorrelated with $n_i(k)$:

$$n_j(k) = -\beta \cdot n_i(k) + m_j(k), \qquad j = 1 \ldots M, j \neq i \tag{11}$$

Because the scrambling is random, all $n_j(k)\,(j = 1 \ldots M,\ j \neq i)$ have equal status. It is reasonable to assume and was also verified by simulations that β is constant for all j's in (11). From (10), $\beta = (M-1)^{-1}$. Since the $n_i(k)\,(i = 1 \ldots M)$ obey such simple relations, we can use them rather than the $b_i(k)$ as the correlating sequences. Combining (7), (6) and (9), we have

$$a(k) = \alpha\sum_{i=1}^{M} b_i(k) + \alpha\sum_{i=1}^{M} n_i(k)\cdot e_i + v_{off} \tag{12}$$

and

$$\begin{aligned} y(k) &= u(k) \circledast stf(k) + q(k) \circledast ntf(k) \\ &\quad + \alpha\sum_{i=1}^{M} n_i'(k)\cdot e_i + v_{off} \circledast etf(k), \end{aligned} \tag{13}$$

where

$$n_i'(k) = n_i(k) \circledast etf(k).$$

The errors e_i are thus modulated by $n_i(k)$ at the DAC output.

The larger the power of the quantization noise, the more clock periods are needed to suppress it. MASH ADCs often have much less quantization noise power in their final outputs than single-loop $\Delta\Sigma$ ADCs. This is the reason we propose the technique in the context of a MASH ADC here.

On the basis of the derivation given above, the error acquiring and correction process is performed as follows (see Fig. 9): as indicated in (9), $\bar{b}(k) = \frac{1}{M}\sum_{i=1}^{M} b_i(k)$ is subtracted from $b(k)$. The estimate of $n_i'(k)$ is obtained in the digital domain then by filtering $n_i(k)$ with a digital filter $E\hat{T}F$, emulating ETF, resulting in $\hat{n}_i'(k)$. The result enters the same high-pass filter (HPF) that is used to suppress the input signal and becomes $n_i''(k)$. Finally, the $n_i''(k)$ are correlated (in block CORR) with the high-pass-filtered ADC output $y'(k)$, giving

$$\hat{e}_i(k) = \left(\frac{M-1}{M}\right) \cdot \frac{\sum_{m=0}^{k}[y'(m)\cdot n_i''(m)]}{\sum_{m=0}^{k}[n_i''(m)]^2}. \tag{14}$$

The scale factor of $\frac{M-1}{M}$ is derived from (11).

The estimated results $\hat{e}_i$ are stored in the RAM and are updated in every clock period. They are read out to multiply the $\hat{n}_i'(k)$, $i = 1 \ldots M$, and the result is subtracted from $y(k)$ to give the corrected output

$$z(k) = y(k) - \sum_{i=1}^{M}[\hat{n}_i'(k)\cdot \hat{e}_i]. \tag{15}$$

3.2 Simulation results

All simulations were done using Simulink and the Schreier Toolbox for $\Delta\Sigma$ Modulators [26]. The multibit DAC in the first stage was assumed to have 33 levels and 32 unit elements. The value of α was assumed to be 1. A random 0.1% rms error was introduced into the unit elements when modeling the real DAC. Fig. 10(a) shows the output spectra of the MASH ADC using an ideal DAC as well as using a real DAC, with no calibration or dynamic element matching used. Here the clock frequency was 100 MHz and the oversampling ratio was 4. With a 1.56 MHz, -0.92 dB sine-wave input, the output SNDR was 102.6 dB for the ideal case and 76.2 dB for the real case.

The simulation results of two dynamic element matching algorithms under the same conditions are shown. Zero-order randomization only caused a 3.1 dB improvement in the SNDR, since it raised the noise floor, althought it removed

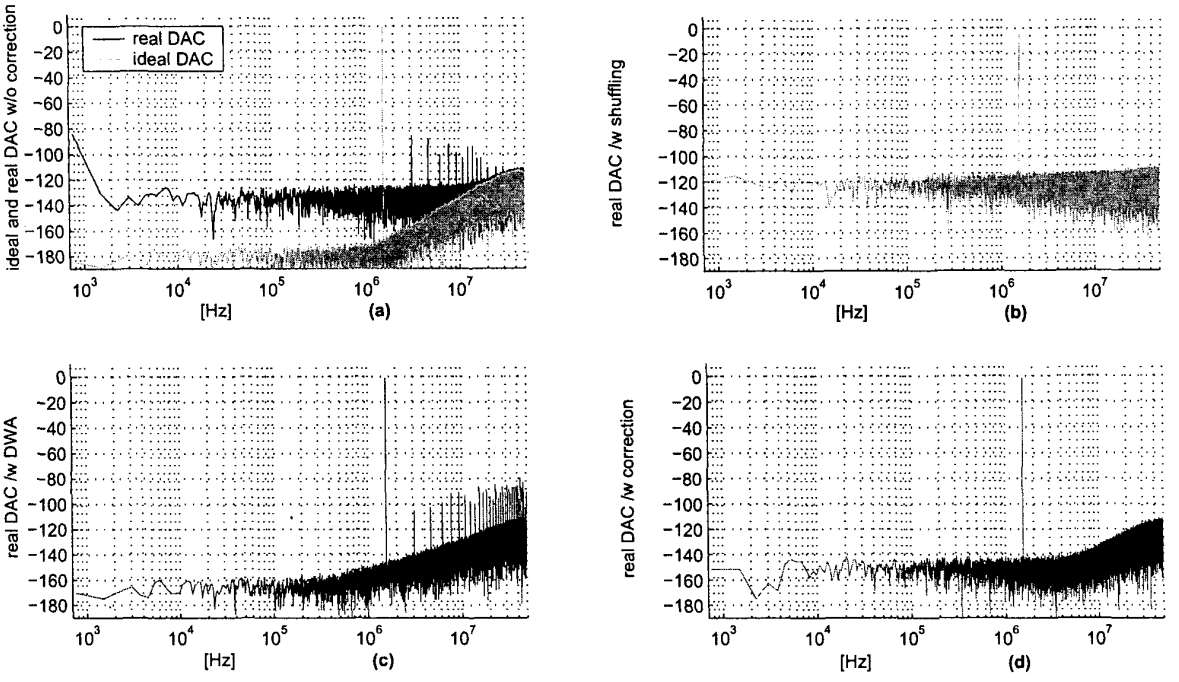

Figure 10: Simulation results.

the tones, as shown in Fig. 10(b). Data-weighted averaging lowered the noise floor, but caused strong signal-dependent tones and only achieved an SNDR of 85.2 dB, as shown in Fig. 10(c). Using the same real DAC, the proposed technique raised the output SNDR to 101.5 dB under the same conditions after a correction process lasting 131,072 clock periods. The output spectrum is shown in Fig. 10(d).

4 Conclusions

Two digital techniques were described in this tutorial, both aimed at improving the accuracy of delta-sigma data converters while using low-performance analog components.

Acknowledgments

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References

[1] P. Kiss, J. Silva, A. Wiesbauer, T. Sun, U. Moon, J. Stonick, and G. Temes, "Adaptive digital correction of analog errors in MASH ADCs — Part II. Correction using test-signal injection," *IEEE Transactions on Circuits and Systems — II: Analog and Digital Signal Processing*, pp. 629-638, July 2000.

[2] G. Cauwenberghs and G. C. Temes, "Adaptive digital correction of analog errors in MASH ADCs — Part I. Off-line and blind on-line calibration," *IEEE Transactions on Circuits and Systems — II: Analog and Digital Signal Processing*, vol. 47, no. 7, July 2000.

[3] A. Marques, V. Peluso, M. S. Steyaert, and W. M. Sansen, "Optimal parameters for delta-sigma modulator topologies," *IEEE Transactions on Circuits and Systems — II: Analog and Digital Signal Processing*, vol. 45, no. 9, pp. 1232–1241, September 1998.

[4] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, delta-sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 927–936, July 1999.

[5] F. Medeiro, B. P. Verdu, and A. R. Vazquez, "A 13-bit, 2.2-MS/s, 55-mW multibit cascade delta-sigma modu-

lator in CMOS 0.7-μm single-poly technology," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 748–760, June 1999.

[6] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. D. Muro, and S. W. Hartson, "A cascaded sigma-delta pipeline A/D converter with 1.25 MHz signal bandwidth and 89 dB SNR," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1896–1906, December 1997.

[7] G. Cauwenberghs and G. C. Temes, "Adaptive calibration of multiple quantization oversampled A/D converters," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, June 1996, vol. 1, pp. 512–515.

[8] S. Abdennadher, S. Kiaei, G. C. Temes, and R. Schreier, "Adaptive self-calibrating delta-sigma modulators," *IEE Electronics Letters*, vol. 28, no. 14, pp. 1288–1289, July 1992.

[9] Y. Yang, R. Schreier, G. C. Temes, and S. Kiaei, "On-line adaptive digital correction of dual-quantization delta-sigma modulators," *IEE Electronics Letters*, vol. 28, no. 16, pp. 1511–1513, July 1992.

[10] A. Wiesbauer and G. C. Temes, "Adaptive compensation of analog circuit imperfections for cascaded sigma-delta modulators," in *Proceedings of the Asilomar Conference on Circuits, Systems and Computers*, November 1996, vol. 2, pp. 1073–1077.

[11] A. Wiesbauer and G. C. Temes, "Adaptive digital leakage compensation for MASH delta-sigma ADCs," Research report, Oregon State University, Department of Electrical and Computer Engineering, July 31, 1997.

[12] T. Sun, A. Wiesbauer, and G. C. Temes, "Adaptive compensation of analog circuit imperfections for cascaded delta-sigma ADCs," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, June 1998, vol. 1, pp. 405–407.

[13] Tao Sun, *Compensation Techniques for Cascaded Delta-Sigma A/D Converters and High-Performance Switched-Capacitor Circuits*, Ph.D. thesis, Oregon State University, Department of Electrical and Computer Engineering, September 21, 1998.

[14] P. Kiss, J. Silva, J. T. Stonick, U. K. Moon, and G. C. Temes, "Improved adaptive digital compensation for cascaded delta-sigma ADCs," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2000, vol. 1.

[15] G. A. Clark, S. K. Mitra, and S. R. Parker, "Block implementation of adaptive digital filters," *IEEE Transactions on Circuits and Systems*, vol. CAS-28, no. 6, pp. 584–592, June 1981.

[16] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*, New York: IEEE Press, 1996.

[17] T. C. Leslie and B. Singh, "An improved sigma-delta modulator architecture," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 1990, pp. 372–375.

[18] J. J. Paulos, G. T. Brauns, M. B. Steer, and S. H. Ardalan, "Improved signal-to-noise ratio using tri-level delta-sigma modulation," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 1987, pp. 463–466.

[19] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr., R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, March 1992.

[20] Jesper Steensgaard-Madsen, *High-Performance Data Converters*, Ph.D. thesis, The Technical University of Denmark, Department of Information Technology, March 8, 1999.

[21] W. Qin, B. Hu, and X. Ling, "Sigma-delta ADC with reduced sample rate multibit quantizer," *IEEE Transactions on Circuits and Systems — II: Analog and Digital Signal Processing*, vol. 46, no. 6, pp. 824–828, June 1999.

[22] A. Panigada, "14-bit 20-MS/s 4x oversampled cascaded delta-sigma-pipelined A/D converter for broadband communications," M.S. thesis, Universitá di Pavia, Facultá di Ingegneria, July 1999, in Italian.

[23] M. Sarhang-Nejad and G. C. Temes, "A high-resolution multibit sigma-delta ADC with digital correction and relaxed amplifier requirements," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, pp. 648–660, June 1993.

[24] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "A wideband low-distortion delta-sigma ADC topology," *IEE Electronics Letters*, 2001, **37**, (12), pp. 737–738

[25] J. Steensgaard, "Adaptive delta-sigma modulator," Research report, Oregon State University, Department of Electrical and Computer Engineering, 12 August 2000.

[26] Richard Schreier, "The delta-sigma toolbox 5.1 for Matlab 5.0," Matlab code and documentation, 1998, `ftp://ftp.ece.orst.edu/pub/delsig.tar.Z`