A 2.5V 10b 120 MSample/s CMOS Pipelined ADC with high SFDR

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Abstract

A 10b multibit-per-stage pipelined ADC incorporating *merged-capacitor switching* (MCS) technique achieves better than 53 dB SNDR at 120 MSample/s and 54 dB SNDR and 68 dB SFDR for input frequencies up to Nyquist at 100 MSample/s. The measured DNL and INL are ±0.40 LSB and ±0.48 LSB, respectively. The ADC fabricated in a 0.25 μm CMOS occupies 3.6 mm^2 active die area and consumes 208 mW under a 2.5V power supply.

Introduction

The dramatic growth in the high-tech sector of the consumer market has created many unprecedented challenges in the area of integrated circuits. The present and future communication systems including high-speed modems and broadband wired and wireless communication subsystems require increasingly higher performance ADCs. The required level of accuracy can exceed 10b at conversion speed of hundreds of megahertz. The pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed trade-off between speed, power consumption, and die area (1)-(7). The CMOS ADCs recently reported with a sampling rate above 50 MSample/s at more than 10b resolution are illustrated in Fig. 1 (1)-(9). A parallel pipeline ADC (5) demonstrated the 46 dB total harmonic distortion at 200 MSample/s with a 0.5um CMOS process, and some mismatches between four channels degraded the full dynamic performance of the ADC.

This work describes design considerations for a new multibit-per-stage pipelined ADC architecture that has resulted in a single-channel 10b 120 MSample/s performance. This prototype includes the IC realization of the merged-capacitor switching (MCS) technique, which enjoys the benefit of employing only 8 unit-size capacitors for a 4-bit multiplying analog-to-digital converter (MDAC) instead of 16 capacitors normally required in the conventional MDAC architecture (10).

Proposed ADC Architecture

The block diagram of the proposed 10b pipelined ADC is illustrated in Fig. 2. It is based on a conventional three-stage pipelined architecture. The ADC consists of an input sample-and-hold amplifier (SHA), two 4b MDACs, three 4b subranging flash ADCs, and some extra supporting circuit

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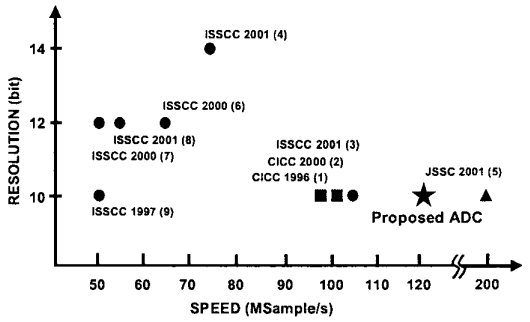

Fig. 1. Recently reported high-speed high-resolution CMOS ADCs.

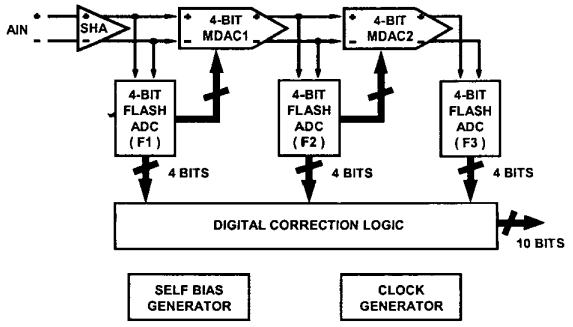

Fig. 2. Proposed 10b 120 MSample/s ADC.

blocks. Two non-overlapping clock phases are internally generated for concurrent operations of all stages to convert analog input signals to digital output codes. Each of the three stages generates a 4b digital code from the flash ADC, and the digital codes are processed in the digital correction/ redundancy logic yielding a final 10b word.

Design Issues for the proposed ADC

A. MCS technique

The MCS technique merges two unit capacitors into one without affecting the performance of the remaining circuits of the ADC. This means the number of unit capacitors required in a conventional MDAC is reduced by 50 %. This is illustrated in Fig. 3. For a given minimum-size unit capacitor, the operating speed of amplifiers can be increased with less power consumption since the total load capacitance is roughly reduced by half. Alternately, the unit capacitor size may be doubled to obtain the better capacitor matching accuracy while speed and power consumption remain unchanged.

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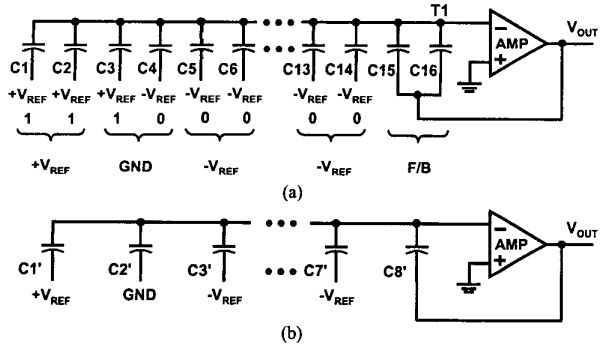

Fig. 3. MDAC during amplification based on : (a) conventional and (b) proposed MCS techniques.

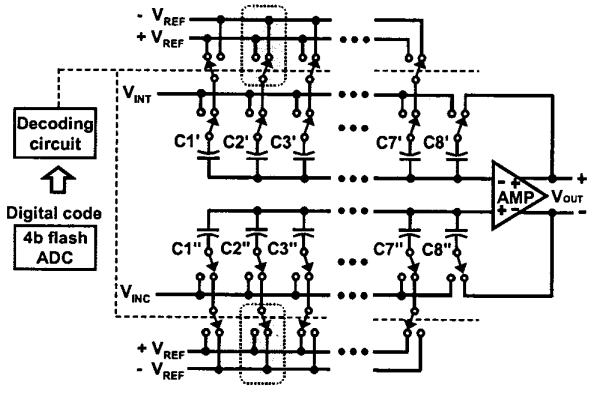

Fig. 4. Fully differential 4b MDAC based on the proposed MCS technique.

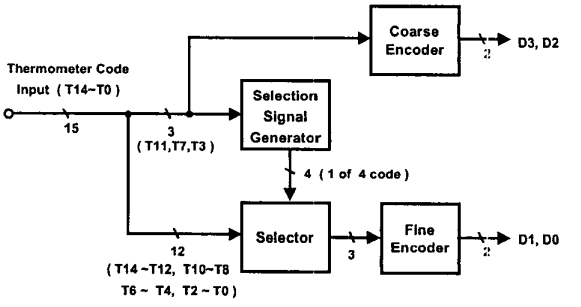

Fig. 5. Block diagram of the proposed encoding.

Table 1. Encoding from a thermometer code to a binary code.

THERMOMETER CODE															BINARY CODE			
T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

A conventional 4b MDAC has 16 unit capacitors, a residue amplifier, and a decoding circuit to control the switches connected to the capacitors. During the sampling phase, all the MDAC capacitor bottom plates are connected to the analog input voltage V_{IN}, which is the output of the previous stage. During the following amplification phase, as shown in Fig. 3 (a), each bottom plate of capacitors C1 to C14 is connected to $+V_{REF}$ or $-V_{REF}$, depending on the digital code generated by the flash ADC. The two remaining capacitors C15 and C16 are connected to the amplifier output, V_{OUT}, for proper residue amplification (8x).

The MCS technique, as illustrated in Fig. 3 (b), reduces the required number of MDAC capacitors by half, by merging 8 pairs of capacitors, C1&C2, C3&C4, ... , C15&C16, into 8 new unit capacitors C1' to C8'. The function of the proposed MDAC employing MCS is identical to that of the conventional MDAC. The only difference is that the signal ground (GND) is used in the MCS technique, when two different references ($+V_{REF}$ and $-V_{REF}$) are applied to two unit capacitors in the conventional MDAC. It is noted, for example, that C3 and C4 of Fig. 3 (a) are directly mapped to the function of C2' in Fig. 3 (b). In this design, only the capacitor C8' is switched to the output, V_{OUT}. However, by allowing different capacitors to switch to V_{OUT} according to a different digital code, this MCS structure can easily lend itself to the commutated feedback capacitor switching (CFCS) technique (10)-(11). In the fully differential implementation, any fixed bias voltage can be employed so that the GND reference is not needed. The 4b MDAC with the proposed MCS technique is implemented as shown in Fig. 4. In this prototype IC implementation, $-V_{REF}$ was employed for GND to simplify layout and to minimize the floating node effect, although a floating differential reset switch can be employed (12).

B. Proposed Encoding Scheme of flash ADCs

The proposed encoder of subranging flash ADCs employs a logic-based two step encoding scheme to reduce chip area and power consumption instead of a ROM-based encoding. Fig. 5 shows the block diagram of the proposed encoding and Table 1 illustrates encoding from a thermometer code to a binary code. The proposed encoding circuit is partitioned into the coarse and fine encoders. Three bits T11, T7, and T3 are used as inputs of the coarse encoder and concurrently used to select one group as inputs of the fine encoder between four

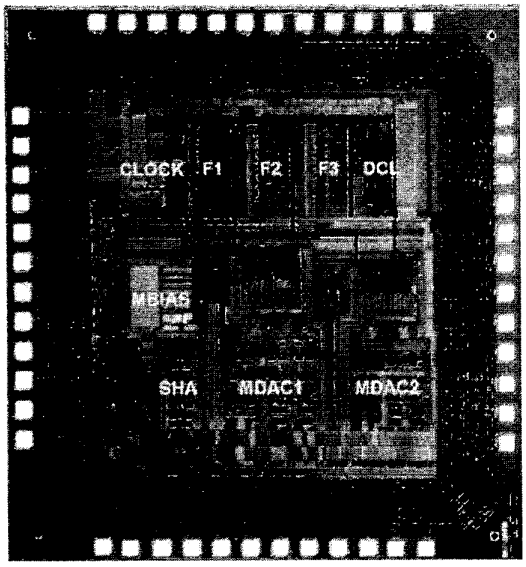

Fig. 6. Die photograph of the prototype ADC.

groups of three bits (T2-T1-T0, T6-T5-T4, T10-T9-T8, and T14-T13-T12). Three bits T11, T7, and T3 and the selected group of three bits are passed to the coarse and fine encoders which respectively generate the two most significant bits and the two least significant bits. While conventional encoding circuitry may be used to implement each of encoders in accordance with the Table 1, the proposed ADC uses a logic-based encoder to simplify implementation. The number of MOS transistors and power consumption can be halved with the proposed encoding circuit instead of the conventional ROM-based encoder.

C. Circuit Implementation

Taking into consideration kT/C noise and adequate capacitor matching for 10b accuracy, the input capacitance used in the SHA is 1.2 pF and the unit capacitance of the first stage MDAC is 0.2 pF. The conventional architecture with 2 sampling capacitors is employed in the SHA to achieve small die area and low power consumption. A two stage Miller-compensated amplifiers with a DC gain of 100 dB are used in the MDAC. The ADC is optimized to operate with a maximum $2V_{p\text{-}p}$ input signal swing at a 2.5V supply voltage.

Prototype Measurements

The proposed ADC is fabricated in a 0.25 μm double-poly five-metal CMOS process. The prototype, shown in Fig. 6, occupies 3.6 mm^2 (= 1.8 × 2.0 mm^2) active die area, and dissipates 208 mW when operated with 120 MHz clock and 2.5V supply. In the IC measurements setup, external low-pass or band-pass filters at the inputs suppress the harmonics and noise from the test signal generator, and a transformer provides a clean single to differential input signal conversion.

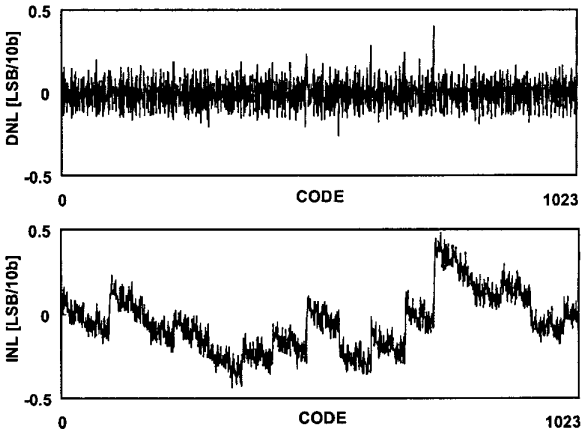

Fig. 7. Measured DNL and INL.

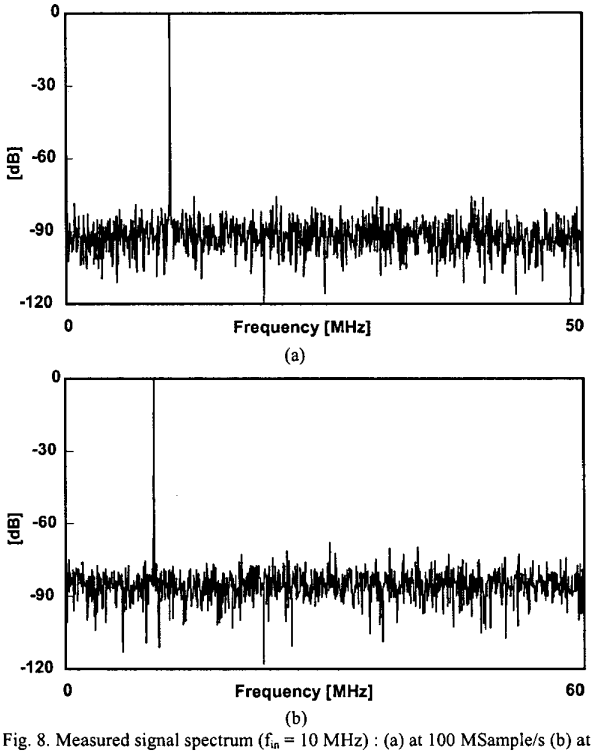

Fig. 8. Measured signal spectrum (f_{in} = 10 MHz) : (a) at 100 MSample/s (b) at 120 MSample/s.

External buffers connected to the ADC digital output drive high-speed measurement equipment directly at the full conversion speed. As shown in Fig. 7, the measured DNL and INL show less than ±0.40 LSB and ±0.48 LSB at a 10-bit accuracy. Figs. 8(a) and (b) show the measured signal spectrum. The measured SNDR with a 10 MHz input sine wave at 100 MSample/s is 58 dB, and it drops by 6 dB at 120 MSample/s due to the increased noise level. However, the

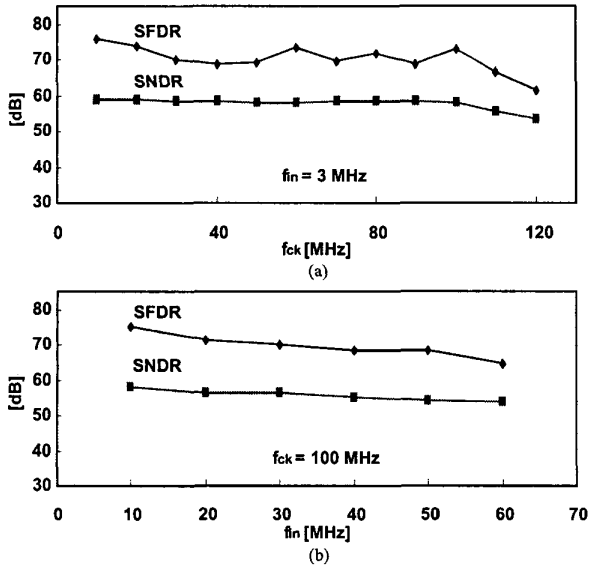

Fig. 9. Measured dynamic performance : (a) SNDR and SFDR vs. sampling frequency (b) SNDR and SFDR vs. input frequency.

ADC achieves the SFDR of 68 dB at 120 MSample/s. Figs. 9(a) and (b) show the dynamic performance of the prototype. At the increased sampling rate of 120 MHz and input frequency of 3 MHz, the measured SNDR demonstrates 53 dB. The multibit-per-stage architecture incorporating the MCS technique maintains SNDR over 54 dB and SFDR over 68 dB for signal frequencies up to Nyquist at a 100 MHz sampling rate. The measured results are summarized in Table 2.

Conclusion

A 10b 120 MSample/s pipelined CMOS ADC has been presented. The MCS technique in a multibit-per-stage pipelined architecture achieves high conversion speed and high SFDR, and a logic-based encoding scheme reduces power consumption and chip area for the encoders of flash ADCs. Another important advantage of this MCS technique is that the amount of metal lines routing, switches, and logic gates driving the affected capacitors is reduced by approximately 50 %. This results in reduced load and parasitic capacitance, lower coupling noise, less power, and less chip area. The measurement results demonstrate the effectiveness of the MCS technique for speed and accuracy in the context of the multibit-per-stage pipelined ADC implementation.

Table 2. Performance summary.

Resolution	10 bits
Max. Conversion Rate	120 MSample/s
Process	0.25 μm double-poly CMOS
Input Range	$2V_{P-P}$
SNDR (at 100 MS/s)	58.2 dB at f_{in} of 10 MHz 54.1 dB at f_{in} of 50 MHz
SFDR (at 100 MS/s)	75.3 dB at f_{in} of 10 MHz 68.4 dB at f_{in} of 50 MHz
DNL	± 0.40 LSB
INL	± 0.48 LSB
ADC Power	208 mW
Die Area	3.6 mm^2 (=1.8 × 2.0 mm^2)

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