An Adaptive PAM-4 5 Gb/s Backplane Transceiver in 0.25 um CMOS

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Abstract - This paper describes a novel backplane transceiver, which uses PAM-4 (pulse amplitude modulated four level) signalling and continuously adaptive transmit based equalization to move 5 Gcb/s (channel bits per second) across typical FR-4 backplanes for total distances of up to 50 inches through two sets of backplane connectors. The paper focuses on the implementation of the equalizer and the adaptation algorithms, and includes measured results. The 17 mm^2 device is implemented in a 0.25um CMOS process, operates on 2.5 V and 3.3 V supplies and consumes 1.2 W.

I. Introduction

The need to switch and route the increasing amounts of data traffic resulting from the recent explosion in Internet usage has made the backplane the critical bottleneck in networking infrastructure. Technical advances in optical links and supporting electronics have increased not only the speed of each port but also the total number of ports in a system. During this same time frame backplane materials and connectors have improved very little. Thus, the distortions arising from skin effect, dielectric losses and reflections, which are frequency-dependent, have become increasingly problematic as symbol rates have increased. The effects of these problems have been quantified and studies show that when the loss in the channel at the Nyquist rate is large, non-binary PAM signaling becomes attractive [3] and that at symbol rates at and above 2.5 gigabaud, substantial equalization is required to maintain signal integrity [1,2].

Thus to develop a 5 Gb/s backplane transceiver we were compelled to incorporate the evolutionary steps of multi-level signaling and transmit equalization. Our decision to make the equalizer self-adaptive stems from the following: First, consistent operation across a large variety of backplane lengths, materials, and connectors demands a rich set of possible equalizer settings, which makes the task of manually tuning the equalizer to optimum performance very difficult. Second, robust operation at a data rate of 5 Gb/s requires us to track and compensate for changes in environmental conditions (power supply, temperature, aging).

In the remainder of this paper we provide an overview of the architecture of our system, describe the operation of the adaptive equalizer, and finally, present a mix of simulated and measured results demonstrating the operation and effectiveness of our part across a variety of backplanes.

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II. Implementation

A. Transceiver Block Diagram

A block diagram of the transceiver is illustrated in figure 1.

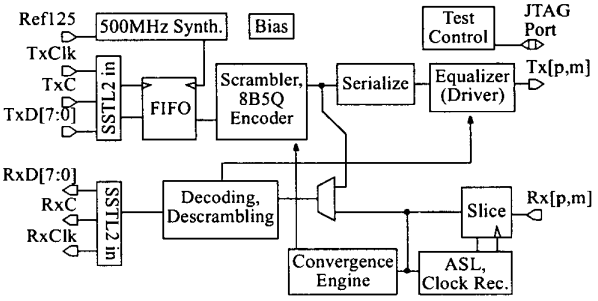

Fig. 1. Transceiver Block Diagram

B. The Transmit Equalizer Architecture

Figure 2 shows a block diagram of the equalizer; it consists of four current steering two-bit output DACs, which are summed to generate the equalized PAM-4 output waveform.

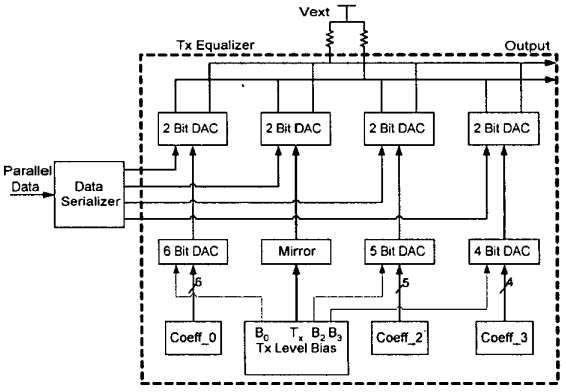

Fig. 2. Transmit Equalizer Architecture

The second of these DACs creates the signal associated with the main symbol. The first and third DACs produce drives that are weighted by coefficient values and proportional to the symbols that trail and precede the main symbol.

The fourth DAC provides a drive that is weighted by a coefficient and is proportional to a symbol, which may have a latency of 2 to 8 symbol intervals after the main symbol. The

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position for this tap is chosen to maximize the correlation between the delayed symbol and the residual intersymbol interference (ISI), thus canceling the greatest remaining error. This so called "rover" tap can be placed immediately after the trailing tap or it may be used to cancel out a significant echo that is farther from the main symbol.

The resulting structure is best thought of as a dynamically configurable, sparse, FIR equalizer. The value for each coefficient is realized by using an appropriately sized coefficient DAC, which controls the amount of current steered by the associated two-bit output DAC. The input to each coefficient DAC is controlled by a separate saturating counter, which accumulates adjustment commands issued by the receiver at the far-end of the channel.

C. The High Speed DACs

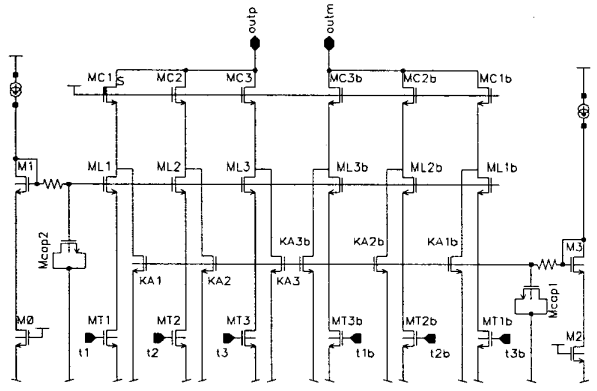

Fig. 3. One of 4 Two Bit DACs Used in Equalizer

Figure 3 shows a schematic view of one of the 2-bit driver DACs. The 2-bit (4 level) output is generated by differentially controlling three identical pairs of current drivers (columns). The three differential digital inputs are thermometer encoded prior to serialization and control the transistors named MT1, MT1b, MT2, MT2b, MT3, MT3b. The amount of current that an "on" column can sink (how the coefficient value is set for the DAC) is controlled by the bias applied to the transistors named ML*. The top transistor in each column, MC*, creates a cascode to isolate the ML* transistors. Finally, the transistors named KA* are present to sink a leakage current through the top cascode devices to keep them out of sub-threshold when their columns are "off".

D. The Adaptation Algorithm

The adaptation and equalization process is driven by a simple, but effective, sign-sign block LMS algorithm. The update equation for the digital representation of the k-th tap for block j is given by equation 1,

$$tap_k(j+1) = tap_k(j) + \mathrm{sign}\left(\sum_{i=0}^{L-1} \mathrm{sign}(e_{jL-i})\mathrm{sign}(d_{jL-i-k})\right) \quad (1)$$

where sign( ) is defined to be +1 if its argument is greater than or equal to 0, and -1 if its argument is less than 0, the subscripts on the error (e) and data (d) represent their position within the block, and L is the length of a block of data.

The tap update algorithm resides in the receiver where the quality of the signal can be directly measured. Once an update is completed the adjustments for the tap are communicated back to the far end transmitter where they are applied. The coefficients are continually updated, a feature which allows the equalizer to not only correct for the impairments of the packages, connectors and backplane traces, but also to track with power supply drift, component aging, and temperature variations. The adaptation overcomes the invariant nature of a fixed setting and thus optimal performance can be continuously maintained for the link. This is important given the stringent BER requirements demanded across the backplane. Finally, a block size of 5115 symbols was empirically determined to provide a good trade-off between tap noise and convergence speed.

E. The Convergence Engine

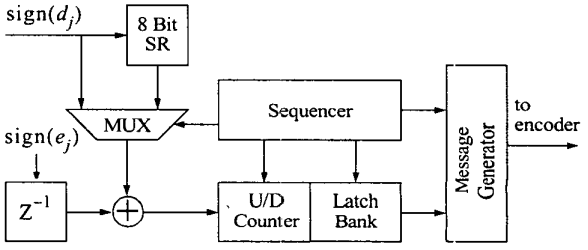

Fig. 4. Digital Round Robin Adaptation Engine

The block diagram of the convergence engine (CVE) responsible for the correlations is shown in Figure 4. It consists of three main parts: digital logic to implement equation 1, a tap sequencer, and a controller to generate the adjustment messages. The sequencer is a simple state machine that cycles the CVE through all tap locations, controls the summation period and latches the results. An 8-bit shift register and associated multiplexer are used to select the appropriate "sign of the data term" for each tap. A single flip-flop provides history for the "sign of error term" required to calculate the tap adjustment for the preceding symbol tap. When appropriately selected, these terms are effectively multiplied by XORing them together; the result is accumulated in an up/down counter. The sign of the result is, in turn, latched by the

sequencer where it is held until all tap adjustments have been determined and the adjustment message is generated.

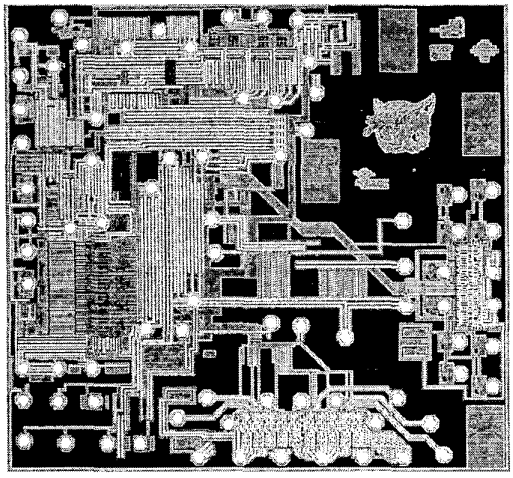

Fig. 5. Chip Microphotograph

III. Results

A. Simulated Results

Figure 6 shows overlays of equalized and non-equalized pulses as delivered to the receiver using 8 mil traces and total lengths of 13", 30", and 50".

These simulations are based on backplane channel responses measured as differential s-parameters on a real backplane made of FR-4 material. The simulator models the equalizer and convergence algorithm, including limitations such as finite tap weight range and resolution and finite transmit and receive bandwidths. The sampling times are marked on the lines. Note that near-zero ISI is achieved for all lengths, despite widely varying non-equalized pulse shapes. It is clear that without equalization the effects of dielectric loss and skin effect are pronounced and cause significant ISI.

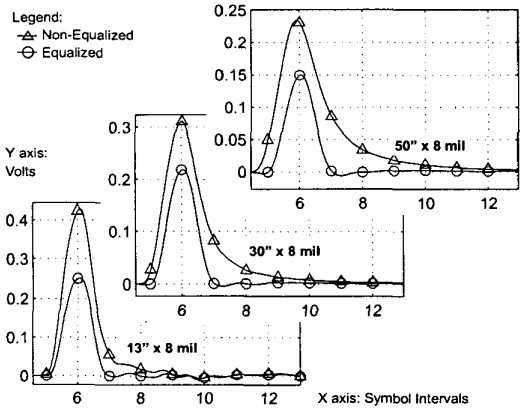

Fig. 6. Equalized and Non-Equalized Pulses

B. Measured Results

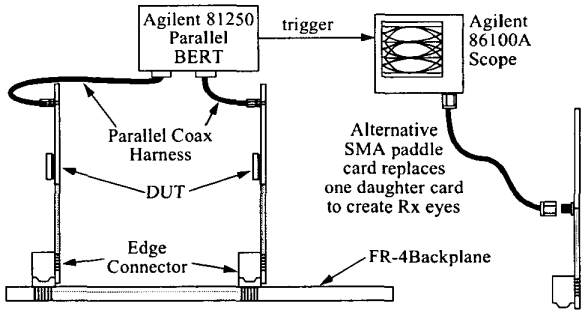

Fig. 7. Bench Test Setup

The bench test hardware is illustrated in figure 7. It includes an FR-4 backplane with 6 mil traces. The devices are each mounted onto daughter cards which are plugged into the backplane and connected with another 4" of 5.5 mil traces.

The parallel interface can be routed via a harness of coaxial cables to the parallel BERT for pattern generation and error rate monitoring. Alternatively, one of the cards may be replaced by a "paddle card" containing only an edge connector and SMA connectors. This allows the capture of eye diagrams as they would appear at the receiver.

Figures 8-11 show the received eye with and without equalization for backplane lengths of 12" and 26".

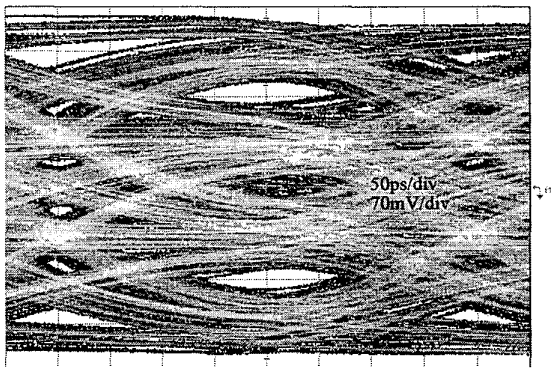

Fig. 8. Receive eye with 0.006" x 12" Backplane (20" total)

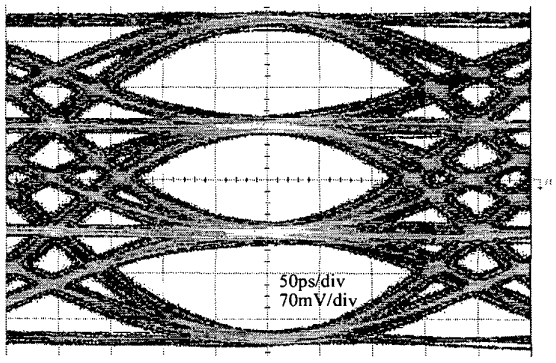

Fig. 9. Receive eye with 0.006" x 12" Backplane (20" total)

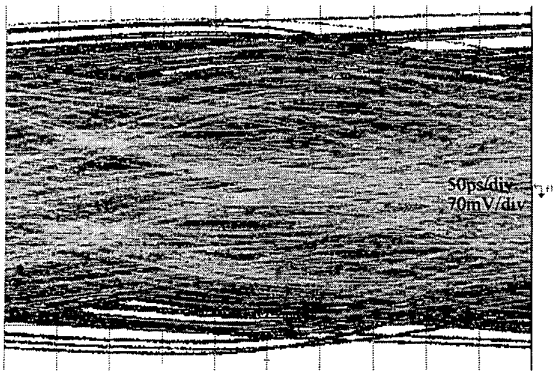

Fig. 10. Receive eye with 0.006" x 36" Backplane (44" total)

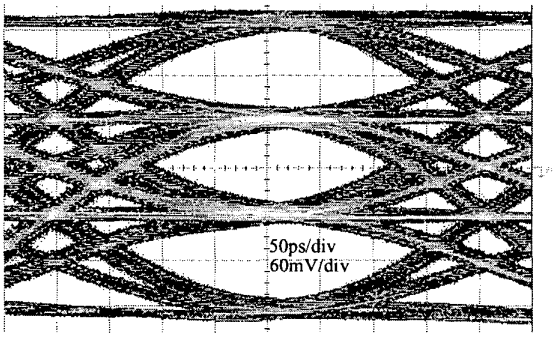

Fig. 11. Receive eye with 0.006" x 36" Backplane (44" total)

For a transceiver, BER is the most important performance criterion. We were unable to measure any errors in overnight measurements, thus, we were forced to develop a margining technique to study performance. The margining technique comprises adding a wideband error signal to the signal; this can be thought of as a simple model for crosstalk. In figures 12 and 13, the resulting BER is plotted as a function of the ratio of the pk-pk additive noise signal to pk-pk signal for both synchronous and asynchronous operation.

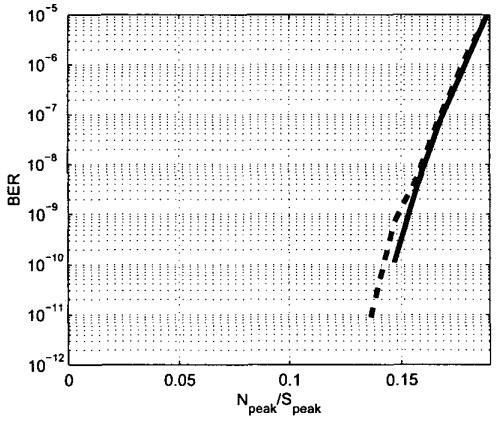

Fig. 12. BER vs NSR for 0.006" x 12" backplane (20" total). Solid = synchronous; Dashed = 200ppm frequency offset.

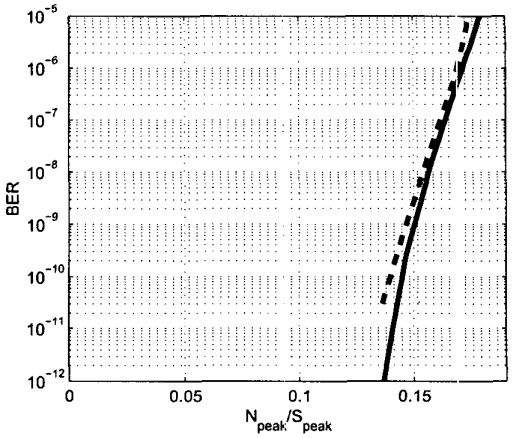

Fig. 13. BER vs NSR for 0.006" x 36" backplane (44" total). Solid = synchronous; Dashed = 200ppm frequency offset.

CONCLUSION

A novel 5 Gb/s transceiver designed for the backplane communications channel has been described. The use of transmit based self-adaptive equalization and PAM-4 signaling was shown to be an effective combination in compensating for the distortions that plaque backplane communications systems. Experimental results were presented, which demonstrate essentially error-free operation. The 17 mm^2 device is implemented in a 0.25 um CMOS process, operates on 2.5 V and 3.3 V supplies and consumes 1.2 W.

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[2] W. J. Dally, J. Poulton, "Transmitter Equalization for 4 Gb/s Signalling," *Proc. Hot Interconnects Symp.*, pp. 29-39, Aug. 1996.

[3] Dr. Howard Johnson, "Multi-Level Signalling," *DesignCon 2000*, Feb. 2000.