# A 1.8-V 67mW 10-bit 100MSPS Pipelined ADC using Time-Shifted CDS Technique

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*ABSTRACT*—A *time-shifted* correlated double sampling (CDS) technique is proposed in the design of a 10-bit 100MSPS pipelined ADC. This technique significantly reduces the finite opamp gain error without compromising the conversion speed, allowing the active opamp block to be replaced by a simple cascoded CMOS inverter. Both high speed and low power operation is demonstrated without compromising the accuracy requirement. An efficient common-mode voltage control is used in the pseudo-differential architecture to further reduced power consumption. Fabricated in a 0.18$\mu$m CMOS process, the prototype 10-bit pipeline ADC achieves 65dB SFDR and 54dB SNDR at 100MSPS. The total power consumption is 67mW at 1.8-V supply.

## I. Introduction

The pipelined ADC architecture has been adopted into many high-speed applications including high performance digital communication systems and high quality video systems [1][2]. The rapid growth in these application areas is driving the design of ADCs towards higher operating speed and lower power consumption. This trend poses great challenges to conventional pipelined ADC designs which rely on high-gain operational amplifiers to produce high-accuracy converters. Given the continuing trend of submicron CMOS scaling which is coupled with lower power supply voltages and the demand for increased clock speed, large open loop opamp gain is difficult to realize without sacrificing bandwidth. As a result, the finite opamp gain is becoming a major hurdle in achieving both high speed and high resolution. To address this issue, we present in this paper a *time-shifted* correlated double sampling (CDS) technique [3]. The proposed technique is highly effective for finite opamp gain compensation in the context of low-voltage and high-speed pipelined ADCs. Due to this effective gain compensation, the time-shifted CDS technique has enabled a successful implementation of a low power and high-speed pipelined ADC that uses simple cascoded CMOS inverters in place of traditional operational amplifiers.

## II. Time-Shifted CDS Technique

One of the simplest implementations of pipelined ADCs incorporating digital correction/redundancy is based on the 1.5-bit-per-stage architecture. This architecture is widely used to maximize the conversion speed. Figure 1 shows a typical multiplying digital-to-analog converter (MDAC) structure used in this type of pipeline ADC architecture. The output of

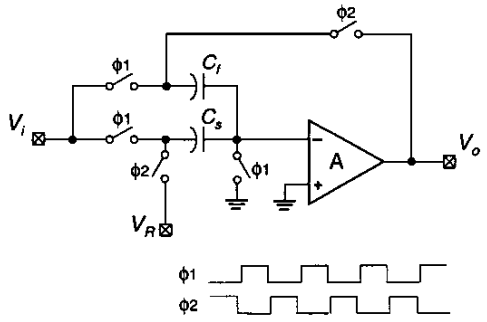


**Fig. 1.** Typical 1.5-bit-per-stage MDAC.

this MDAC at the end of the amplification phase ($\phi_2$) is

$$V_o = \left(\frac{C_s + C_f}{C_f}\right) \cdot V_i - \left(\frac{C_s}{C_f}\right) \cdot V_R + e, \qquad (1)$$

where $V_i$ is the sampled input ($\phi_1$), $V_R$ is $\pm V_{ref}, 0$ that depends on the result of the sub-ADC conversion of the sampled input, and the error resulting from the finite opamp gain is

$$e = \frac{-1}{A}\left(1 + \frac{C_s}{C_f}\right) \cdot V_o. \qquad (2)$$

This error $e$ is inversely proportional to the opamp gain $A$, directly deteriorating the overall linearity of the ADC.

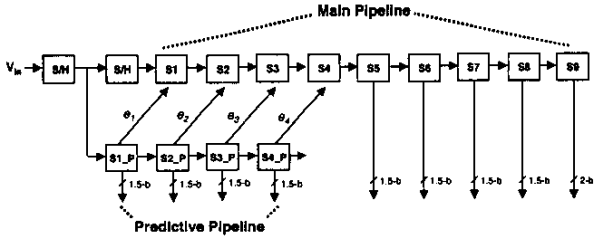


**Fig. 2.** Proposed pipelined ADC architecture.

Figure 2 illustrates the proposed pipelined ADC architecture employing the time-shifted CDS technique. This architecture realizes two pipelined paths working in parallel for

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the first few stages. One path represents the *predictive* path which only operates for the first four stages, and the other path represents the main signal path which operates for all nine stages necessary for the 10-bit conversion. The first four stages of the main signal path are very similar to their corresponding stages in the predictive path, and they share the same set of active stages (opamps/inverters and comparators). Both signal paths (main and predictive) process the same input signal from the first sample-and-hold (S/H) stage, but the main signal path is delayed a half clock cycle (one phase) by an additional S/H (shares the same opamp/inverter) following the first S/H. The input signal is first processed by the predictive pipeline and the finite opamp gain error is stored on a capacitor. The stored error is used to correct the corresponding stage in the main pipeline in the following clock phase (half clock cycle delay). As both signal paths (predictive and main) share the same opamp/inverter, this operation is easily achieved with added switches and capacitors.

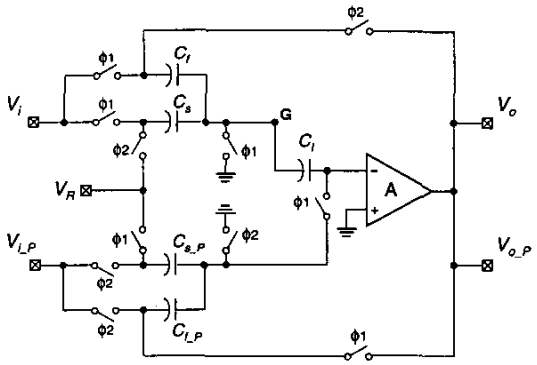


**Fig. 3.** Proposed MDAC structure.

The switched-capacitor implementation of this MDAC operation merging both the predictive pipeline and the main pipeline is shown in Fig. 3. $V_i$ and $V_o$ are the input/output of the main pipeline, whereas $V_{i\_P}$ and $V_{o\_P}$ are the input/output of the corresponding predictive pipeline. The capacitors are chosen such that $C_{s\_P} = C_{f\_P} = C_s = C_f$. In the proposed time-shifted CDS scheme, the sampling and amplifying operation is actually performed twice. The initial/first operation is done by $C_{s\_P}$ and $C_{f\_P}$, and the non-zero error voltage due to finite opamp gain at the negative input of opamp is stored in $C_I$. The following/second operation is done by $C_s$ and $C_f$, with $C_I$ connected between the negative input of opamp and the common node of $C_s$ and $C_f$ (node G). An accurate virtual ground is created at node G. While the operation of this time-shifted CDS technique appear similar to conventional CDS techniques [4][5], it performs without the additional capacitive load to the opamp and/or the extra clock phase(s) to the ADC operation. Any possible speed penalty due to CDS operation is completed avoided, which is critical in achieving the low-power and high-speed ADC performance.

Some design considerations of the proposed architecture are in the following. First, because the inputs of MDAC are not the same for the predictive path and the main path (with the exception of the very first MDAC), the effect of error correction will not be as good as the conventional CDS techniques (e.g. [4]). The output error at stage $i$ in the main pipeline is approximately by

$$e_i \approx \frac{-i}{A^2}(1+\frac{C_s}{C_f})\left[(1+\frac{Cs+C_I}{C_f})\cdot V_{oi}(n) - (\frac{C_I}{C_f})\cdot V_{oi}(n-1/2)\right], \quad (3)$$

where $V_{oi}(n)$ is the current output in the main pipeline, and $V_{oi}(n-1/2)$ is the output of previous clock phase (predictive pipeline). Note that the error is inversely proportional to $A^2$. However, this error will increase from stage to stage down the pipeline. This is because the discrepancy between the outputs of the predictive path and the main path will become larger from stage to stage down the pipeline. The second design issue is that the time-shifted CDS will add extra offset to sub-ADCs in the main pipeline. The reason is that the MDACs in the main pipeline need to use the digital code generated by the sub-ADCs in the predictive pipeline. This is equivalent to putting a signal-dependent offset to the sub-ADCs in the main pipeline. Fortunately, digital redundancy of the pipelined ADC is able to correct for the offset, whether signal-dependent or not, as long as the amount of the offset is within the correctable range ($\pm\ V_{ref}/4$ for 1.5-bit-per-stage MDAC).

## III. Circuit Design

### *A. CMOS Inverter*

Opamp is the most critical building block in pipeline ADCs. The opamp dc gain and bandwidth determine the achievable accuracy and conversion rate. For a 10-bit pipeline ADC, open-loop opamp gain needs to be well over 60dB. It is not uncommon to see 80dB gain in practical design examples. To design such high gain opamp at low supply voltage is quite challenging because traditional stacking of cascode transistors are not feasible. Use of compensated multi-stage opamps will lead to a considerably increased power consumption and reduced speed. In the prototype IC implementation, we used simple cascoded (both the NMOS input and PMOS current source) CMOS inverters. Replacing opamps with these inverters allowed wide swing, large bandwidth, and low power consumption. Simulation results have indicated approximately 46dB open-loop dc gain in the 0.18$\mu$m CMOS process. This level of dc gain is insufficient for a 10-bit accuracy pipeline ADC, but we are able to tolerate the low dc gain due to the enhancements achieved from the time-shifted CDS technique described in the above.

### *B. Pseudo-differential MDAC*

The use of inverters in place of opamps imply inherently single-ended design. We have adopted pseudo-differential configuration throughout the pipelined ADC design. In other words, two single-ended MDACs in parallel are used to build a pseudo-differential MDAC. As in fully differential circuits,

all pseudo-differential structures require some sort of equivalent common-mode feedback (CMFB) operation. Without the equivalent CMFB function, any common-mode error in the pipeline would be amplified just the same way the differential input signal is amplified (residue amplification). This can cause single-ended opamps (inverters) to saturate down the pipeline. Without implementing a traditional CMFB with large amount of overhead, a new pseudo-differential MDAC that uses differential *float* sampling scheme is proposed. This is shown in Fig. 4 (time-shifted CDS not shown for simplicity). The differential gain of this MDAC is still two but the common-mode gain is just one due to one of the input capacitor pairs ($C_2$ and $C_3$) that is differentially sampled without a specific common-mode reference (thus floating). This equivalent CMFB operation is achieved with no speed penalty.

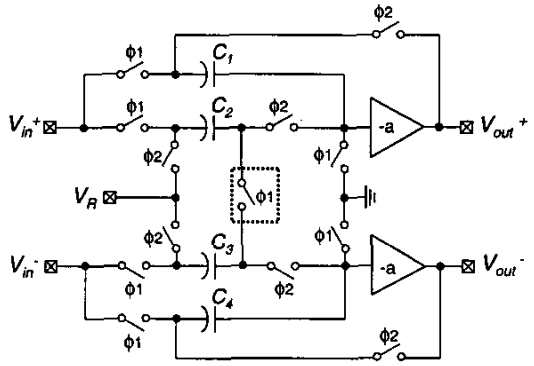


**Fig. 4.** Proposed pseudo-differential MDAC.

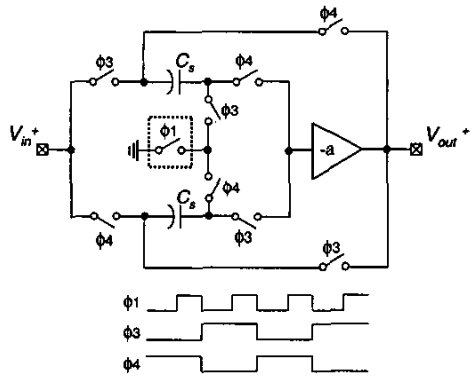


**Fig. 5.** Timing-skew insensitive double-sampling S/H.

*C. Double Sampling S/H stage*

The proposed architecture shown in Fig. 2 indicates that two S/H blocks are needed to apply the time-shifted CDS technique. To minimize power consumption and kT/C noise, a timing skew insensitive double sampling S/H circuit [6] shown in Fig. 5 (single-ended illustrated for simplicity) is employed. There are two sets of sampling switches and capacitors for this time-interleaved operation, and they operate at half the speed of the overall ADC. So the output the this S/H circuit will provide a sampled output (hold operation) for the two sampling phases of the first stage pipeline employing the time-shifted CDS. This double sampling S/H circuit is insensitive to the timing skew due to the series master sampling switch [6]. The opamp offset and gain (memory) mismatches are manageable at the 10-bit level. Any capacitor mismatches are alleviated due to inherently voltage-mode operation (i.e. sampled input voltage is "flipped" to the output).

## IV. Measurement Results

The prototype ADC was fabricated in a 0.18$\mu$m CMOS process. The die photograph is shown in Fig. 6 where the active die area is 1.2mm×2.1mm. The total power consumption is 67mW at 1.8-V supply and 100MHz sampling frequency. Analog portion consumes 45mW. The measured DNL and INL are 0.8LSB and 1.6LSB as shown in Fig. 7. With

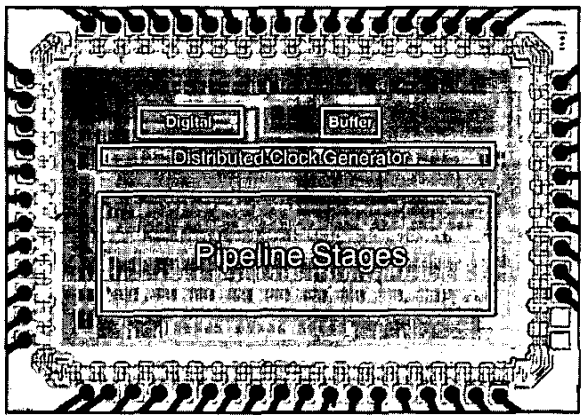


**Fig. 6.** Die photograph of the prototype ADC.

| | |
|---|---|
| Resolution | 10-bit |
| Sampling Rate | 100MSPS |
| Technology | 0.18$\mu$m CMOS |
| Supply Voltage | 1.8V |
| Power Consumption | 67mW |
| DNL/INL | 0.8LSB / 1.6LSB |
| SNR/SNDR/SFDR | 55dB / 54dB / 65dB |
| Die Area | 1.2mm×2.1mm |

**Table 1.** Performance summary.

1MHz input and 100MSPS, the measured SFDR, SNR, and SNDR are 65dB, 55dB, and 54dB, respectively. Figure 8 shows a typical measured frequency spectrum at 1MHz input and 100MSPS (the digital output of the ADC is decimated/down-sampled by four on chip for testing purposes). Figure 9 shows the dynamic performance versus input frequency at 100MSPS. The measured SFDR, SNR, and SNDR at the 99MHz input frequency are 63dB, 52dB, and 51dB. Figure 10 shows the

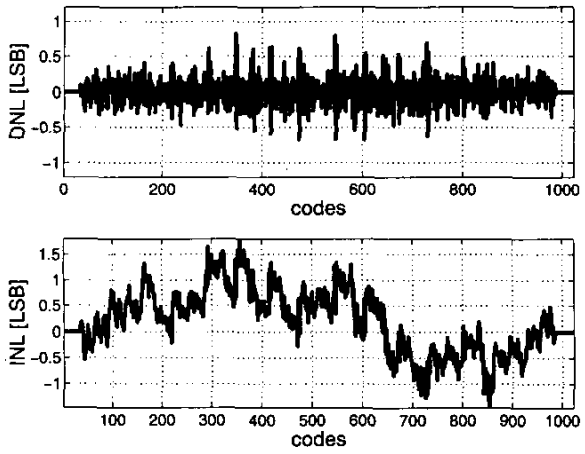


Fig. 7. Measured DNL and INL.

dynamic performance versus conversion/clock rate. The performance degrades past 100MSPS. The measurement results are summarized in Table 1.

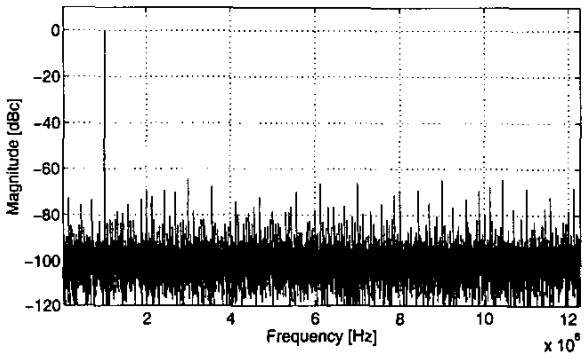


Fig. 8. Measured ADC output spectrum at 100MSPS.

## V. Conclusions

A *time-shifted* CDS technique which compensates for the finite amplifier gain of inverter-based pipelined ADC is described. The proposed technique enables low-power high-speed operation by allowing significantly reduced amplifier gain without the added overhead of increased power dissipation or extra clock phase(s). Prototype IC measurements demonstrate 67mW 10-bit 100MSPS performance. The achieved results indicate that a design incorporating effective CDS techniques (e.g. time-shifted CDS) in combination with simplistic active stages (e.g. inverter) can achieve significant speed improvement while maintaining, or even lowering, the overall power consumption.

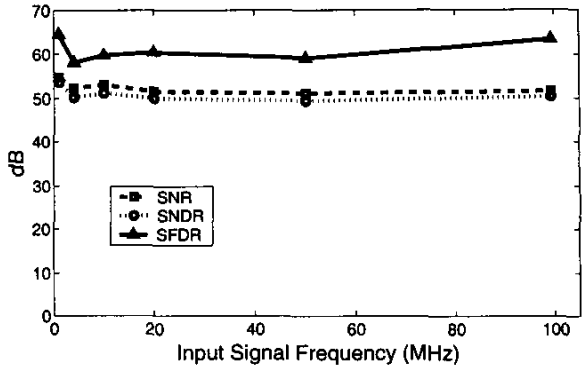


Fig. 9. Dynamic measurements vs. input frequency.

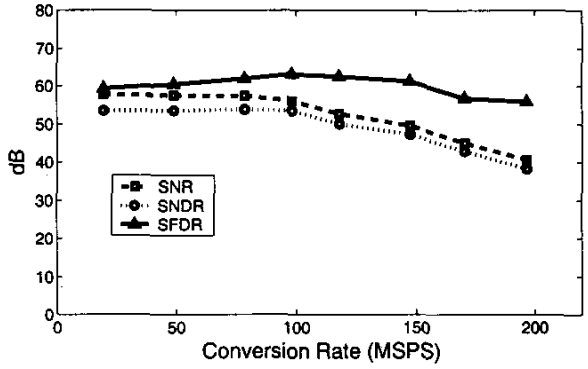


Fig. 10. Dynamic measurements vs. conversion rate.

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