Experimental Verification of a Correlation-Based Correction Algorithm for Multi-Bit Delta-Sigma ADCs

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Abstract

A multi-chip system was built to provide experimental verification of a correlation-based digital algorithm, which acquires and corrects all element errors in the internal DAC of a multi-bit delta-sigma ADC. The proposed correction method does not rely on noise shaping, and hence it remains fully effective even for very low oversampling ratios (OSRs). Measured results obtained for OSR = 4 confirmed that a 12 dB SNDR improvement can be achieved using such digital correction, while only 1~2 dB with the commonly used mismatch-shaping technique.

I. Introduction

For high-accuracy delta-sigma ADCs, it is usually necessary to use multi-bit internal quantizers. Then, the linearity of the internal DAC becomes a major limitation on the performance: for usual errors (0.1~0.5 %), the peak SNDR is restricted to about 60~65 dB. Using mismatch shaping (1)-(4), for high oversampling ratios (say, for OSR > 16) the DAC error signal can be adequately suppressed in the signal band. However, for wideband applications, a high OSR requires impractically fast opamps, and hence should be avoided. For low OSR, mismatch shaping becomes ineffective.

In (5), we proposed a fully digital correction method which acquires a digital estimate of the DAC mismatch error from the overall ADC output and the DAC input sequences, after both signals were digitally preprocessed. The error can then be removed from the ADC output. This technique can be used even for very low OSR values, and hence it is applicable to wideband signals.

In this paper, the first implementation of a multi-bit delta sigma ADC exploiting this technique will be reported.

II. The correlation-based error correction technique

The block diagram of the ADC is shown in Fig.1. It is a cascade of two stages. The first stage is a second-order delta sigma loop with a 3-bit quantizer Q1 and a 3-bit internal DAC. The second stage is a 10-bit quantizer Q2, whose input is the quantization noise of Q1 amplified by an inter-stage gain of 4, which is directly obtained from the internal node A (6). The outputs of the two stages are entered into the error cancellation logic (ECL) which delivers the ADC output. In the output, the quantization noise of Q1 is cancelled and the smaller quantization noise of Q2 is shaped with a second-order noise transfer function (NTF). However, the DAC error is not shaped by the loop when appearing in the ADC output, so this error directly limits the overall performance. We assume the usual DAC structure built from unit elements, which is also used in our design. The input **b**(k) to the DAC is thermometer coded , and contains the same number of bits as the number of the unit elements. They are called the selecting sequences. Its *i*th bit $b_i(k)$ turns on or off the *i*th unit element. For this structure, the DAC output is the sum of the outputs of all unit elements, and the DAC error is the sum of all unit element errors. A simple derivation leads to the following conclusions. A nonzero average of the unit element errors introduces a DC offset and a gain error into the ADC output signal. These are usually not important in communication applications. However, the nonzero variance of the unit element errors adds a nonlinear mismatch error to the DAC output (and to the ADC output), as shown in Fig.2. This error limits the linearity of the ADC performance, and it is the target of the digital correction technique.

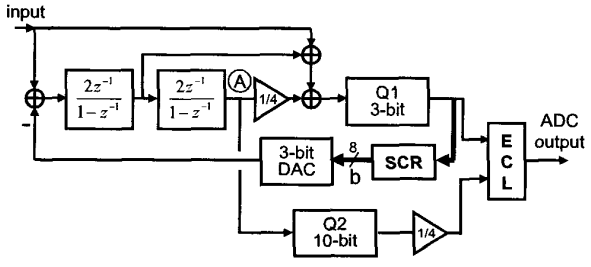

Fig.1 Block diagram of experimental cascaded multi-bit delta-sigma ADC.

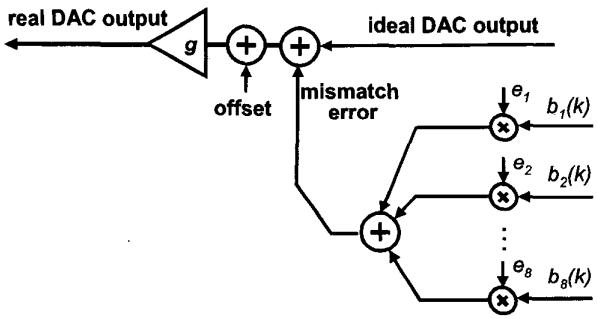

Fig. 2 A model for three effects of the DAC error.

The deviation e_i of each element error from the average error will determine the mismatch error of the DAC. This is the sum of all error constants e_i (i=1, 2,... 8), modulated by the corresponding selecting sequences, as shown in Fig.2. In the proposed error correction method, a digital correlation operation CORR is performed between the selecting sequences and the ADC output to extract the error constants e_i. From the extracted e_i, which are stored in the RAM, the mismatch error can be recovered (since the selecting sequences are known) and subtracted from the ADC output, as shown in Fig.3.

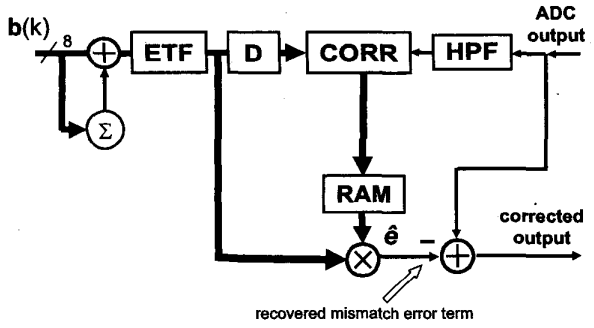

Fig. 3 System for estimation and correction of mismatch error.

Since the mismatch error of the DAC is shaped by a (known) error transfer function (ETF) when it appears in the ADC output, a digital block implementing the same transfer function is inserted to match the paths of the selecting sequences and the ADC output signal for CORR and the recovery of the mismatch error.

Unfortunately, the ADC output contains also components other than the DAC error: the input signal and the quantization noise of Q2. In the correlation process, these are interference signals. Only if they are uncorrelated with the selecting sequences can the correlation converge accurately to give the error constants. To achieve this condition, two additional operations are needed. First, a digital scrambler SCR, which rearranges the bits of the DAC input **b**(k) randomly in every clock period, is embedded between Q1 and the DAC, as shown in Fig.1. This process is similar to that performed in dynamic element matching, but the purpose here is to decorrelate **b**(k) from the interferences. Second, in every clock period, the mean value of all bits of the current **b**(k), which is scaled version of the ADC output, is subtracted from each selecting sequence before the correlation is performed, as shown in Fig.3. Even though as a result of these operations the interferences are less correlated with the selecting sequences, and the correlation will be converging to an accurate estimate of the errors, the speed of convergence is unsatisfactory. Simulations showed that the convergence is especially slow when the input signal, which is an interference, has a large amplitude. To overcome this problem, a high-pass filter HPF is used to reduce the input signal in the ADC output before carrying out the correlation. This accelerates the convergence. Correspondingly, a delay block D is placed between ETF and CORR to synchronize the selecting sequences with the filtered ADC output.

III. Implementation of the experimental ADC

To verify the effectiveness of the digital correction algorithm, the 2-0 cascade multi-bit delta-sigma ADC of Fig.1 was implemented in integrated form. In order to have a flexible realization which can be used to test various versions of the correction technique, a multi-chip system was built, as shown in Fig.4. The first stage, except for the SCR block, was designed and fabricated in the 1.6 μm CMOS process of AMI Semiconductor. The die photo of this chip is shown in Fig. 5. The second stage used a commercial chip from Analog Devices (AD9221). The SCR was implemented with the butterfly structure using commercial electronic switch chips (74LS157). The gain block following Q2, the ECL, and other blocks of the digital correction system were all realized in software off-line by a MATLAB program.

The structure used the digital correction technique described in (7) for the correction of the mismatch error occurring in the quantization noise cancellation inherent in cascaded delta-sigma structures.

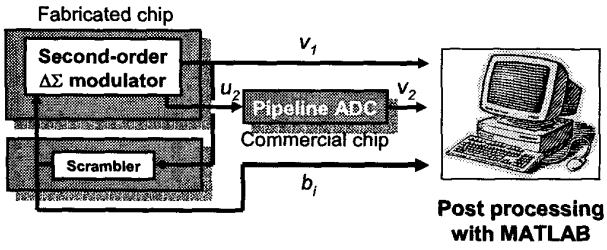

Fig. 4 Multi-chip system for implementing the correction algorithm.

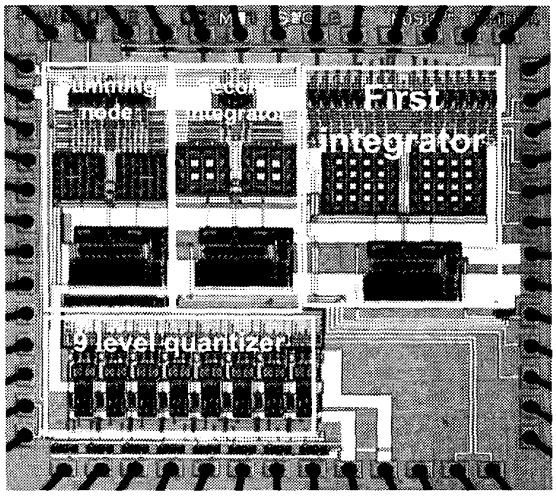

Fig. 5 Die photo of the fabricated chip.

IV. Experimental results

The ADC was tested with a clock frequency of 100 kHz, and a 1 kHz sine-wave signal at -6 dBFS. 60,000 data points were collected, and used in the correlation operation to obtain the digital estimate of the mismatch errors used for the correction. Fig.6 shows the measured in-band spectrum of the ADC output without the digital correction, but with scrambled **b**(k), for an OSR=4. The in-band SNDR was 60.3 dB, which corresponds to an RMS mismatch error of about 0.5%.

Fig.7 shows the output spectrum measured when first-order mismatch shaping, implemented with a butterfly structure (8), was used. This lowered the in-band noise floor, especially at low frequencies, but it also introduced tones, and it improved the SNDR only slightly, to 61.6 dB.

The measured output spectrum of the digitally corrected architecture is shown in Fig.8. The noise floor was now lowered at all in-band frequencies, and the SNDR improved significantly, by over 11 dB, to 71.8 dB.

Additional measurements were carried out with different amplitudes of the input signal. Fig.9 illustrates the results. For input amplitudes below -2.5 dBFS, the SNDR results for the correlation-based correction technique were better by about 12 dB than those for the first-order mismatch error shaping.

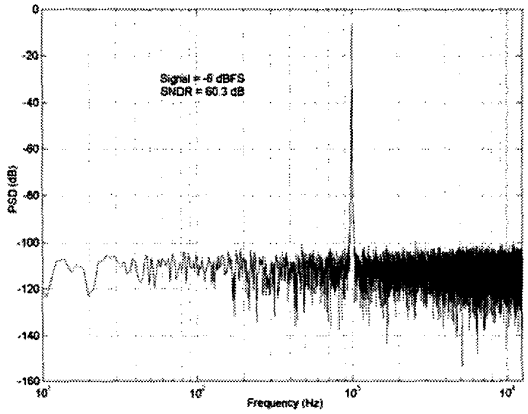

Fig. 6 Measured output spectrum without digital correction.

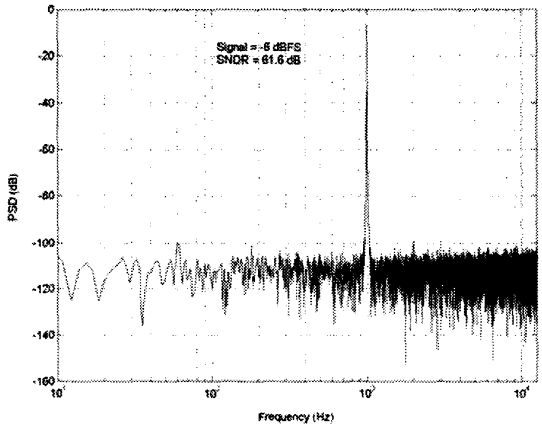

Fig. 7 Measured output spectrum with 1st-order mismatch shaping.

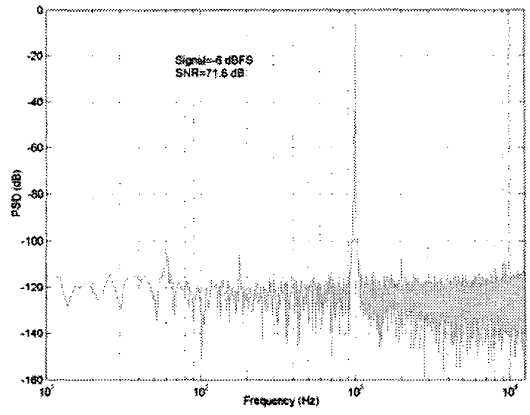

Fig. 8 Measured output spectrum with the proposed digital correction.

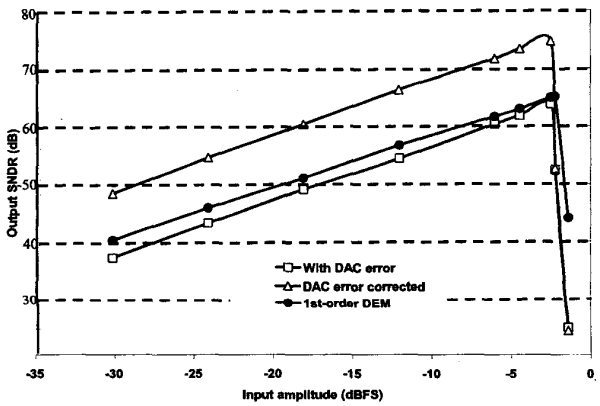

Fig. 9 SNDR vs. input signal amplitudes.

Conclusions

An experimental multi-bit delta sigma ADC was built to verify the effectiveness of the correlation-based DAC error correction algorithm proposed by us earlier (5). The ADC used a fully digital technique for the estimation and correction of the mismatch error of the internal DAC. The measured results verified that the technique works well in an integrated realization, and that for low OSR values it is vastly superior to mismatch error shaping techniques.

Acknowledgements

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