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A 0.8V Accurately-Tuned Continuous-Time Filter

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Abstract

An accurately tunable, low-voltage, linear continuous-time filter is presented in this paper. The system, designed using 0.18μm CMOS process, occupies 0.4mm^2 of area. The filter part of the circuit dissipates 2.6mW and the tuning part of the circuit dissipates 2mW of power. The filter achieves good tuning accuracy. The THD of the filter for a 10-kHz, 250-mVpp signal at 0.8-V supply voltage is 0.01%.

1. Introduction

One of the most critical issues in practical continuous-time (CT) filter applications is the corner frequency variation due to variations in process, temperature and voltage (PVT). The corner frequency is set by the absolute value of the RC time constant. However, both resistor and capacitor values can vary by as much as 25% in modern day CMOS technologies. This would result in a prohibitively wide variation of the corner frequency of the filter. Unlike CT filters, in switched capacitor (SC) filters the corner frequency is set by capacitor ratios and can therefore provide accurate corner frequencies. However due to their inherent sampled nature, input anti-aliasing and output smoothing filters are required. Moreover with aggressive supply scaling in modern CMOS processes, SC filters suffer from limited head room issues mainly due to the requirement of floating switches.

Due to these issues with SC filters, we focus on overcoming the corner frequency variation and low voltage issues in CT filters. We propose a tuning technique to accurately set the corner frequency while operating with high linearity at sub-1V supply voltage.

The next section describes various tuning techniques and highlights the basic mismatch problem in one of the widely used tuning techniques. Low-voltage CT filter design issues are also briefly summarized. The proposed tuning technique to compensate for corner frequency variation is presented in Section 3. Circuit design of the complete system is presented in Section 4. Section 5 presents experimental results of the fabricated chip.

2. Linear and tunable low-voltage continuous-time filters

Many tuning techniques have been proposed to compensate for the corner frequency variation [1]-[9]. These techniques can be broadly classified into two categories—direct tuning and indirect tuning. Direct tuning is performed by observing the filter's output and correcting for the corner frequency error. This method requires disrupting the normal filter operation during the tuning process and is therefore also referred to as foreground method. However due to the direct measurement of the corner frequency error, this method has the benefit of extremely accurate tuning. In the case of indirect tuning the corner frequency error is measured indirectly without disrupting the normal filter operation and therefore tuning can be performed in the background. Of the existing indirect tuning methods, the master-slave tuning technique is the most popular one. In this scheme, the corner frequency of the slave filter is set by the master filter whose corner frequency in turn is typically set by a PVT invariant element. For example, in [7] and [4] a switched capacitor resistor is used as the reference element. Ideally, the PVT variations in the slave filter are annulled by the PVT invariant master filter. However, in practice the accuracy of the tuning is limited by the mismatch between the master and the slave. Therefore, accurate tuning of CT filters using master-slave approach requires precise matching of master and slave components. In this work we combine the advantages of both the direct and indirect tuning methods.

The filter is continuously tuned using master-slave approach, while the mismatch between the master and slave is cancelled by the direct measurement of the error during power-up.

Linearity of CT filters is an important requirement in many modern day applications. The most popular tunable filters are the MOSFET-C filters because of their simplicity. The overall linearity of these filters is limited by the linearity of the MOSFET itself (typically 40-60dB). The linearity of MOSFET-C filters can be improved by using R-MOSFET-C technique as proposed in [4] (Figure 1). However, low-voltage tuning of CT filters poses formidable design challenges. For example, MOSFET-C filter is tuned by varying its gate voltage V_G and therefore varying the ON resistance. For the MOSFET to be operational, $V_{GSMIN} \geq V_{TH}$ and to prevent gate oxide stress related reliability issues $V_{GSMAX} \leq V_{DD}$. So V_G can only be varied between V_{TH} and V_{DD} which implies a very small tuning range. This problem can be circumvented, as illustrated in Figure 2, by using thick oxide devices that are readily available in most sub-micron technologies. Since these transistors are used as resistors, using thick-oxide devices does not levy any speed penalty on the overall filter.

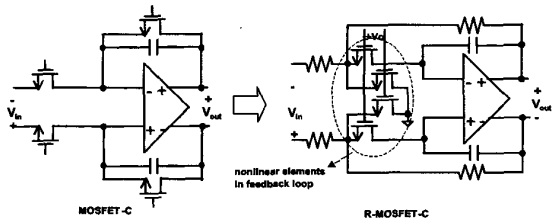

Figure 1 RC to R-MOSFET-C conversion.

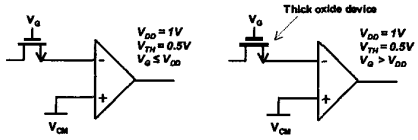

Figure 2 Use of thick oxide devices to allow greater V_{GS}.

3. Mismatch minimization scheme

The system level block diagram of the proposed mismatch minimization scheme is shown in Figure 3. On power up switches S_1 and S_2 are turned ON while S_3 is turned OFF. A digitally synthesized sine wave of desired frequency (typically the -3dB frequency of the filter) is applied to the slave filter. The output of the filter is used to detect and correct for the mismatch between the master and the slave. The filter is switched back to its normal mode of operation after the mismatch is suppressed within the required accuracy.

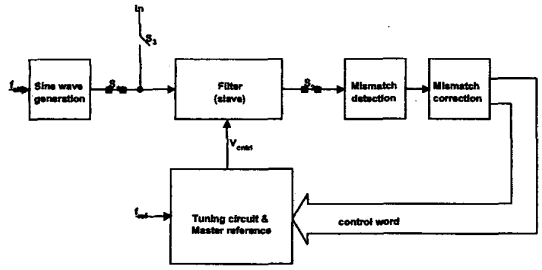

Figure 3 Block diagram of mismatch minimization system.

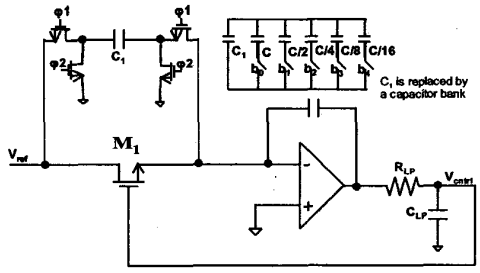

Figure 4 Switched capacitor based tuning.

A switched capacitor tuning scheme in conjunction with a linearity enhanced R-MOSFET-C filter is adopted in this work and is shown in Figure 4. It consists of a switched capacitor resistor where the capacitor C_1 and f_{clk} sets the reference resistance value and M_1 is the replica of the resistor in the slave. The tuning loop sets the control voltage (V_{cntrl}) so that the ON resistance of M_1 matches the reference switched capacitor resistance. Even though it has been shown that this scheme tracks PVT variations, the accuracy of the corner frequency is limited by the absolute accuracy of the capacitor C_1 to capacitors in the filter/slave. In this work, capacitor C_1 is self-calibrated during power up, therefore alleviating the absolute accuracy requirement. In order to perform this calibration, capacitor C_1 is replaced by a capacitor bank as shown in Figure 4, and the calibration is done as follows. A digitally synthesized sine wave is applied to the filter and the peak filter output (-3dB value) is determined and compared with the ideal -3dB peak. The output of this comparison determines whether the mismatch is positive or negative, thereby enabling the mismatch correction block to increase or decrease the capacitance value in the switched capacitor resistor. This system is designed to accommodate for ± 10% mismatch between the master and the slave. Once the mismatch minimization is done, the control word is frozen so that the effective capacitance of the reference switched capacitor is changed to accommodate for the mismatch between the master and the slave.

4. Prototype system implementation

4.1. Filter and Tuning

To verify the concept of mismatch minimization on power up to tune the filter accurately, a simple low-pass Butterworth biquad is implemented. The corner frequency of the filter is chosen to be 115 kHz and the power supply for the filter part is under 1V. Since the proof-of-concept-prototype is designed in a 1.8V process, the tuning circuit uses 1.8V supply. However, as mentioned earlier, thick oxide devices can be used in true sub-1V processes. The implementation of the R-MOSFET-C version of the biquad is shown in Figure 5.

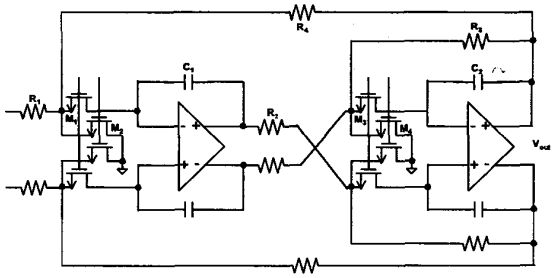

Figure 5 Differential R-MOSFET-C version of the biquad.

A high gain two stage operational amplifier was chosen so that the first stage provides the high gain and the second

stage provides high output swing to maximize the dynamic range. High gain of the opamp is required to improve the linearity of the filter significantly [5]. Automatic tuning employed in [4] is used in this system.

4.2. Sine-wave generation

The sine wave required to perform mismatch minimization is generated as shown in Figure 6. The sine-wave is synthesized using a digital state machine and a non-linear digital to analog converter (DAC). The state machine generates the control word and the current mode DAC converts the digital word to the corresponding analog value. The current sources in the DAC are scaled non-linearly to accommodate non-uniform step size required to generate the sine wave without indulging in a large number of current sources.

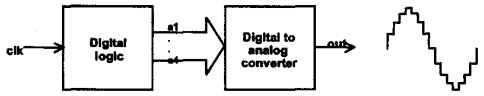

Figure 6 Block diagram of sine-wave generation.

4.3. Mismatch Detection and Correction

Mismatch detection and correction scheme is shown in Figure 7 and is done as follows. The peak filter output is detected by a peak detector and is compared with the ideal peak voltage. The error signal indicates the mismatch between the master and the slave i.e., if the filter's (slave) equivalent resistance is greater then or less than the switched capacitor resistance (master). This error signal is fed to the counter, which is used to switch-in and switch-out the capacitance in the switched capacitor resistor.

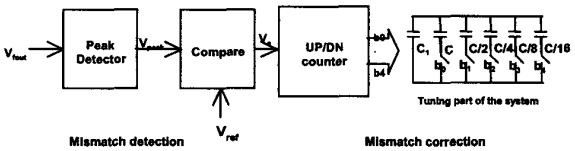

Figure 7 Mismatch detection and correction.

A differential peak detector is employed to minimize the errors due to common mode variations in the differential reference voltage.

5. Experimental Results

A 115 kHz -3dB frequency, 2nd order low pass filter was designed in 0.18μ CMOS technology. The filter is tuned accurately by using the proposed mismatch minimization scheme. This section presents measurement results of the fabricated chip.

Figure 8 shows the measured output spectrum for a 10 kHz, 250mVpp input signal for the filter. It can be seen from the figure that the filter has -80dB THD for a 10 kHz, 250mVpp input signal with a power supply of 0.8V. Signal to Noise Ratio for a 250mVpp 10 kHz input signal is 56dB. The overall SNR is lower than expected mainly due to the unaccounted flicker (1/f) noise of the opamp, which is reinforced by the -10-dB/dec slope of the noise floor at lower frequencies. The measured SNR without flicker noise is about 84dB. Figure 9 shows THD vs. input frequency. The THD degradation at high frequencies is mainly due to the fact that the loop gain decreases as the bandwidth of the filter is approached which results in less suppression of the non-linearities due to the MOSFET resistors used in the filter.

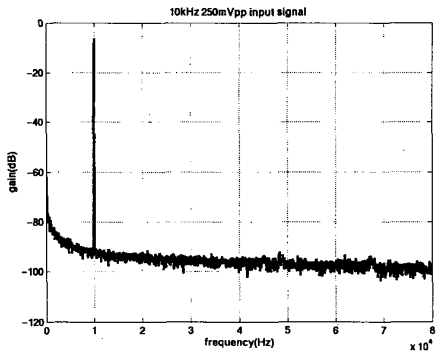

Figure 8 Measured output spectrum of a 10 kHz 250mVpp input signal.

Measurement results demonstrating the power-up tuning for the system are presented in this section. Figure 10 and Figure 11 shows the measured frequency response of 3 chips with the power-up mismatch minimization scheme turned off and turned on respectively. It is clear that the filter is tuned to an accurate corner frequency (115 kHz) when the power-up mismatch minimization scheme is ON. The results for only 3 parts are provided because the fabricated chip has a problem with the tuning loop becoming unstable in some parts. Die photo is shown in Figure 12.

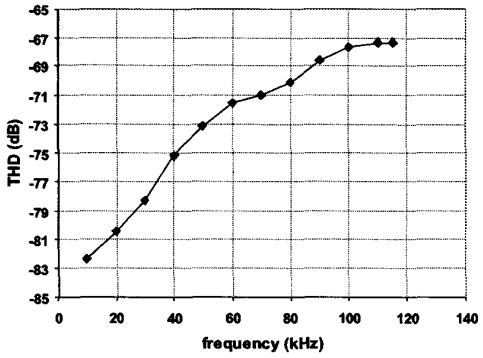

Figure 9 THD Vs Input frequency.

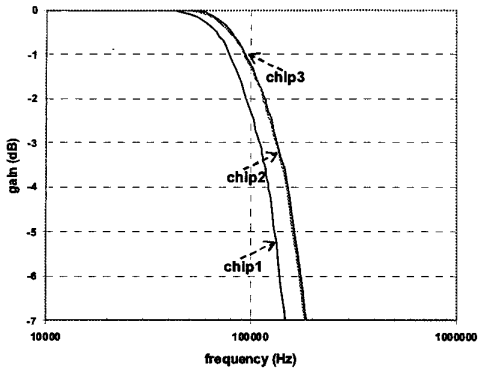

Figure 10 Frequency responses of 3 chips with power-up mismatch minimization scheme OFF. f_{-3dB1}=106kHz, f_{-3dB2}=129kHz, f_{-3dB3}=130kHz.

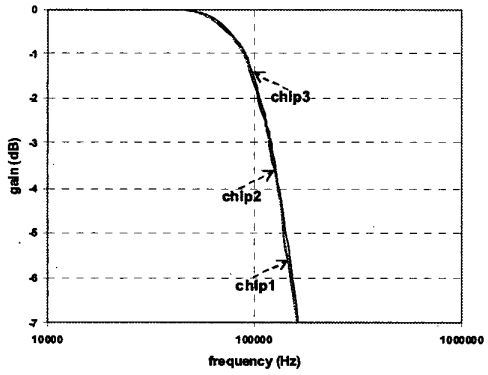

Figure 11 Frequency responses of 3 chips with the power-up mismatch minimization scheme ON. f_{-3dB1}=117kHz, f_{-3dB2}=119kHz, f_{-3dB3}=120kHz.

Table 1 Performance summary of the chip.

Performance Summary	
Corner Frequency	115kHz
Die Area	800ux500u
Power Consumption	Filter : 2.6mW(1V supply)
	Tuning : 7mW (1.8V supply when both tuning schemes are operational)
	Tuning : 2mW (1.8V supply when only indirect tuning scheme is operational)
Linearity(THD)	0.8V supply, 250mVpp, 10kHz signal: 0.01%
Signal to Noise Ratio (SNR)	0.8V supply, 250mVpp, 10kHz signal: 55dB**

** 84dB without flicker noise

6. Conclusion

A foreground tuning technique in conjunction with a master-slave based background tuning scheme is presented to track PVT variations and to minimize inherent mismatches between the master-slave filters. Challenges encountered in the design of truly low-voltage filters are discussed and techniques to improve linearity are presented.

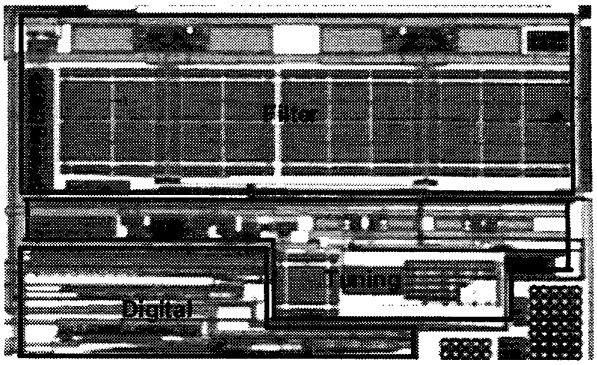

Figure 12 Die-photo of the fabricated chip.

A 115 kHz low-pass 2nd order Butterworth filter is implemented in 0.18μm CMOS technology. Measurements indicate a total harmonic distortion of -80 dB for a 10 kHz 250mVpp input signal with a supply voltage of 0.8V. Measured results also indicate good tuning accuracy in corner frequency when both of the tuning schemes are employed.

Acknowledgment

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